YOUR NAME ________________________________

Department of Electrical Engineering and Computer Science
Massachusetts Institute of Technology

6.012 Electronic Devices and Circuits

FINAL EXAMINATION

Open Book.

Notes:

1. Unless otherwise indicated, assume room temperature and that kT/q is 0.025 V, kT/q ln 10 = 60 mV, and $n_i = 10^{10}$ cm^{-3} for Si. Use q = 1.6 x 10^{-19} Coul.

2. This test is designed so that most parts can be worked independently of the others.

3. All of your answers and any relevant work must appear on these pages. Any additional paper you hand in will not be graded.

4. Make reasonable approximations and assumptions. State and justify any such assumptions and approximations.

5. Be certain that you have all twelve (12) pages of this exam booklet and make certain that you write your name at the top of this page as indicated.

6. You may see your final exam in Room 13-3058 beginning January 7, 2002.

Grader Use Only			
	PROBLEM 1	____________	(out of 30 possible)
	PROBLEM 2	____________	(out of 25 possible)
	PROBLEM 3	____________	(out of 20 possible)
	PROBLEM 4	____________	(out of 25 possible)
	TOTAL		

Problem 1 - (30 points) Three independent mini-problems

a) An isolated n-type Si sample with 10^{17} cm^{-3} donors, and having an electron mobility of 1600 cm^2/V-s, hole mobility of 600 cm^2/V-s, and minority carrier lifetime of 10^{-5} s, is illuminated with light generating G_L hole-electron pair/cm^3-s uniformly throughout its bulk, and leading to an excess hole population of 10^{18} cm^{-3}.

i) What are the thermal equilibrium carrier concentrations, n_o and p_o, in this sample at room temperature?

n_o = ____________________

p_o = ____________________

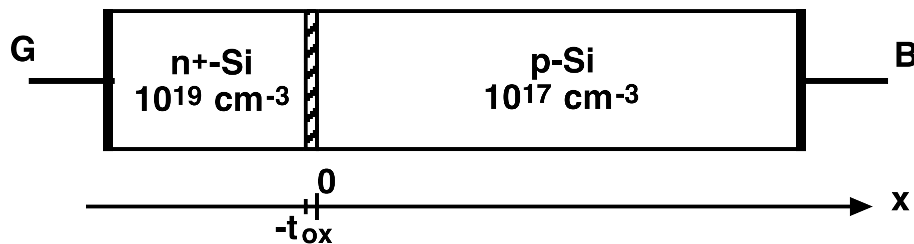
ii) What is the conductivity, σ, of the illuminated sample?

σ = ____________________

iii) How (approximately) are n' and p' related to G_L? Explain

______ $n',p' \propto G_L^{1/2}$ ______ $n',p' \propto G_L$ ______ $n',p' \propto G_L^2$, because

b) This mini-problem concerns the MOS capacitor structure illustrated below. In this structure the n^+-Si plays the role of the metal gate. The oxide thickness is 50 nm (5 x 10^{-6} cm) and its dielectric constant is 3.3 x 10^{-13} F/cm. The dielectric constant of Si is 10^{-12} F/cm and $n_i = 10^{10}$ cm^{-3} at room temperature.



i) What is the flatband voltage, V_{FB}, of this structure?

V_{FB} = ____________________

Problem 1 continues on the next page.

Problem 1 continued

ii) At threshold (that is, when the surface of the p-Si at $x = 0$ is at the threshold of inversion), what is the change in electrostatic potential, $\Delta\phi$, crossing the depletion region in the p-type Si and how wide is this depletion region?

$\Delta\phi$ = ______________________________

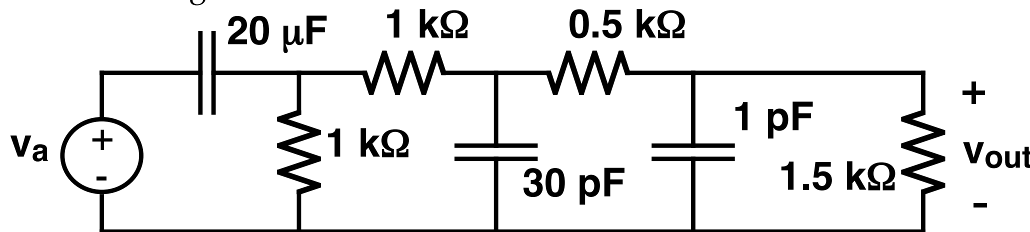
x_{Dp} = ______________________________

iii) What is the width of the depletion region and what is the potential change in the n^+-Si under the same conditions as in Part (ii)?

x_{Dn+} (in n^+-Si) = __________________________

$\Delta\phi$ (in n^+-Si) = __________________________

c) Consider the passive circuit shown below. In the mid-band range this circuit functions as a voltage divider.



i) What is the mid-band voltage gain, $A_v = v_{out}/v_a$, of this circuit?

A_v = ________________________

ii) What is ω_{LO} for this circuit?

ω_{LO} = ________________________

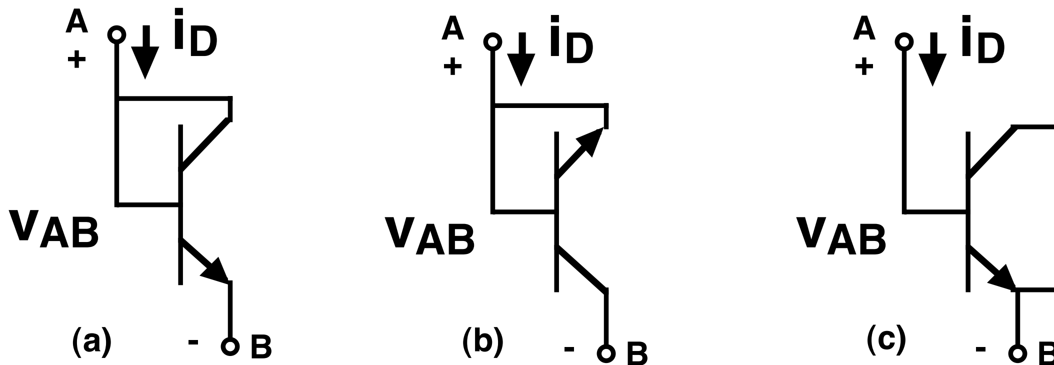
iii) Estimate ω_{HI} for this circuit.

ω_{HI} = ________________________

End of Problem 1

Problem 2 (25 points)

In an integrated circuit, when a designer needs a diode it is easiest to use a transistor and connect it so it functions as a diode. A transistor, after all, contains two p-n junctions. There are at least five ways to connect an npn transistor as a diode; three of them are pictured below:



For purposes of this question, assume that the npn bipolar junction transistor in question has a base doping that is 4 times the collector doping and 1/4 the emitter doping, that base width is the same as the emitter width and 1/2 the collector width, and that the electron mobility is twice the hole mobility; that is:

$N_{DE} = 4\,N_{AB} = 16\,N_{DC}$, $w_E = w_B$, $w_C = 2w_B$, and $\mu_e = 2\mu_h$

a) i) Which of these diode connections will have the largest small signal depletion capacitance at a reverse bias of 1 V, and why? Check all that apply.

a ( ) b ( ) c ( ) All are similar ( ) because:

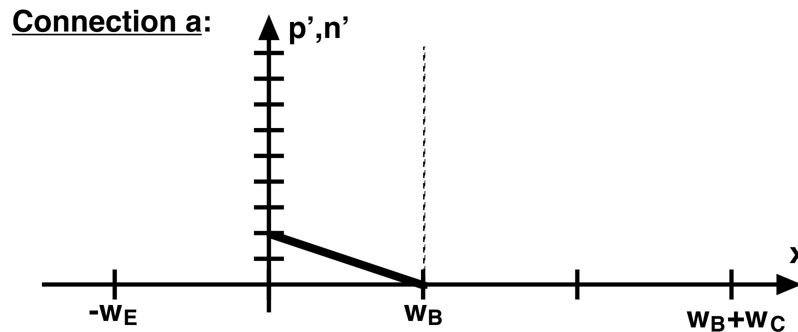
ii) Which of the three diode connections will have the largest small signal conductance about the bias point $I_D = 1$ mA, and why? Check all that apply.

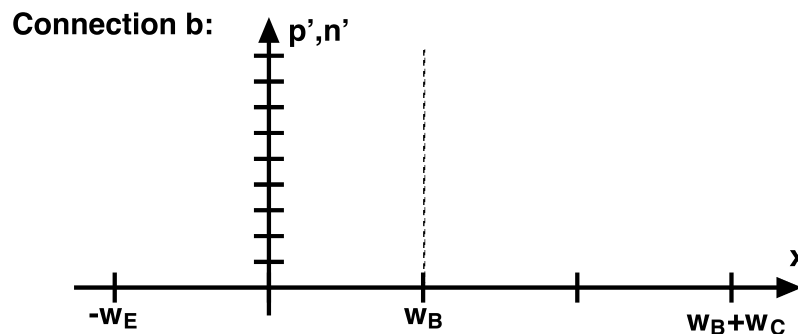
a ( ) b ( ) c ( ) All are similar ( ) because:

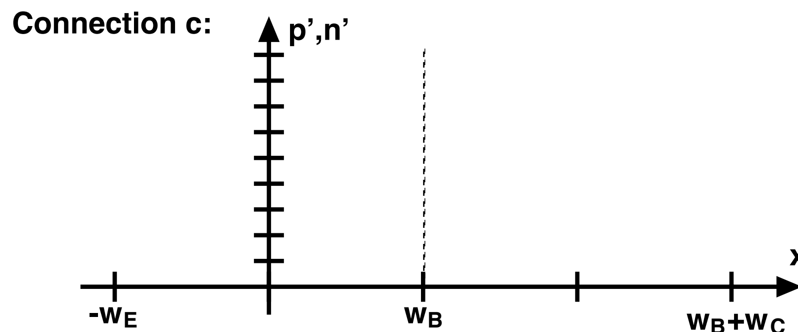
Problem 2 continues on the next page

Problem 2 continued

b) i) On the axes provided below sketch the excess carrier populations as a function of position in the emitter and collector, respectively, of connections a, b, and c, when a forward bias, V_{AB}, of 0.6V is applied to the diode. The profile in the base of Connection a is indicated on the axes; use the same scale in all plots.







ii) Which one of the three diode connections a, b, or c will have the <u>smallest</u> small signal <u>diffusion</u> <u>capacitance</u> at a forward bias of 0.6 V, and why?

a ( ) b ( ) c ( ) All are similar ( ) because:

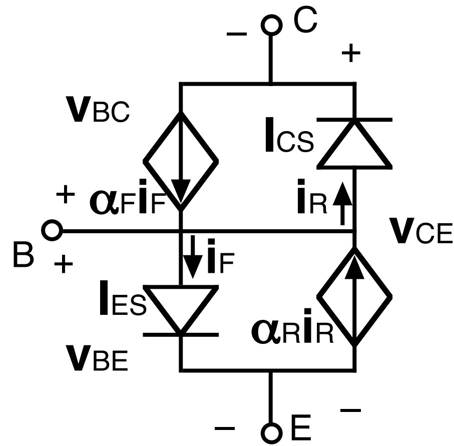
Problem 2 continues on the next page

Problem 2 continued

c) Use the Ebers-Moll Model for the large signal characteristics of a bipolar junction transistor (pictured below) to show that i_D vs v_{AB} of Connection c can be written as

$$i_D = I_{DS} (\exp qv_{AB}/kT - 1)$$

and find an expression for I_{DS} of Connection c in terms of the Ebers-Moll Model parameters.

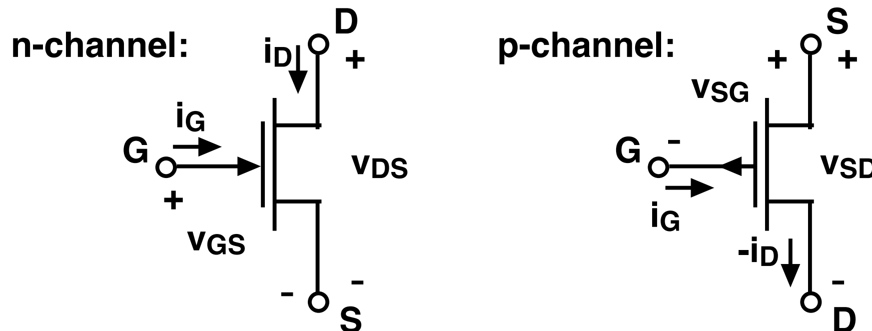


I_{DS} = ____________________

End of Problem 2

Problem 3 - (20 points)

A SATFET is a field effect transistor having three terminals (gate, source, and drain) and represented by the symbol below; it can be either n- or p-channel. A



SATFET is similar to a MOSFET but has somewhat <u>different</u> terminal characteristics. The static terminal characteristics of n- and p- channel SATFETs are as follows:

<u>n-channel</u>

$i_G = 0$ under all conditions

$$i_D = \begin{cases} 0 & \text{if } v_{GS} < V_T \\ A\,(v_{GS} - V_T)\, v_{DS}\,(1 + \lambda v_{DS}) & \text{if } v_{GS} > V_T \text{ and } 0 < v_{DS} < V_{Sat} \\ B\,(v_{GS} - V_T)\,(1 + \lambda v_{DS}) & \text{if } v_{GS} > V_T \text{ and } v_{DS} > V_{Sat} \end{cases}$$

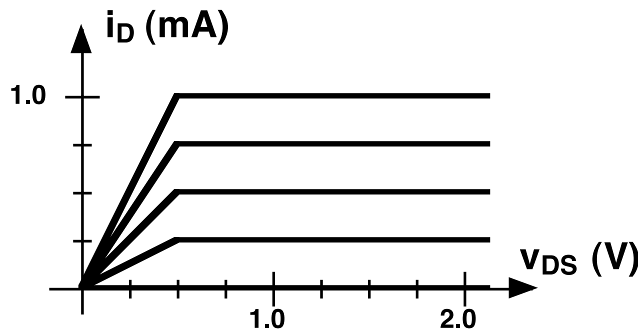
<u>p-channel</u>

$i_G = 0$ under all conditions

$$-i_D = \begin{cases} 0 & \text{if } v_{SG} < V_T \\ A\,(v_{SG} - V_T)\, v_{SD}\,(1 + \lambda v_{SD}) & \text{if } v_{SG} > V_T \text{ and } 0 < v_{SD} < V_{Sat} \\ B\,(v_{SG} - V_T)\,(1 + \lambda v_{SD}) & \text{if } v_{SG} > V_T \text{ and } v_{SD} > V_{Sat} \end{cases}$$

with $V_T = 0.25$ V, $V_{Sat} = 0.5$ V, $\lambda = 0.01\ V^{-1}$, $A = 2 \times 10^{-3}\ A/V^2$, $B = 10^{-3}\ A/V$.

The output characteristics (i.e., i_D vs v_{DS}) for an <u>n-channel</u> SATFET are shown below for the range $0 < v_{DS} < 2$ V, for $v_{GS} = 0, 0.5, 0.75,$ and 1.0 V. Note that λ has been approximated as being zero for purposes of this sketch.

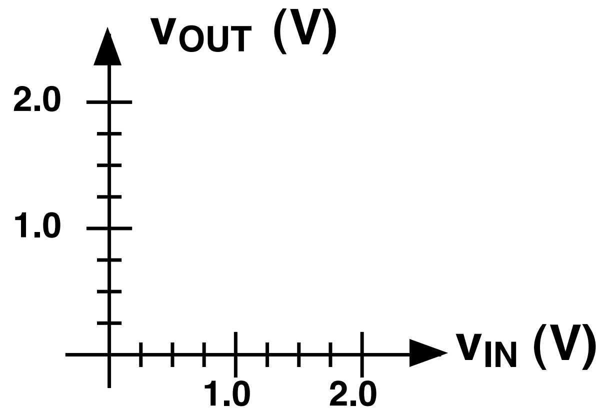


a) Indicate on the characteristics what region corresponds to the "forward active region", i.e., what would be the preferred bias region when using this device in linear amplifier applications.

Problem 3 continues on the next page

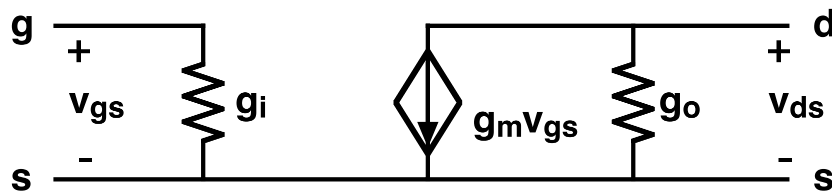
Problem 3 continued

b) i) In the space to the left below draw a complementary SATFET inverter stage that would be the analog of a CMOS inverter.



ii) On the axes provided above to the right plot the transfer characteristic of the SATFET inverter you drew above on the left. Assume that the power supply voltage is 2 V, and approximate λ as zero (for this part only).

c) A possible incremental linear equivalent circuit for this device is shown below. Find expressions for g_i, g_m, and g_o valid for bias points for which $V_{GS} > V_T$ and $V_{DS} > V_{Sat}$. Give your expressions in terms of the approximate quiescent currents.



i) Input conductance, g_i:

g_i = ________________________________

ii) Transconductance, g_m:

g_m = ________________________________

Problem 3 continues on the next page

Problem 3 continued

iii) Output conductance, g_o:

$g_o =$ ____________________________

d) This question concerns the open-circuit mid-band incremental voltage gain of a SATFET, $A_{v,oc}$, and how it depends on the bias current.

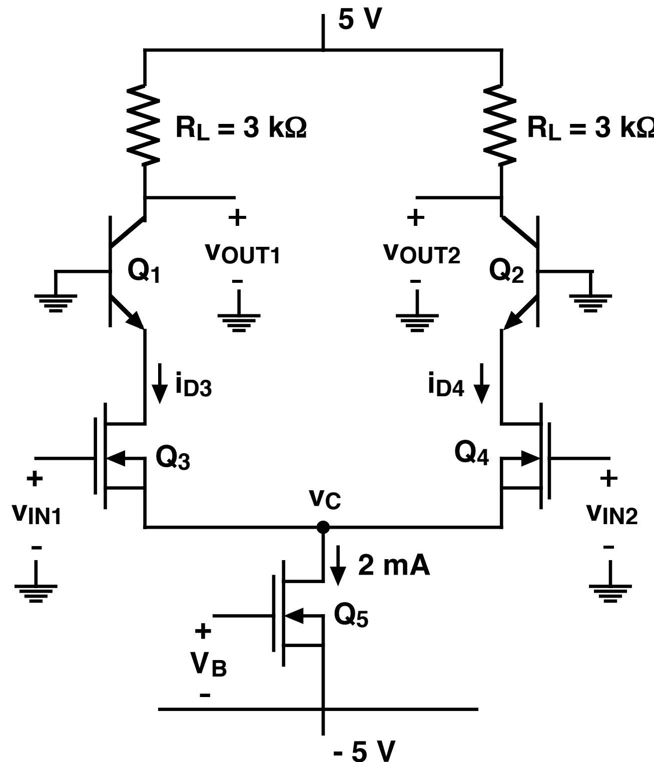
i) Derive and expression for the small-signal, mid-band open-circuit voltage gain, A_{voc}, of a SATFET as a function of the approximate drain current.

ii) In 25 words or less compare this behavior to that of a MOSFET and a BJT.

End of Problem 3

Problem 4 - (25 points)

The circuit below uses three identical n-channel MOSFETs and two identical npn BJTs in a differential amplifier. Note that each side of the differential amplifier is a cascode circuit. The transistor characteristics are listed below the circuit.



Characteristics: n-channel MOSFETs: $K = 2 \times 10^{-3}$ A/V^2, $V_T = 1$ V, $|V_a| = 20$ V.
npn BJTs: $\beta = 100$, $v_{BE} \cong 0.6$ V at the current of interest, $|V_a| = 100$ V.

a) With both inputs zero (i.e, $v_{IN1} = v_{IN2} = 0$) determine the indicated quiescent currents and voltages. Specify units:

i) I_{D3} (= I_{D4})

I_{D3} = ________________________

ii) V_{OUT1} (= V_{OUT2})

V_{OUT1} = ________________________

iii) V_C

V_C = ________________________

Problem 4 continues on the next page.

Problem 4 continued

iv) V_{CE1} (= V_{CE2})

V_{CE1} = ____________________

v) V_{DS3} (= V_{DS4})

V_{DS3} = ____________________

b) In the spaces provided below draw two mid-band linear equivalent half circuits (LEHCs) for this differential amplifier, one for common-mode inputs and one for difference-mode inputs. Label all of the elements in them.

i) Common-mode LEHC:

ii) Difference-mode LEHC:

c) Derive literal expressions for the common-mode and difference-mode voltage gains, A_{vc} and A_{vd}, respectively, of this differential amplifier. Use the definitions for A_{vc} and A_{vd} indicated by the blanks provided for your answers. The output conductances of Q_1, Q_2, Q_3, and Q_4 are of insignificant effect and should be neglected in these derivations.

i) Common-mode voltage gain, $A_{vc} = v_{oc}/v_{ic}$:

$A_{vc} = v_{oc}/v_{ic}$ = ______________________________

Problem 4 continues on the next page

Problem 4 continued

ii) Difference-mode voltage gain, $A_{vd} = v_{od}/v_{id}$:

$A_{vd} = v_{od}/v_{id} =$ ______________________________

End of Problem 4

End of Exam

Happy Holidays; have a great IAP