

MASSACHUSETTS INSTITUTE OF TECHNOLOGY
 Department of Electrical Engineering and Computer Science

6.012 ELECTRONIC DEVICES AND CIRCUITS

Problem Set No. 8

Issued: October 24, 2003

Due: October 31, 2003

Reading Assignments:

- Lecture 15 (10/26/03) - Chap. 15 (15.1, 15.2)
- Lecture 16 (10/28/03) - Chap. 15 (15.2.4)
- Lecture 17 (10/30/03) - Chap. 11 (11.1, 11.2)
- Lecture 18 (11/4/03) - Chap. 11 (11.3 to end)
- Lecture 19 (11/6/03) - Chap. 12 (12.1, 12.2)

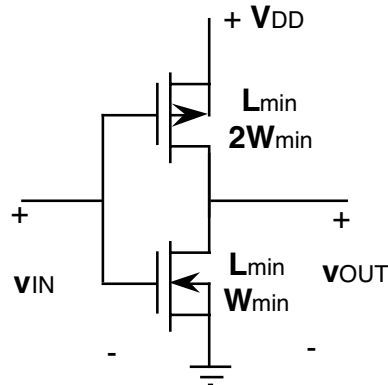
The second hour exam is scheduled for Wednesday night, November 5, from 7:30 to 9:30 pm in Room 10-250. The exam is closed book and will cover the material through 10/29/03 and Problem Set #8, including BJT operation and large signal modeling; the MOS capacitor; MOSFET operation and large signal modeling; incremental models for diodes, BJTs, and MOSFETs; and MOSFET inverters. There will be no weblab or HSPICE questions on the exam.

Problem 1 - (a) Do Problem 15.8 in the course text, doing only case $V_{TN} = |V_{TP}| = 0.5$ V in Part b of this problem (that is, do not do 0.75 V). Use $\alpha = 1$. Also, in Part b, consider the statement made that it should be clear to you that it is desirable to reduce the threshold voltage. This might not be so clear. In fact good reasons can be found for making the the threshold large, also. Give some arguments on each side, and particularly in Part c discuss how large and how small V_T could safely be made if the process being used gives you an uncertainty of ± 0.1 V in V_T .

(b) Do Problem 15.7 in the course text.

Problem 2 - Do Problem 10.1 in the course text using $L = 0.25$ μm (rather than 1.0 μm as specified in the problem statement).

Problem 3 - This problem deals with CMOS inverters fabricated using a process for which the minimum gate length and width are L_{\min} and W_{\min} , respectively. In order to obtain symmetrical transfer characteristics and minimize the gate delay, the inverters are designed to have $V_{Tn} = |V_{Tp}|$, $t_{oxn} = t_{oxp}$, and $K_n = K_p$. All the inverters have minimum length gates, i.e., $L_n = L_p = L_{\min}$, and the width of the p-channel devices is twice that of the n-channel devices, i.e., $W_p = 2W_n$, because the hole and electron mobilities in the channel differ by a factor of two, i.e., $\mu_e = 2\mu_p$. The smallest inverters have $W_n = W_{\min}$ and $W_p = 2W_{\min}$, and we will call the corresponding K value K_{\min} .



This minimum size inverter is shown above. The gate delay, τ_{GD} , of this minimum size inverter is found to be 100 ps (10^{-10} s) when the fan-out is one. We will call this gate delay the minimum gate delay, τ_{min} .

- (a) What is the gate delay of a minimum-size inverter which has a fan-out of four, i.e., when its output is connected to four stages?
- (b) Suppose that some of the minimum-size inverters on an integrated circuit chip were mistakenly designed with $W_n = W_p = W_{min}$. Determine what impact this has on the gate delay, τ_{GD} , of these inverters, and calculate their gate delay.
- (c) The inverters which drive the bond pads and the wires going to other chips must supply much larger currents because they have much larger capacitances to charge and discharge than do the inverters which simply drive other inverters on the same chip. We will call these "output inverters." Suppose that on the present chip, the MOSFETs in the output inverters must have K values of $100 K_{min}$.
 - (i) What are W_n and W_p of the devices in the output inverters?
 - (ii) What is the input capacitance of these output stages in terms of the input capacitance of a minimum-size inverter, which you can call C_{min} ?
 - (iii) What would the gate delay be for a minimum-size inverter loaded with a single output inverter stage, i.e., loaded with the capacitance you found above in Part (c)(ii)?
- (d) Consider inserting an inverter stage with $K = 10 K_{min}$ between the minimum-size inverter and an output inverter.
 - (i) Draw the circuit schematic for these three inverter stages, indicating next to each device its gate width.
 - (ii) What are the gate delays, τ_{GD} 's, for the first (K_{min}) and second ($10 K_{min}$) stages in this circuit?

- (iii) What is the total delay going through both the K_{\min} and 10 K_{\min} stages, and how does it compare with your answer in Part (c)(iii)?
- (iv) If one intermediate stage before an output stage is good, are two better? How about n , where $n > 2$? Is there an optimum n ?

Problem 4 - This problem concerns using small signal modeling to examine the slope of the transfer characteristics of the n-MOS inverter in Figure 15.11(a) of the course text in Region III. Use the transistors described in the caption of this figure, with the added information that $\lambda = 0.1 \text{ V}^{-1}$ ($V_A = 10 \text{ V}$) and $\eta = 0.1$ for both transistors.

- (a) i) Draw a small signal linear equivalent circuit for this inverter which is valid about an operating point in Region III, which is where both transistors are in saturation. [Remember that the supply, V_{DD} , is incrementally 0 V, i.e., ground.]
- ii) Evaluate the voltage gain, $A_v (= v_{\text{out}}/v_{\text{in}} = dv_{\text{OUT}}/dv_{\text{IN}}|_Q)$, when $V_{\text{IN}} = V_{\text{OUT}} = V_{\text{TR}}$ (also called V_M) $\approx 3 \text{ V}$. [This is not the exact value of V_{TR} , but it is sufficiently close to use in this exercise.]
- (b) In traditional IC processes it is impossible to connect the substrate of Q_L in this circuit to its source, but in some modern processes it is possible to do this. What would the voltage gain of this circuit be if the substrate of Q_L is connected to its source, i.e. if $v_{\text{bsL}} = 0$? [This is mathematically equivalent to saying $\eta = 0$ for Q_L .]

Problem 5 - This problem concerns the transfer characteristics of a CMOS inverter like that illustrated in Figure 15.12a (the same as in Problem 1).

- (a) Calculate by hand and sketch the transfer characteristics for the case $K_p \equiv \mu_p C_{\text{ox}} = 27.5 \mu\text{A}/\text{V}^2$, and $K_n \equiv \mu_n C_{\text{ox}} = 80 \mu\text{A}/\text{V}^2$, $L_n = L_p = 1.5 \mu\text{m}$, $W_n = W_p = 3 \mu\text{m}$, $V_{\text{Th}} = -V_{\text{Tp}} = 1 \text{ V}$. In your sketch, do accurate sketches in regions I, III, and V, and rough sketches in regions II and IV. Ignore the body effect (i.e. assume $\eta = 0$) and the Early effect (i.e., assume $\lambda [\equiv 1/|V_A|] = 0$).
- (b) Use HSPICE to calculate the transfer characteristic of this same gate, but with a variety of device widths: $W_p/W_n = 60 \mu\text{m}/3 \mu\text{m}$, $30\mu/3\mu$, $3\mu/3\mu$, $3\mu/12\mu$, and $3\mu/24\mu$.
- (c) Comment on the changes you see in the transfer characteristics when W_p/W_n is changed.

Problem 6 - This problem has two parts; one deals with two bipolar transistors, the other with two MOSFETs. Think of it as a warm-up review for Hour Exam 2.

- (a) Consider two npn silicon bipolar junction transistors, A and B. All of the dimensions of these two devices, and the magnitudes of all of the doping levels in these two

devices are identical, except that the base width, w_B , of Transistor A is twice that of Transistor B.

- (i) Which transistor, if either, has the larger dc current gain, β_F ? Explain your answer and estimate the ratio of the two β_F 's.
 - (ii) Which transistor, if either, has the larger emitter-base junction saturation current, I_{ES} ? Explain your answer and estimate the ratio of the two I_{ES} 's.
 - (iii) With the base-collector junctions of both transistors reverse biased with the same values of base-collector junction voltage, V_{BC} , which transistor, if either, has the largest small-signal base-collector junction capacitance, C_{μ} ? Explain your answer and estimate the ratio of the two C_{μ} 's.
 - (iv) With both transistors biased at the same quiescent collector current level, I_C , which transistor, if either, has the largest small-signal transconductance, g_m ? Explain your answer and estimate the ratio of the two g_m 's.
 - (v) With both transistors biased at the same quiescent collector current level, I_C , which transistor, if either, has the largest small-signal input resistance, r_{π} ? Explain your answer and estimate the ratio of the two r_{π} 's.
 - (vi) Which transistor, if either, has a larger Early voltage, V_A ? Explain your answer.
- (b) Consider an n-channel silicon MOSFET and a p-channel silicon MOSFET which are identical in all dimensions and doping level magnitudes except that the gate length, L , of one of the devices is twice that of the other. The K-factors in the large signal characteristics are also identical. [The K-factor is defined as $(W/L)\mu(e_{ox}/t_{ox})$.]
- (i) Which transistor, if either, would you expect to be the one with the longer gate length, and why?
 - (ii) What is the ratio of the electron to hole mobility in these transistors (i.e., what is the ratio of the mobility of the electrons in the channel of the n-channel MOSFET to that of the holes in the channel of the p-channel MOSFET)? Explain.
 - (iii) Which transistor, if either, has the larger small-signal gate-to-source capacitance in saturation, C_{gs} ? Explain your answer.
 - (iv) Which transistor, if either, has the larger small-signal gate-to-drain capacitance in saturation, C_{gd} ? Explain your answer.
 - (v) Both transistors are biased in saturation so they have the same magnitude of quiescent drain current, I_D . Which transistor, if either, has the largest small-signal transconductance, g_m ? Explain your answer and estimate the ratio of the two g_m 's.
 - (vi) Which transistor, if either, has a larger Early voltage, V_A ? Explain your answer.