

Lecture 11 - The MOS Capacitor - Outline

- **Announcements**

 - Handout - Lecture Outline and Summary

 - Exams - Will be returned in recitation next Wed.

- **Qualitative description - MOS in thermal equilibrium**

 - Definition of structure: metal/silicon dioxide/p-type Si (Example: n-MOS)

 - Electrostatic potential of metal relative to silicon: ϕ_m

 - Zero bias condition: Si surface depleted if $\phi_m > \phi_{p-Si}$ (typical situation)

 - Negative bias on metal: depletion to flat-band to accumulation

 - Positive bias on metal: depletion to threshold to inversion

- **Quantitative modeling - MOS in thermal equilibrium, $v_{BC} = 0$**

 - Depletion approximation applied to the MOS capacitor

 - 1. Flat-band voltage, V_{FB}

 - 2. Accumulation layer sheet charge density, q_A^*

 - 3. Maximum depletion region width, X_{DT}

 - 4. Threshold voltage, V_T

 - 5. Inversion layer sheet charge density, q_N^*

- **MOS with bias applied to the adjacent n⁺-region**

 - Implication for depletion region width

 - Impact on threshold voltage

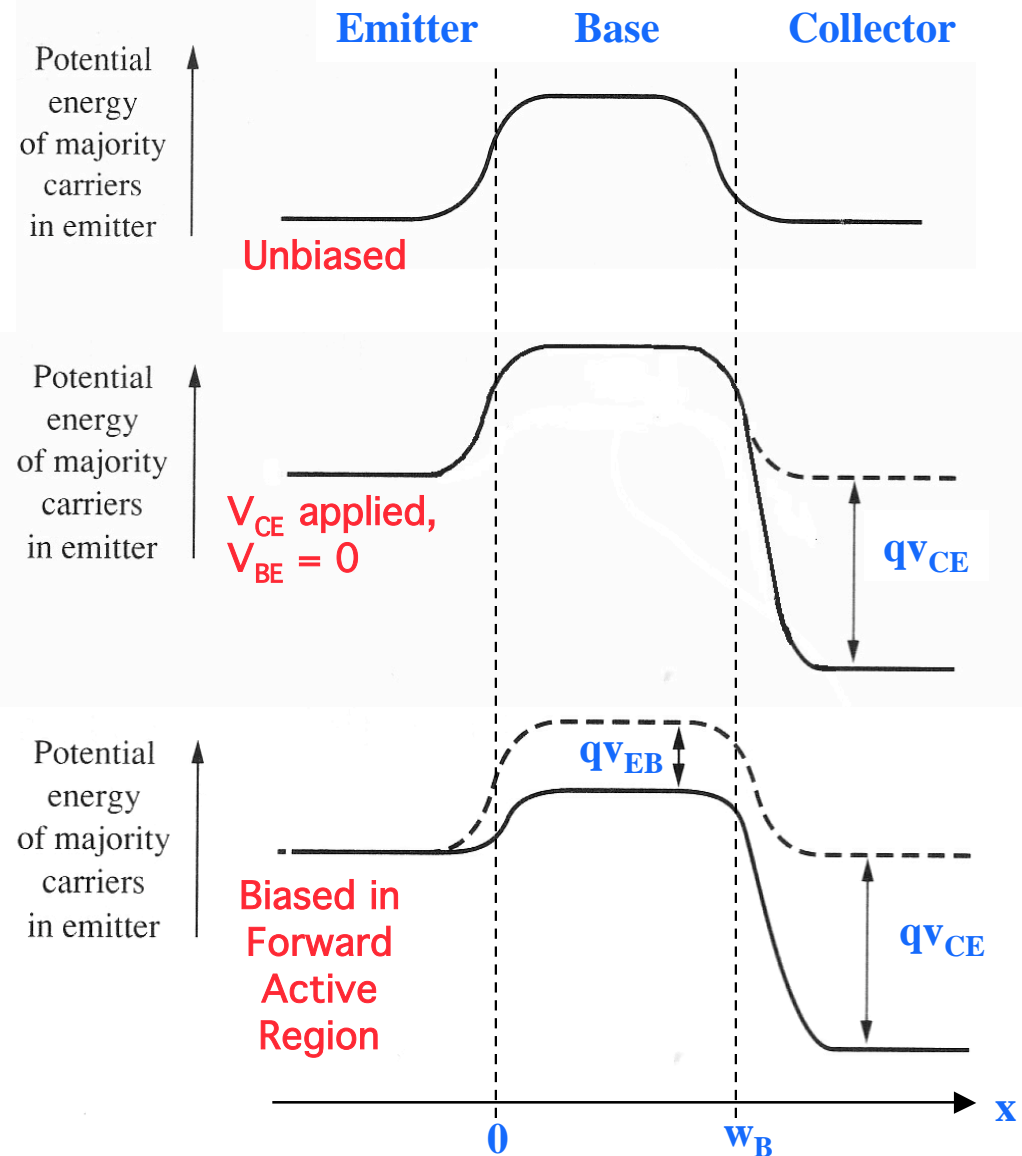
Another view of bipolar transistor operation:

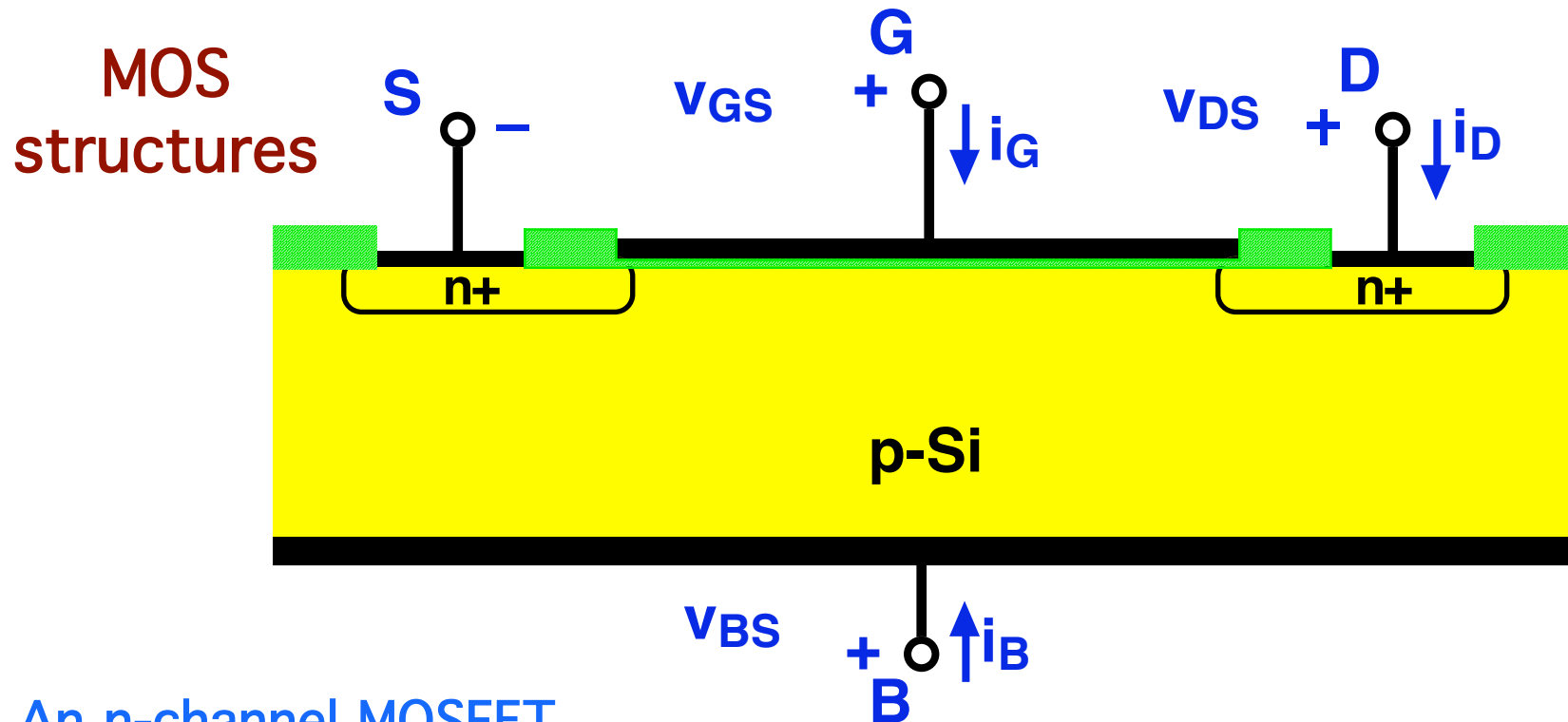
Changing the potential energy barrier between emitter and collector with the B-E voltage

The p-type base region places a potential energy barrier for electrons, $q\phi_b$, between the n-type emitter and collector regions.

When the collector is biased positive relative to the emitter is becomes attractive to electrons, but the electrons are still blocked from flowing to the collector by the potential barrier at the EB junction.

Electrons can only flow from the emitter to the collector when this potential barrier, $q\phi_b$, is reduced by applying a forward bias on the base-emitter junction. [It is reduced to $q(\phi_b - V_{BE})$.]





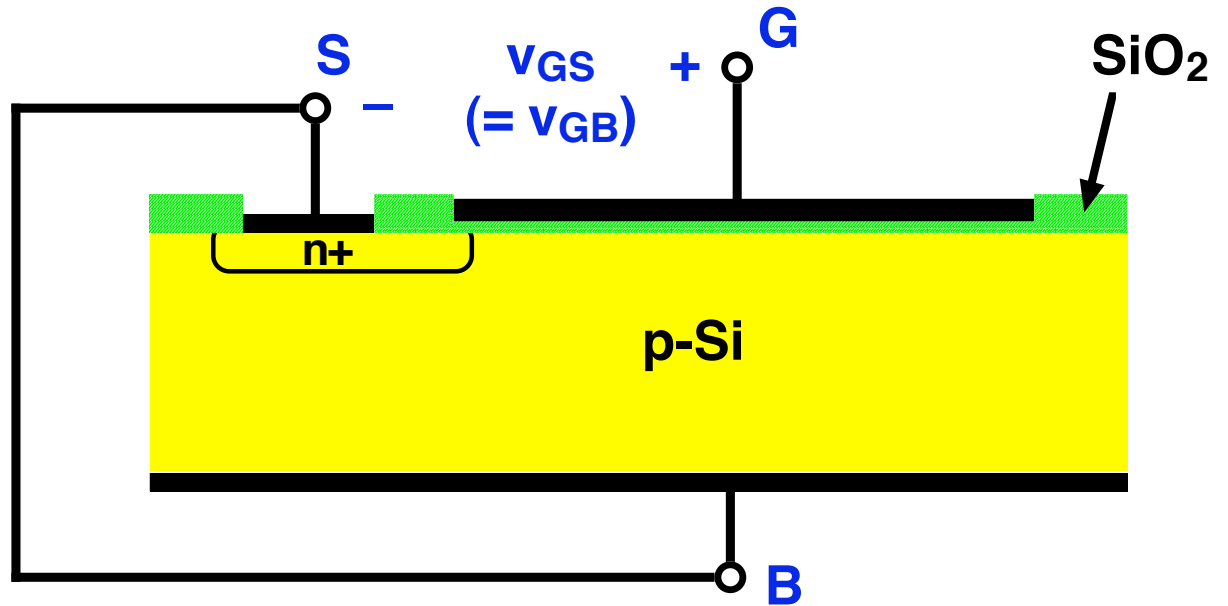
An n-channel MOSFET

In an n-channel MOSFET, we have two n-regions (the source and the drain), as in the npn BJT, with a p-region producing a potential barrier for electrons between them. In this device, however, it is the voltage on the gate, v_{GS} , that modulates the potential barrier height.

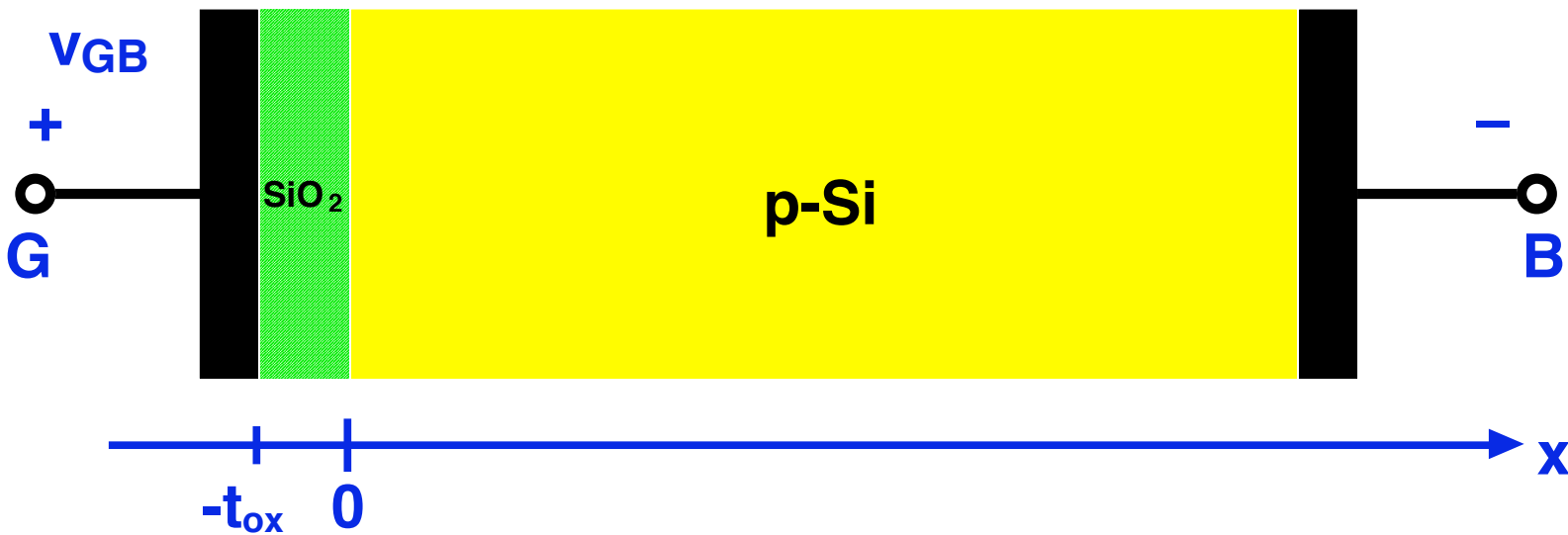
The heart of this device is the MOS capacitor, which we will study today. To analyze the MOS capacitor we will use the depletion approximation that we introduced in conjunction with p-n junctions.

The n-MOS capacitor

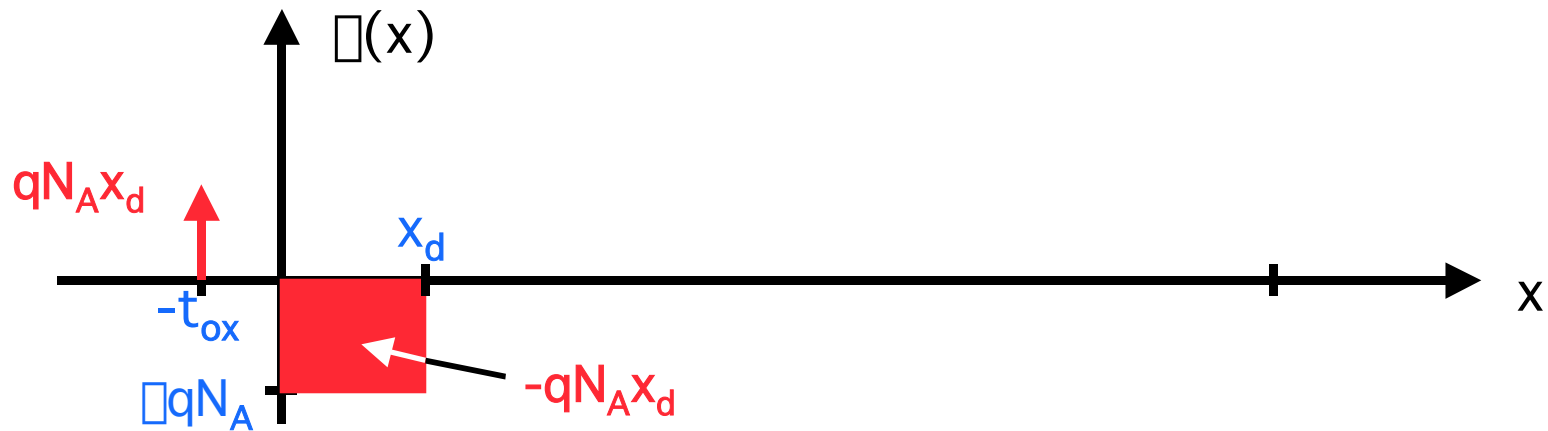
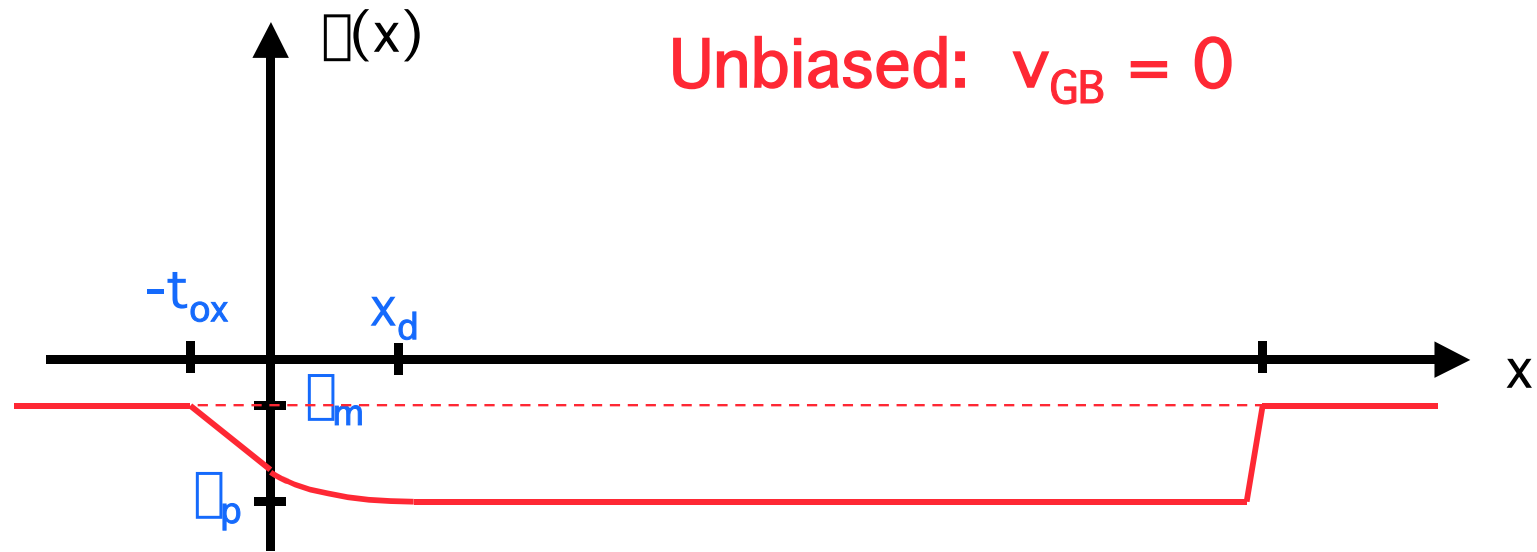
Right: Basic device with $v_{BC} = 0$



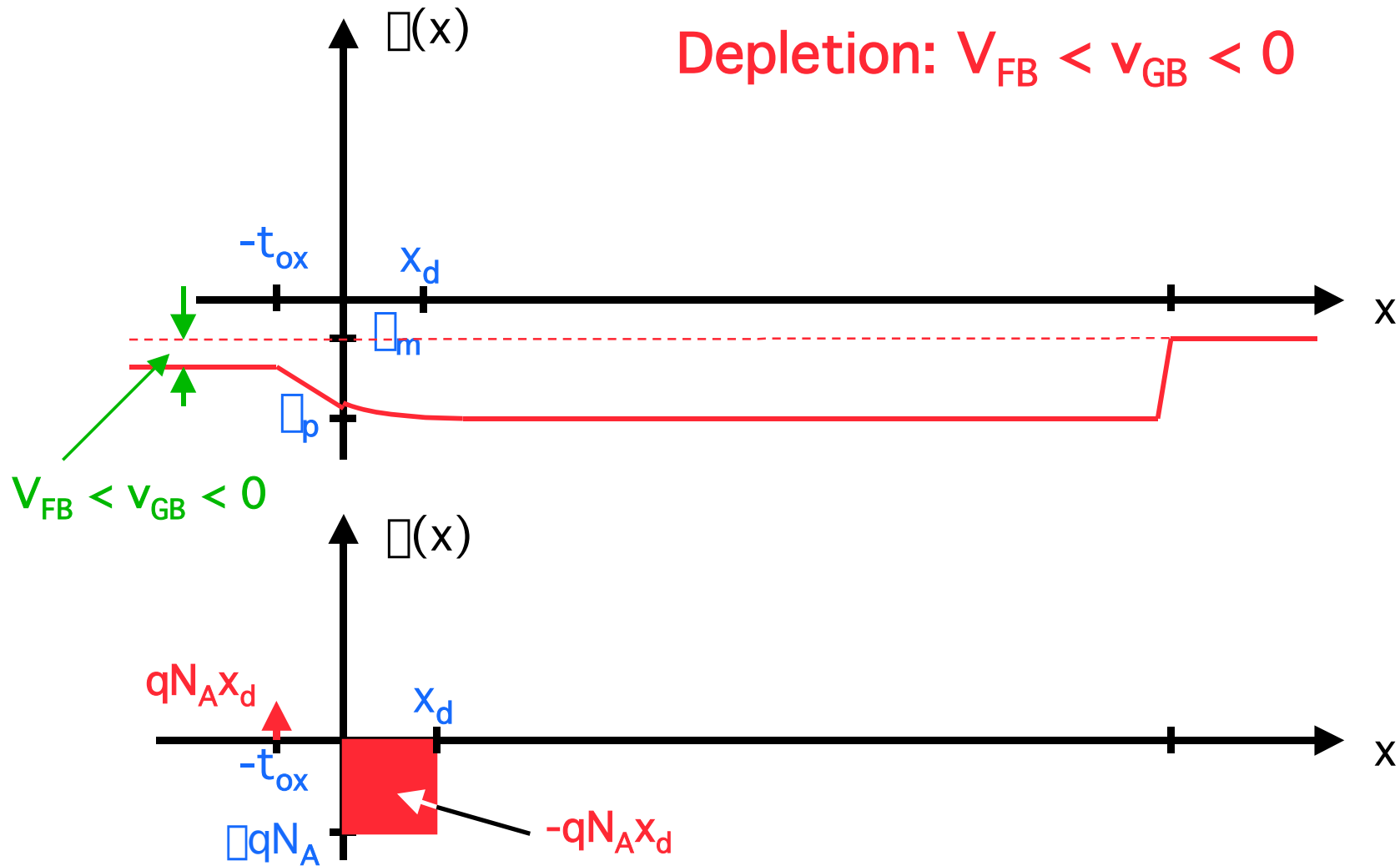
Below: One-dimensional structure for depletion approximation analysis



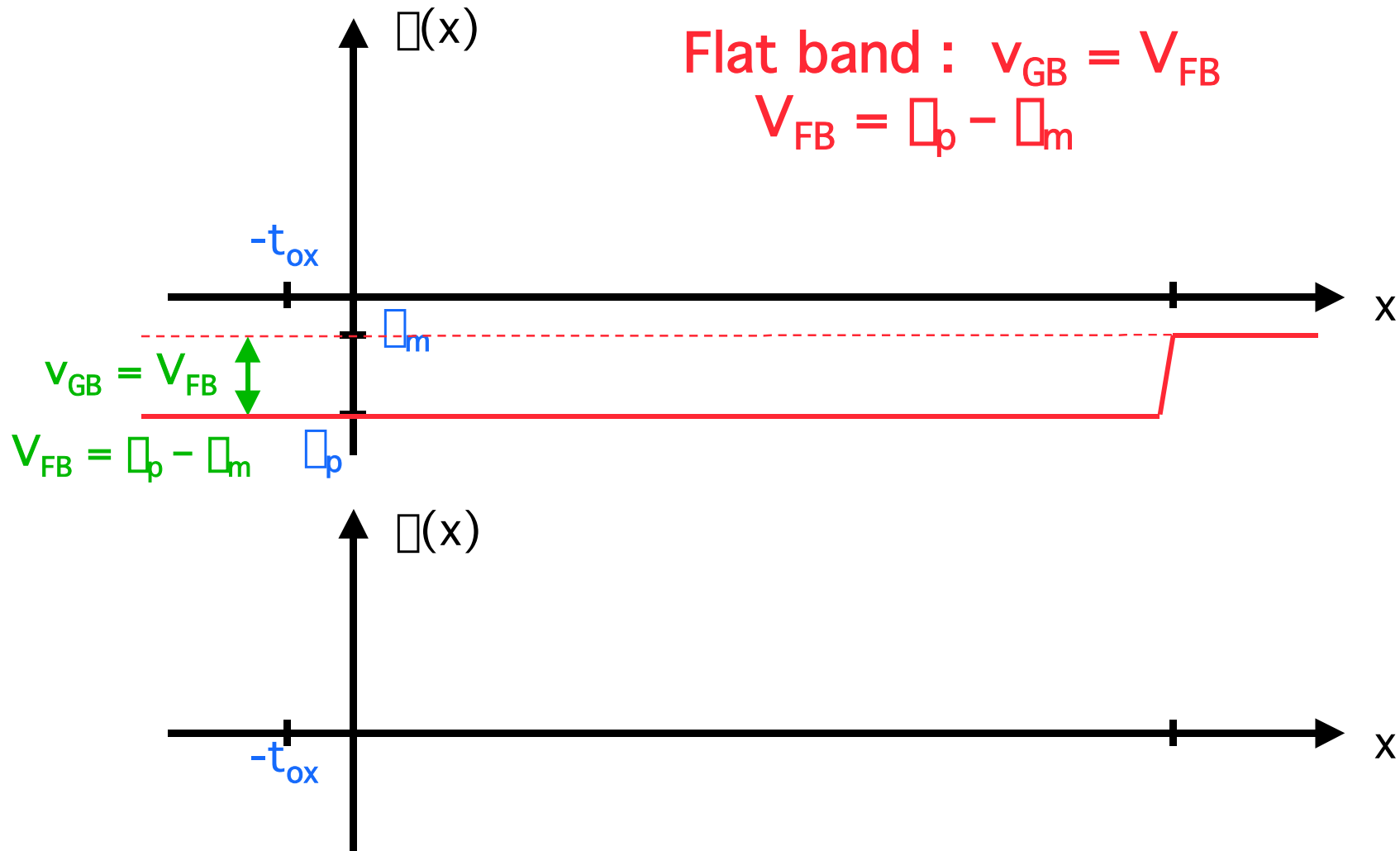
Electrostatic potential and net charge profiles



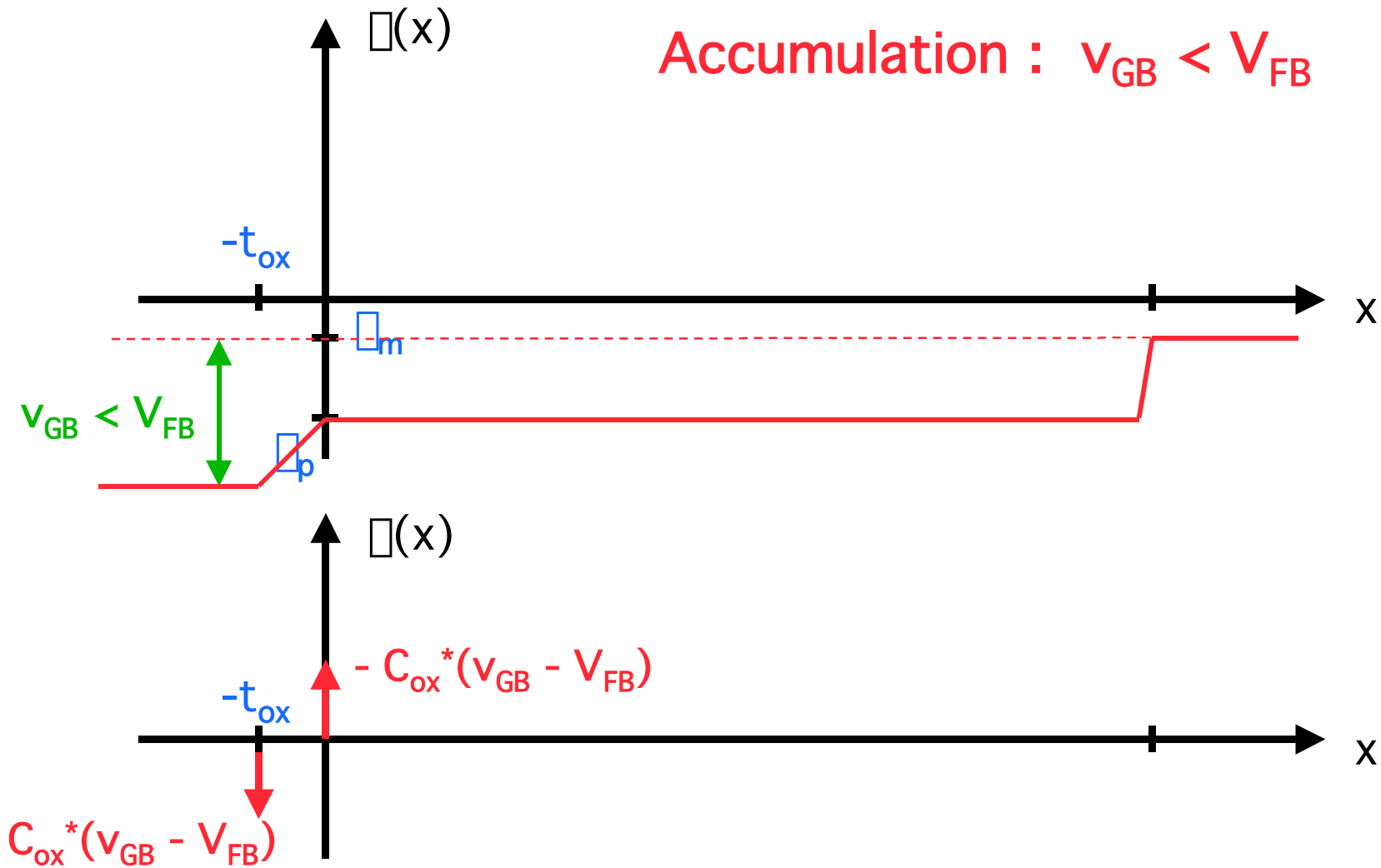
Electrostatic potential and net charge profiles



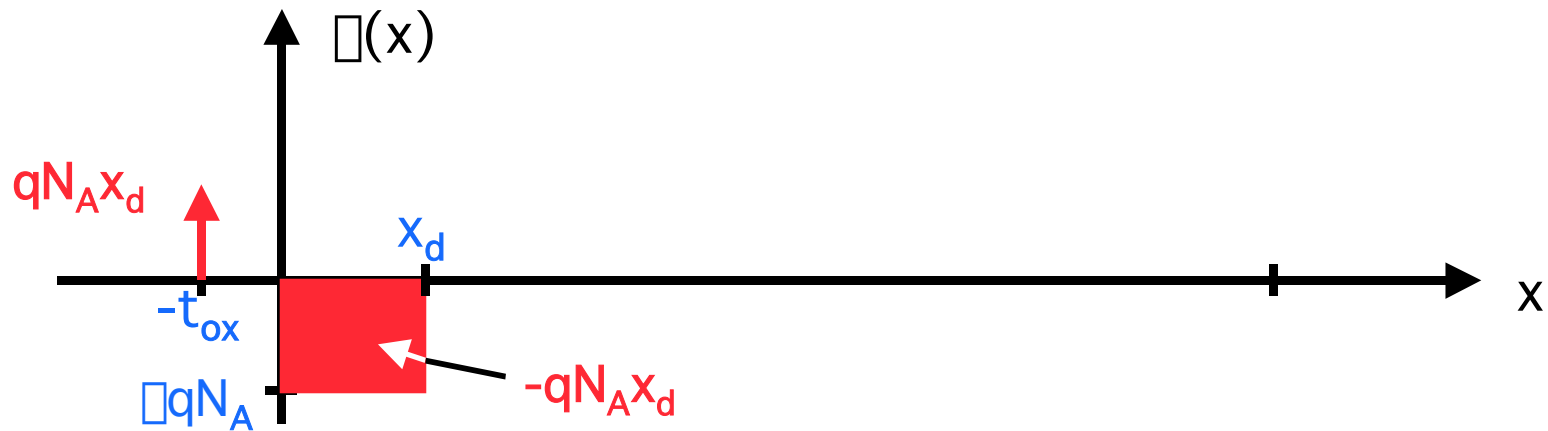
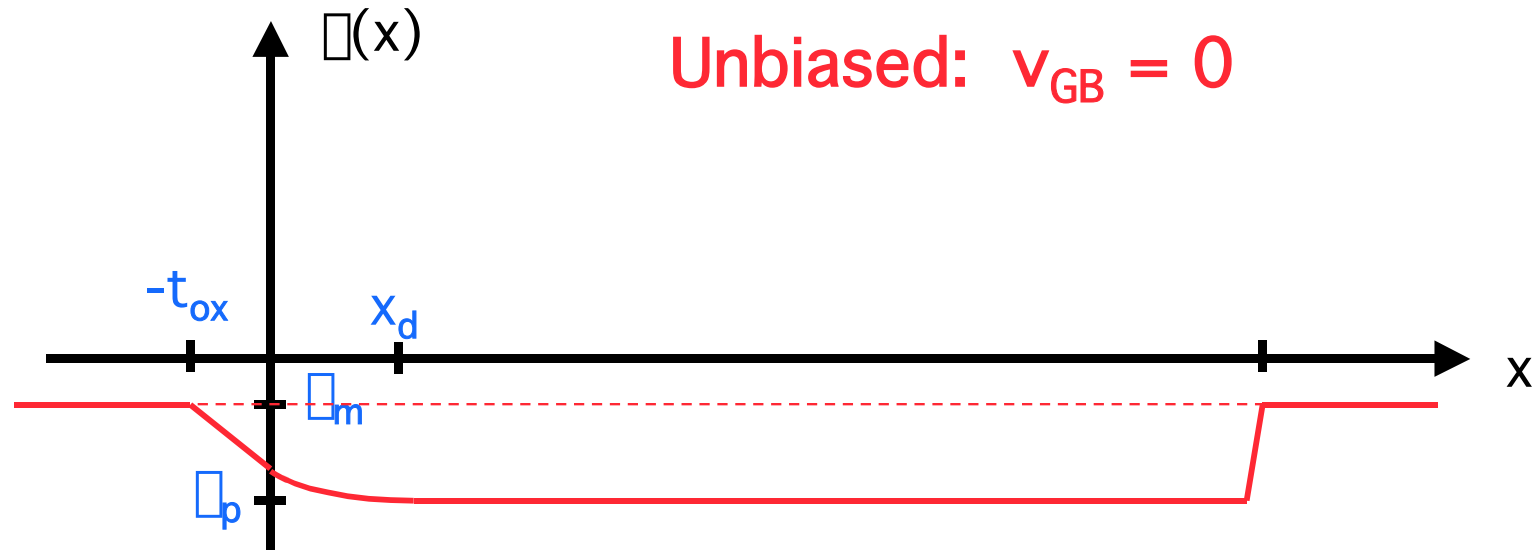
Electrostatic potential and net charge profiles



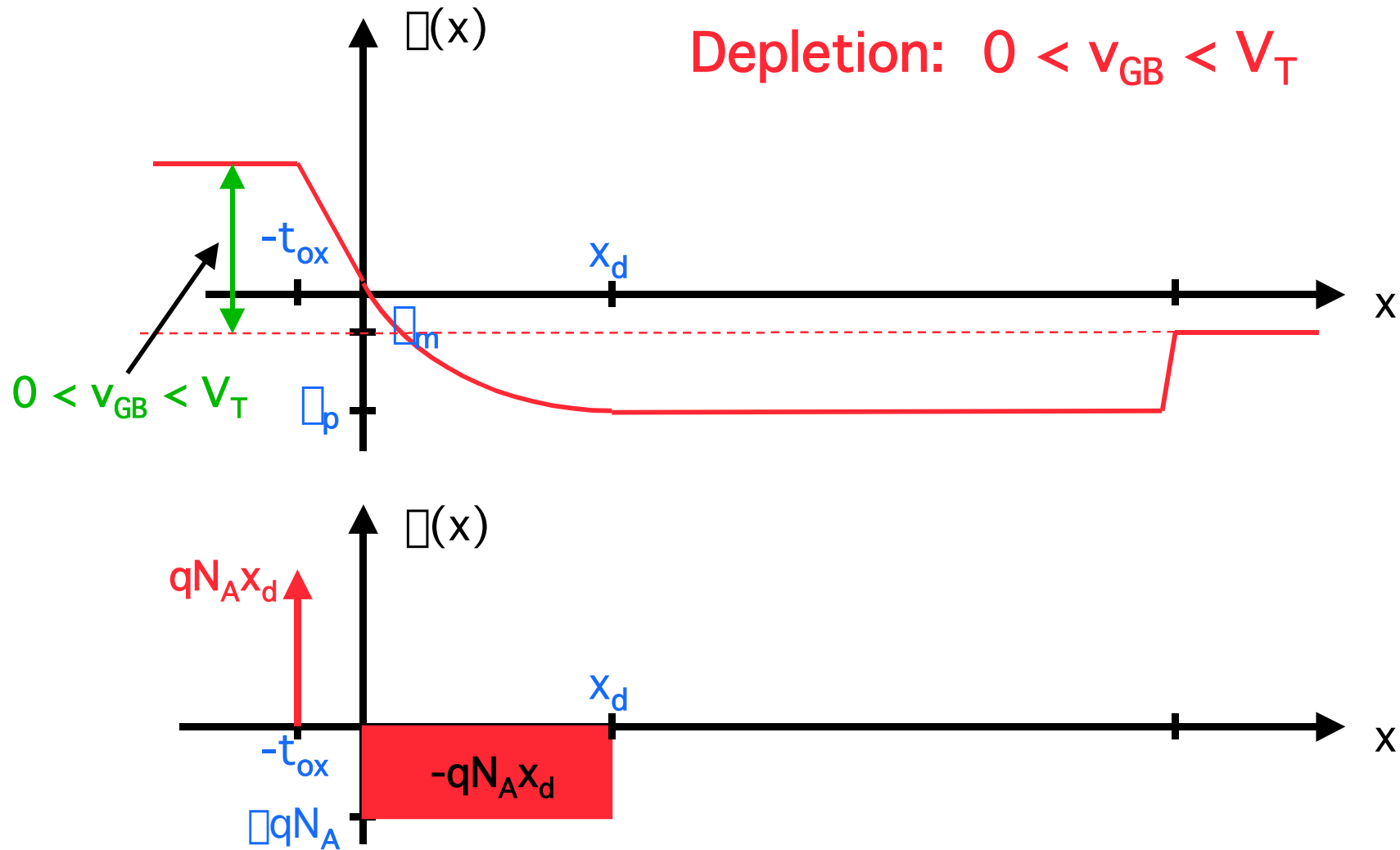
Electrostatic potential and net charge profiles



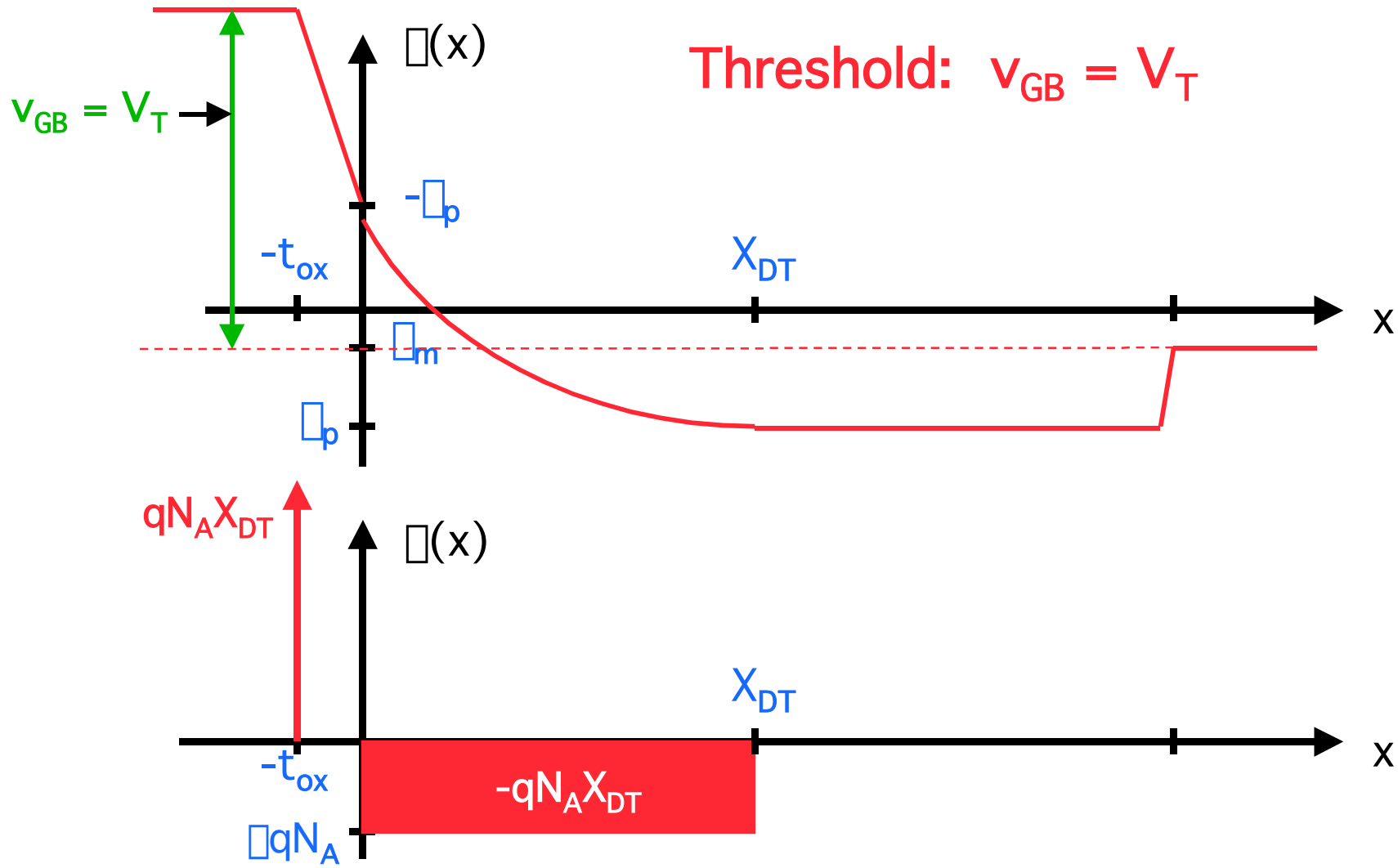
Electrostatic potential and net charge profiles



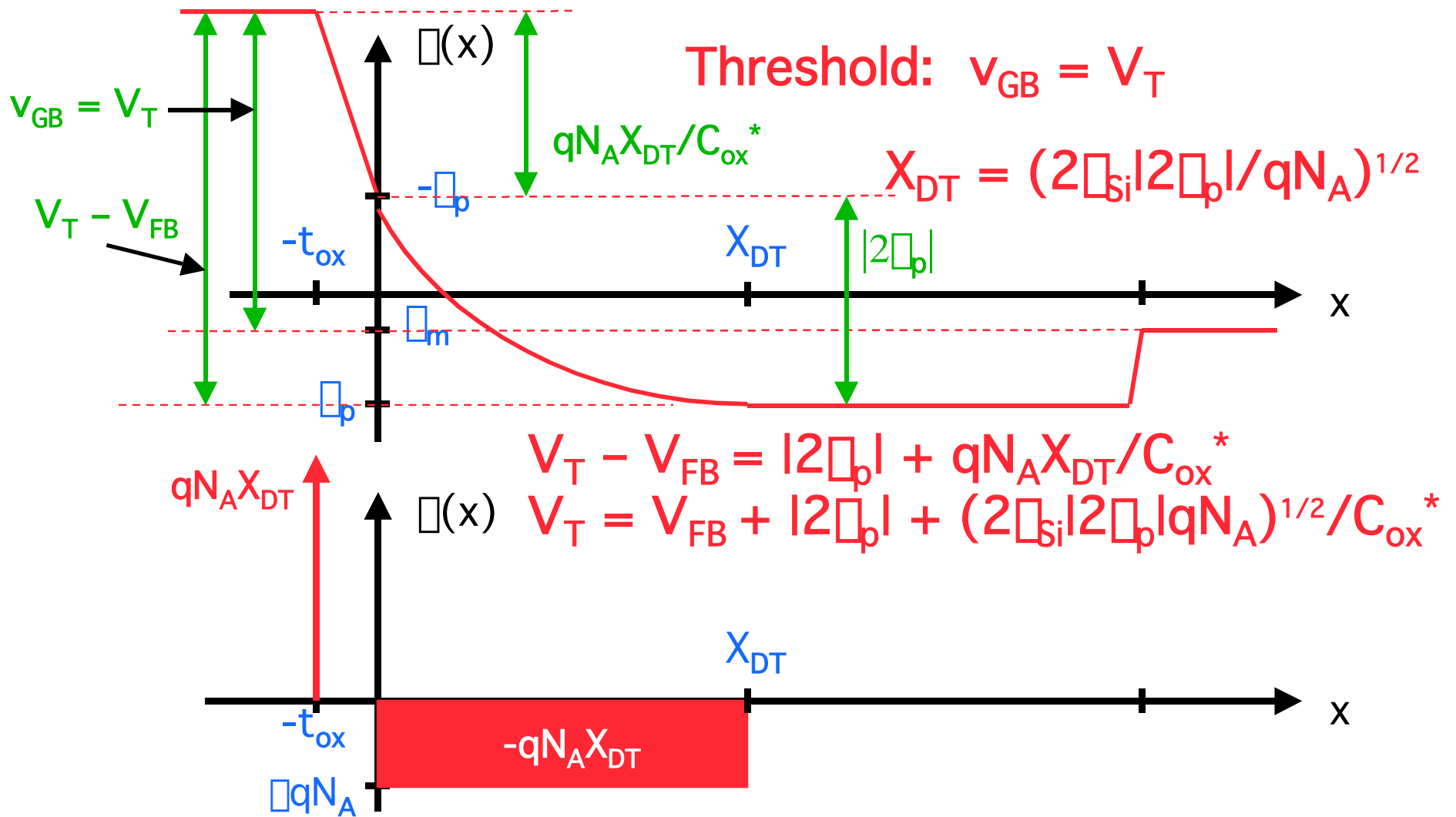
Electrostatic potential and net charge profiles



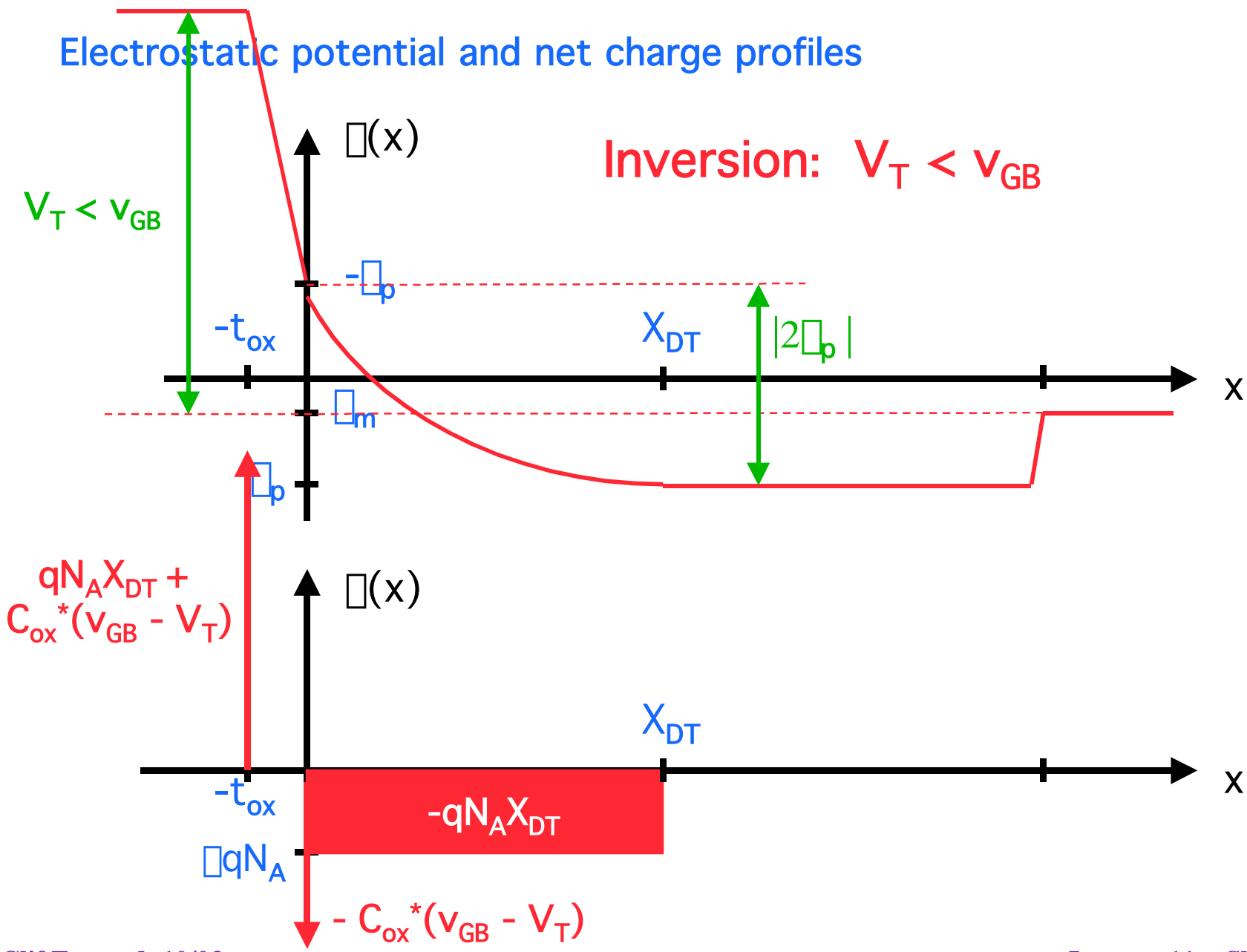
Electrostatic potential and net charge profiles



Electrostatic potential and net charge profiles

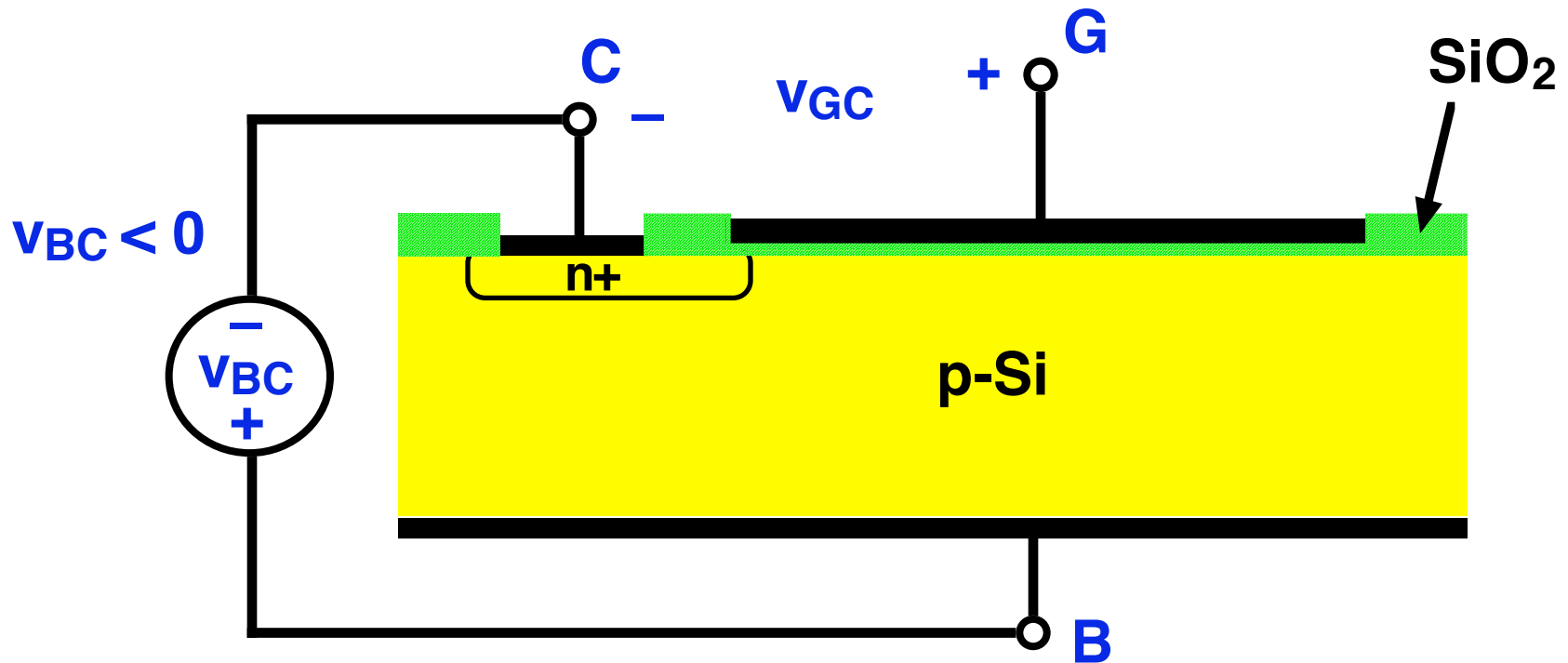


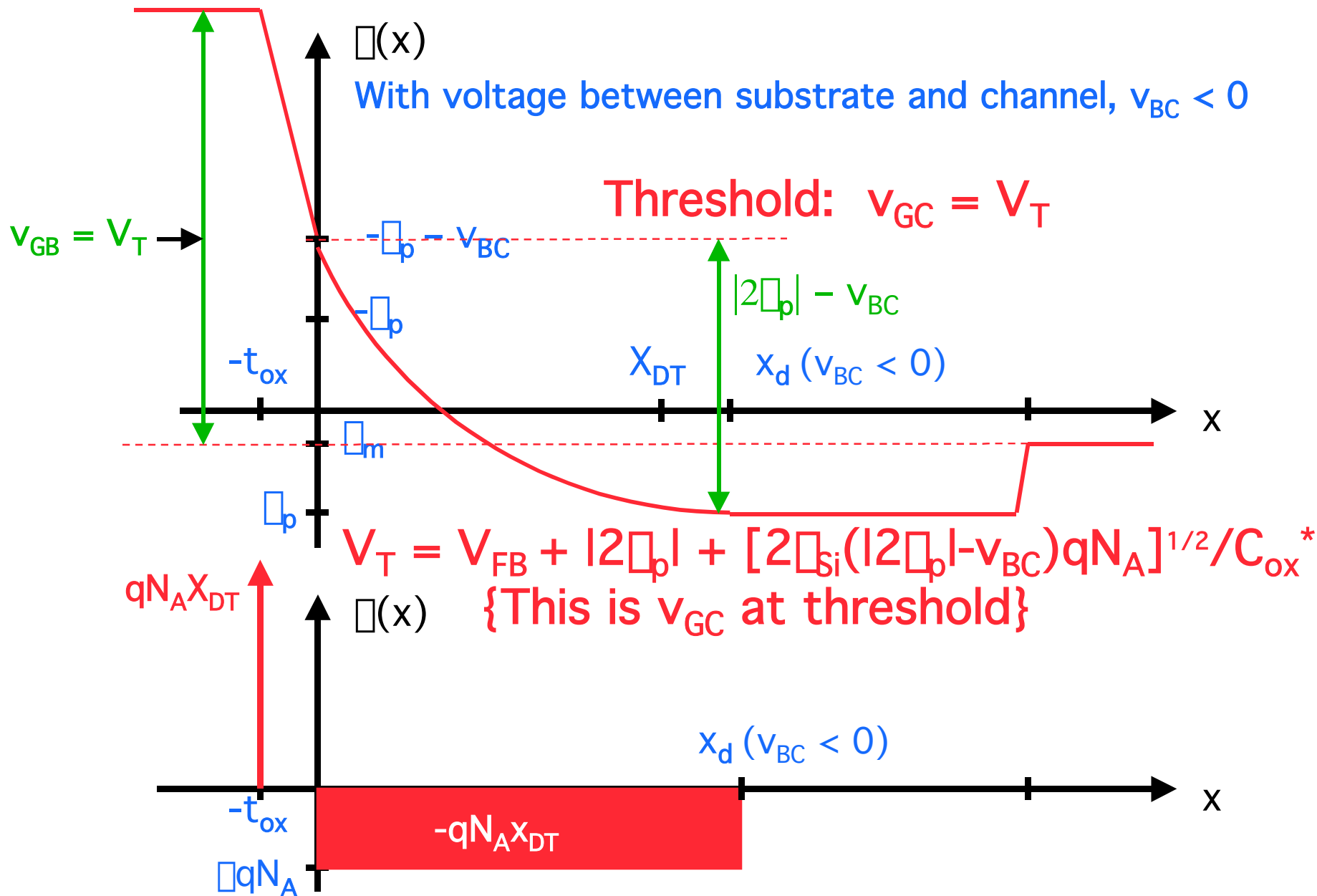
Electrostatic potential and net charge profiles



The n-MOS capacitor with bias on the substrate

Reverse bias applied to substrate, i.e. $v_{BC} < 0$





Lecture 11 - The MOS Capacitor - Summary

- **Qualitative description**

Three surface conditions: accumulated, depleted, inverted

Two key voltages: flat-band voltage, V_{FB} ; threshold voltage, V_T

The progression: accumulation through flat-band to depletion, then depletion through threshold to inversion

- **Quantitative modeling**

Apply depletion approximation to the MOS capacitor, $v_{BC} = 0$

Definitions: $V_{FB} \equiv v_{GB}$ such that $\psi(0) = \psi_{p-Si}$

$V_T \equiv v_{GB}$ such that $\psi(0) = -\psi_{p-Si}$

$C_{ox}^* \equiv \epsilon_{ox}/t_{ox}$

Results and expressions (For n-MOS example)

1. Flat-band voltage, $V_{FB} = \psi_{p-Si} - \psi_m$

2. Accumulation layer sheet charge density, $q_A^* = -C_{ox}^*(v_{GB} - V_{FB})$

3. Maximum depletion region width, $X_{DT} = [2\epsilon_{Si}|2\psi_{p-Si}|/qN_A]^{1/2}$

4. Threshold voltage, $V_T = V_{FB} - 2\psi_{p-Si} + [2\epsilon_{Si}qN_A|2\psi_{p-Si}|]^{1/2}/C_{ox}^*$

5. Inversion layer sheet charge density, $q_N^* = -C_{ox}^*(v_{GB} - V_T)$

- **MOS with bias applied to the adjacent n⁺-region**

Maximum depletion region width: $X_{DT} = [2\epsilon_{Si}(|2\psi_{p-Si}| - v_{BC})/qN_A]^{1/2}$

Threshold voltage: $V_T = V_{FB} - 2\psi_{p-Si} + [2\epsilon_{Si}qN_A(|2\psi_{p-Si}| - v_{BC})]^{1/2}/C_{ox}^*$

(v_{GC} at threshold)