

Lecture 13 - Large-Signal Models - Outline

- **Announcements**

Handout - Lecture Outline and Summary

- **Review**

MOSFET model: gradual channel approximation (Example: n-MOS)

$$i_D \approx \begin{cases} 0 & \text{for } (v_{GS} - V_T)/\beta \leq 0 \leq v_{DS} \quad \text{(cutoff)} \\ K (v_{GS} - V_T)^2 / 2\beta & \text{for } 0 \leq (v_{GS} - V_T)/\beta \leq v_{DS} \quad \text{(saturation)} \\ K (v_{GS} - V_T - \beta v_{DS}/2) v_{DS} & \text{for } 0 \leq v_{DS} \leq (v_{GS} - V_T)/\beta \quad \text{(linear)} \end{cases}$$

with $K \equiv (W/L)\mu_e C_{ox}^*$, $V_T = V_{FB} - 2\phi_{p-Si} + [2\phi_{Si} q N_A (|\phi_{p-Si}| - v_{BS})]^{1/2} / C_{ox}^*$
 and $\beta = 1 + [(\phi_{Si} q N_A / 2 (|\phi_{p-Si}| - v_{BS}))^{1/2} / C_{ox}^*]$ (frequently $\beta \approx 1$)

Comparison of MOSFET and BJT models and characteristics

- **Refined device models**

Charge stores:

1. Junction diodes
2. BJTs
3. MOSFETs

The Early Effect:

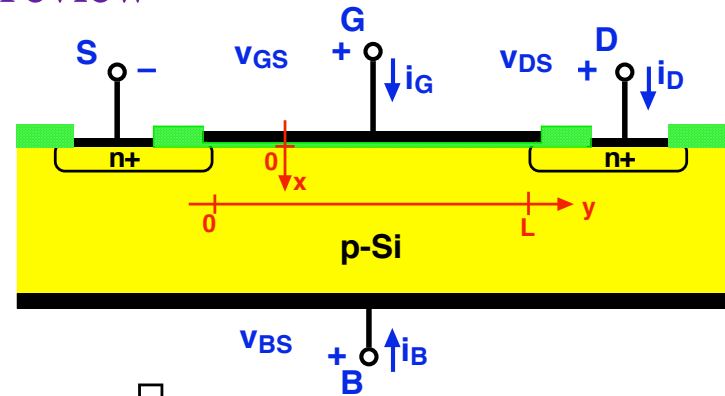
1. Base-width modulation in BJTs: $w_B(v_{CE})$
2. Channel-length modulation in MOSFETs: $L(v_{DS})$

Extrinsic parasitics: Lead resistances, capacitances, and inductances

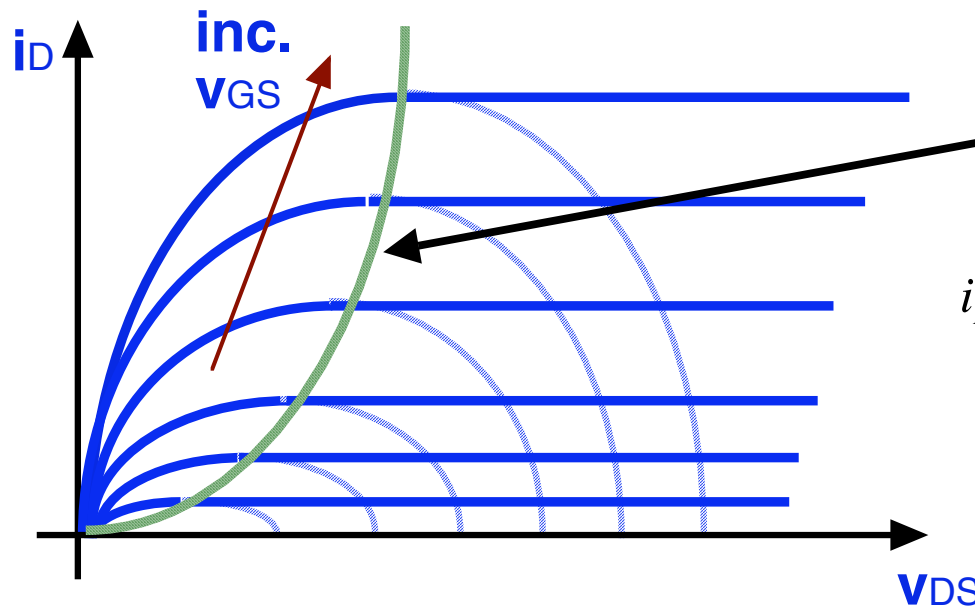
- The gradual channel approximation - review

Electrostatics problem in x-direction
to find $q_n^*(y)$ as a function of v_{GS} ,
 v_{BS} , and $v_{CS}(y)$

Drift problem in y-direction to relate
 i_D to v_{GS} , v_{DS} , and v_{BS}



$$i_D(v_{GS}, v_{DS}, v_{BS}) = \frac{W}{L} \mu_e C_{ox} \left[v_{GS} - V_T(v_{BS}) \right] \left[\frac{v_{DS}}{2} \right]_{v_{DS}}$$



When v_{DS} reaches $(v_{GS} - V_T)/\mu$,
the channel vanishes at $y = L$
and the current holds steady
at its saturation value.

$$i_D(v_{GS}, v_{DS}, v_{BS}) = \frac{1}{2} \frac{W}{L} \mu_e C_{ox} \{v_{GS} - V_T(v_{BS})\}^2$$

- The gradual channel approximation - review cont.

The full result is:

Valid for $v_{BS} \leq 0$, and $v_{DS} \geq 0$:

$$i_G(v_{GS}, v_{DS}, v_{BS}) = 0 \quad \text{and} \quad i_B(v_{GS}, v_{DS}, v_{BS}) = 0$$

$$i_D(v_{GS}, v_{DS}, v_{BS}) = \begin{cases} 0 & \text{for } \frac{1}{L} [v_{GS} - V_T(v_{BS})] < 0 < v_{DS} \\ \frac{1}{2} \frac{W}{L} \mu_e C_{ox}^* [v_{GS} - V_T(v_{BS})]^2 & \text{for } 0 < \frac{1}{L} [v_{GS} - V_T(v_{BS})] < v_{DS} \\ \frac{W}{L} \mu_e C_{ox}^* \left[\frac{1}{L} [v_{GS} - V_T(v_{BS})] - \frac{v_{DS}}{2} \right] v_{DS} & \text{for } 0 < v_{DS} < \frac{1}{L} [v_{GS} - V_T(v_{BS})] \end{cases}$$

with $C_{ox}^* \equiv \epsilon_{ox} / t_{ox}$

The threshold voltage is written several different ways (all equivalent, of course)

$$\begin{aligned} V_T(v_{BS}) &\equiv V_{FB} - 2\phi_{pSi} + \phi \left[2\phi_{pSi} | \phi v_{BS} \right]^{1/2} \quad \text{with } \phi \equiv \frac{1}{C_{ox}^*} [2\phi_{Si} q N_A]^{1/2} \\ &= V_{FB} - 2\phi_{pSi} + \phi \left[2\phi_{pSi} \right]^{1/2} + \phi \left\{ \left[2\phi_{pSi} | \phi v_{BS} \right]^{1/2} - \left[2\phi_{pSi} \right]^{1/2} \right\} \\ &= V_T(0) + \phi \left\{ \left[2\phi_{pSi} | \phi v_{BS} \right]^{1/2} - \left[2\phi_{pSi} \right]^{1/2} \right\} \quad \text{with } V_T(0) \equiv V_{FB} - 2\phi_{pSi} + \phi \left[2\phi_{pSi} \right]^{1/2} \end{aligned}$$

The factor ϕ is typically not included in the model because it is approximately 1 and contributes little to the accuracy or to our intuition and insight.

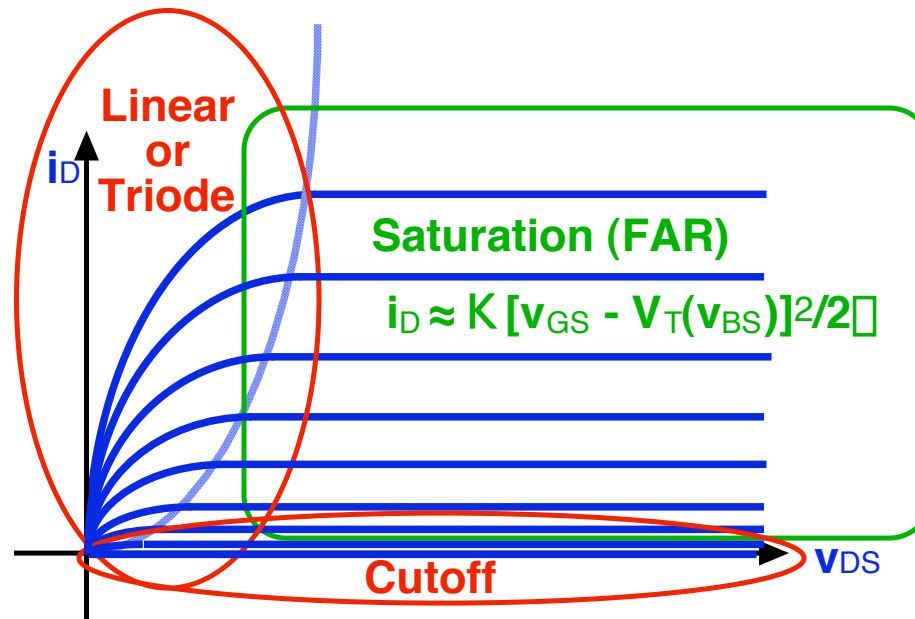
MOSFET Characteristics (n-channel)

Also:

$$i_G \approx 0$$

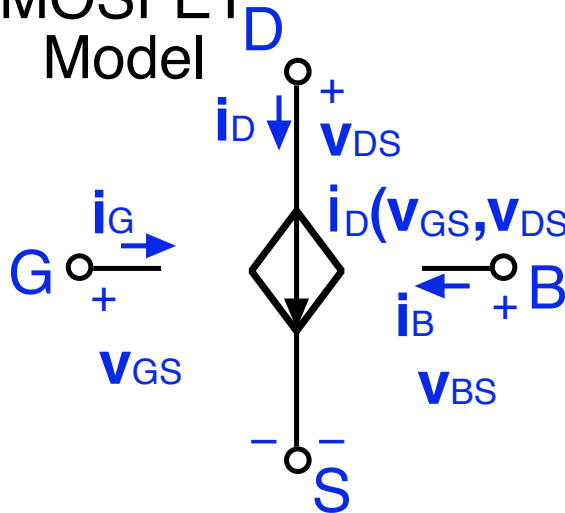
$$i_B \approx 0$$

$$K = (W/L)\mu_e C_{ox}^*$$



Output family

MOSFET Model

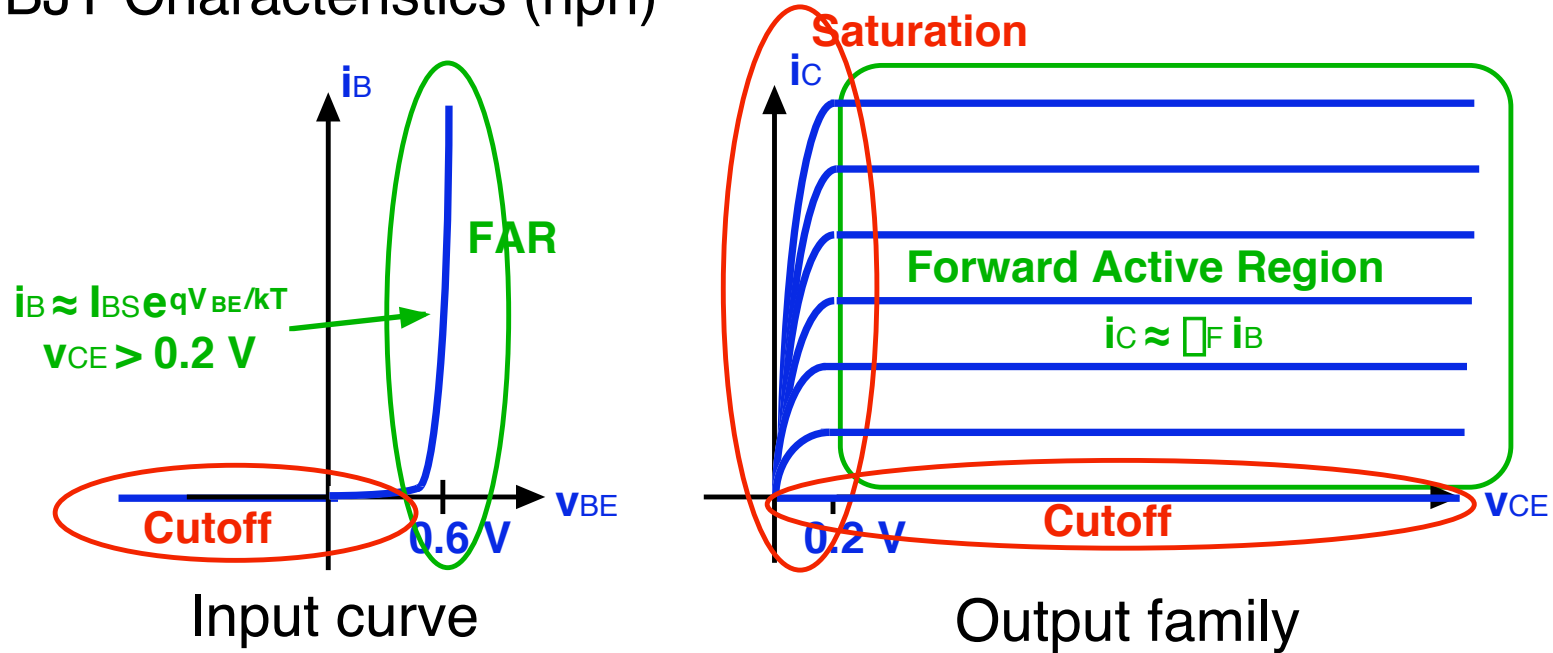


Model valid for $v_{BS} \leq 0$ and $v_{DS} \geq 0$, insuring $i_G(v_{GS}, v_{DS}, v_{BS}) \approx 0$, $i_B(v_{GS}, v_{DS}, v_{BS}) \approx 0$

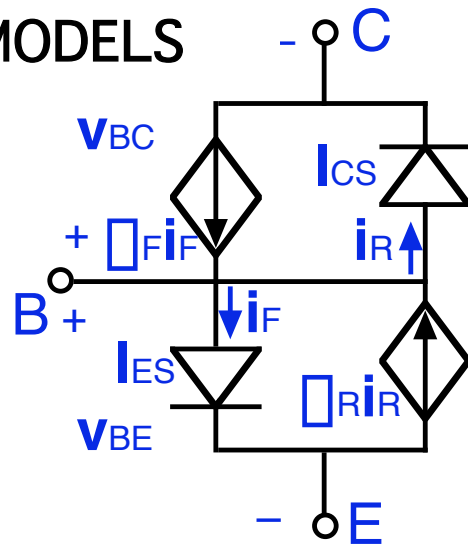
$$i_D(v_{GS}, v_{DS}, v_{BS}) \approx \begin{cases} 0 & \text{for } (v_{GS} - V_T)/\gamma \leq 0 \leq v_{DS} \quad (\text{cutoff}) \\ (W/L)\mu_e C_{ox}^* (v_{GS} - V_T)^2 / 2\gamma & \text{for } 0 \leq (v_{GS} - V_T)/\gamma \leq v_{DS} \quad (\text{saturation}) \\ (W/L)\mu_e C_{ox}^* (v_{GS} - V_T - \gamma v_{DS}/2)v_{DS} & \text{for } 0 \leq v_{DS} \leq (v_{GS} - V_T)/\gamma \quad (\text{linear}) \end{cases}$$

with $V_T = V_{FB} - 2\phi_{p-Si} + [2\phi_{Si} q N_A (2\phi_{p-Si} - v_{BS})]^{1/2} / C_{ox}^*$
 $\gamma = 1 + [(\phi_{Si} q N_A / 2 (2\phi_{p-Si} - v_{BS}))^{1/2} / C_{ox}^*]$ (frequently ≈ 1)

BJT Characteristics (npn)



BJT MODELS

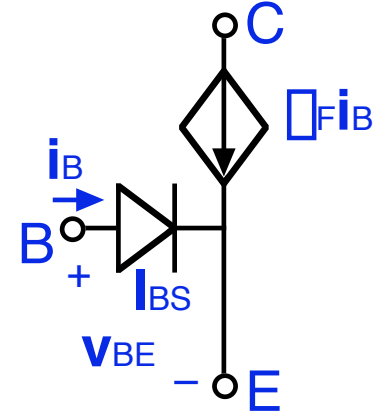


Forward active region

$V_{BE} > 0.6 \text{ V}$
 $V_{CE} > 0.2 \text{ V}$
 (i.e. $V_{BC} < 0.4 \text{ V}$)
 i_R is negligible

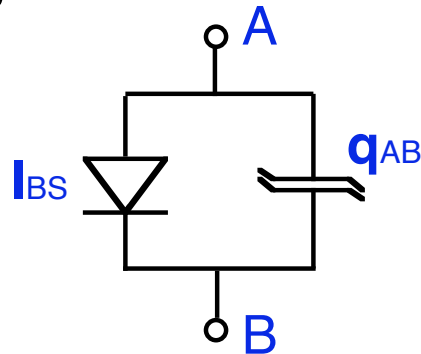
Other regions

Cutoff:
 $V_{BE} < 0.6 \text{ V}$
Saturation:
 $V_{CE} < 0.2 \text{ V}$



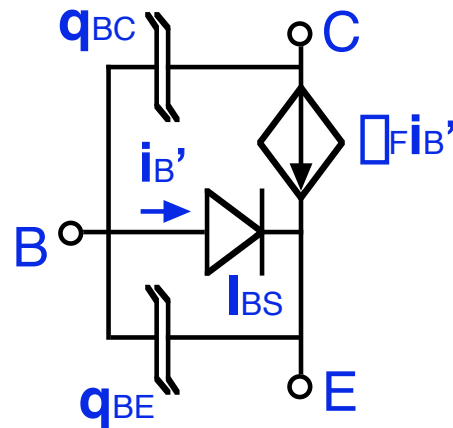
Adding charge stores to the large signal models:

p-n diode:



q_{AB} : Excess carriers on p-side plus excess carriers on p-side plus junction depletion charge.

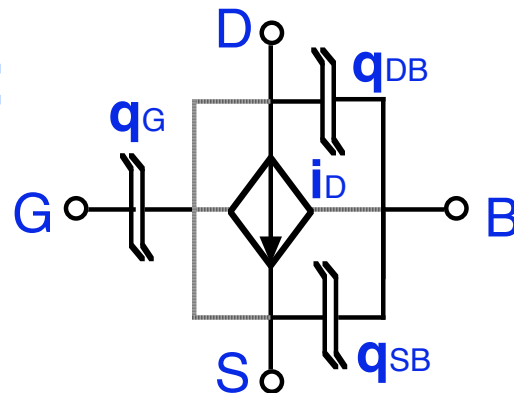
BJT: npn
(in F.A.R.)



q_{BE} : Excess carriers in base plus E-B junction depletion charge

q_{BC} : C-B junction depletion charge

MOSFET:
n-channel



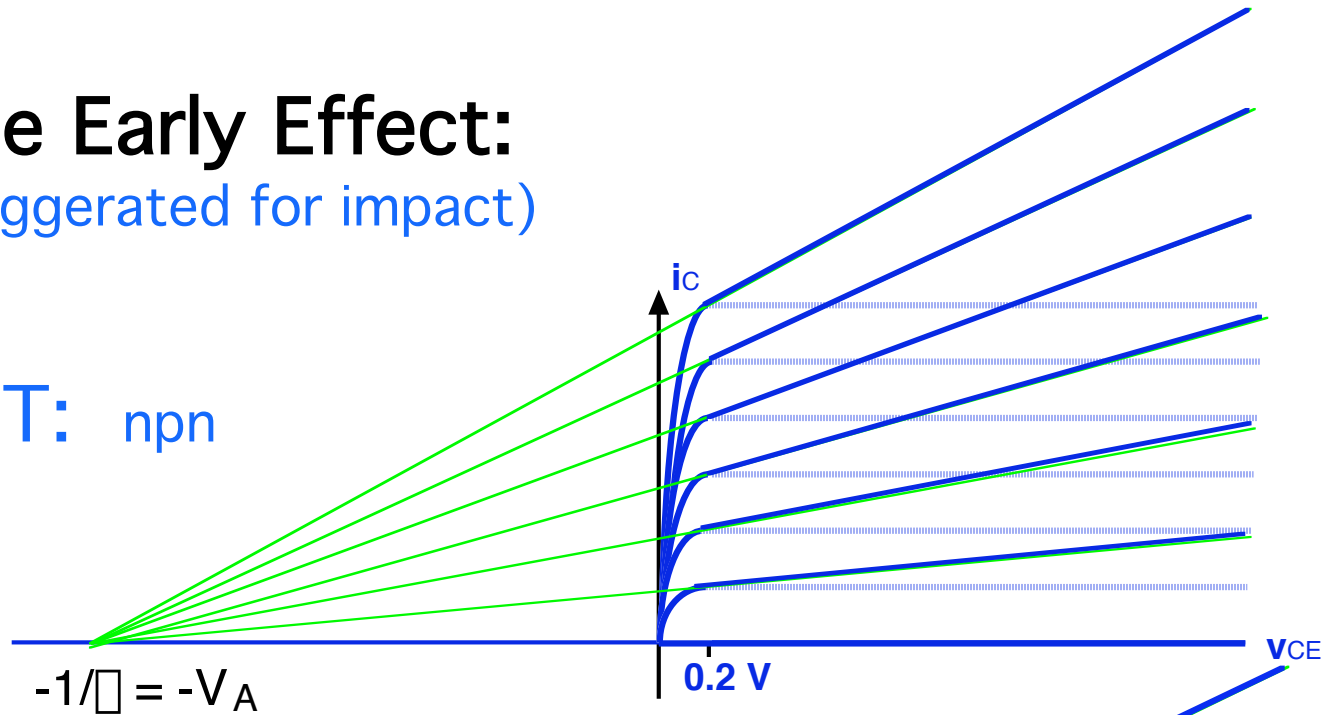
q_G : Gate charge; a function of v_{GS} , v_{DS} , and v_{BS} .

q_{DB} : D-B junction depletion charge

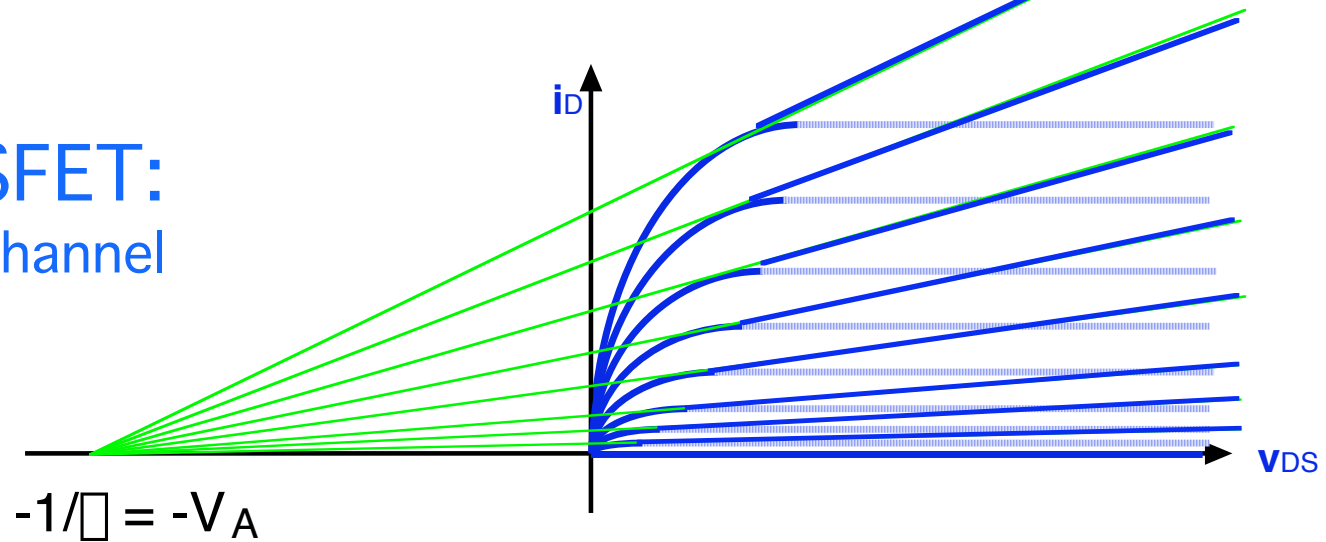
q_{SB} : S-B junction depletion charge

The Early Effect: (exaggerated for impact)

BJT: npn



MOSFET:
n-channel



Active Length Modulation - the Early Effect: MOSFET

MOSFET:

We begin by recognizing that the channel length decreases with increasing v_{DS} and writing this dependence to first order in v_{DS} :

$$L \approx L_0(1 - \alpha v_{DS}) \text{ and } 1/L \approx (1 + \alpha v_{DS})/L_0$$

$$K = (W/L) \mu_e C_{ox}^*$$

Inserting the channel length variation with v_{DS} into K we have:

$$K \approx K_0 (1 + \alpha v_{DS}) \text{ where } K \equiv (W/L_0) \mu_e C_{ox}^*$$

Thus, in saturation:

$$i_D \approx K_0 (v_{GS} - V_T)^2 (1 + \alpha v_{DS})/2 \square$$

Active Length Modulation - the Early Effect: **BJT**

BJT:

We begin by recognizing that the base width decreases with increasing v_{CE} and writing this dependence to first order in v_{CE} :

$$w_B^* \approx w_{B0}^*(1 - \alpha v_{CE}) \text{ and } 1/w_B^* \approx (1 + \alpha v_{CE})/w_{B0}^*$$

Then we note that in a modern BJT the emitter defect is the more important factor:

$$\alpha_F = (1 - \alpha_B)/(\alpha_E + \alpha_B) \approx 1/\alpha_E = (D_e/D_h)(N_{DE}/N_{AB})(w_E^*/w_B^*)$$

Inserting the base width variation with v_{CE} into α_F we have:

$$\alpha_F \approx \alpha_{F0}(1 + \alpha v_{CE})$$

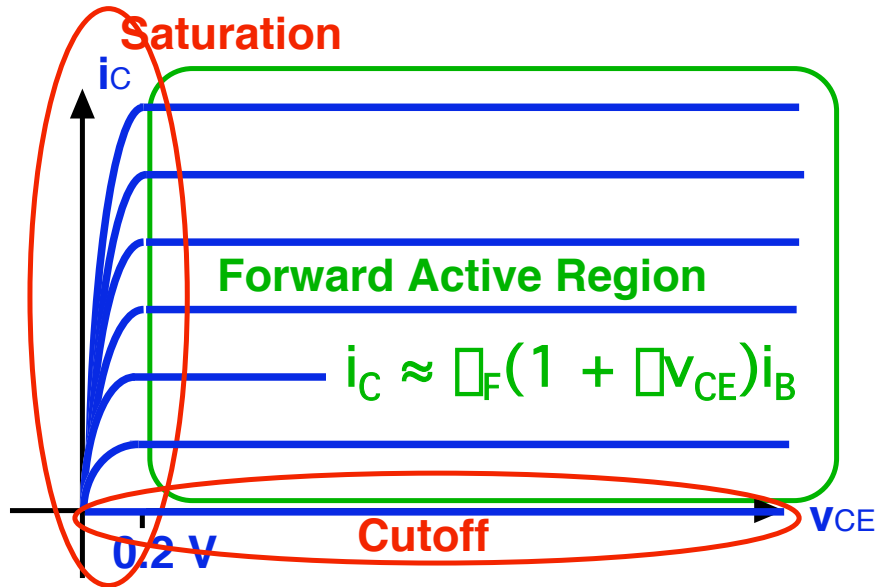
where $\alpha_{F0} \equiv (D_e/D_h)(N_{DE}/N_{AB})(w_E^*/w_{B0}^*)$

Thus, in the F.A.R.:

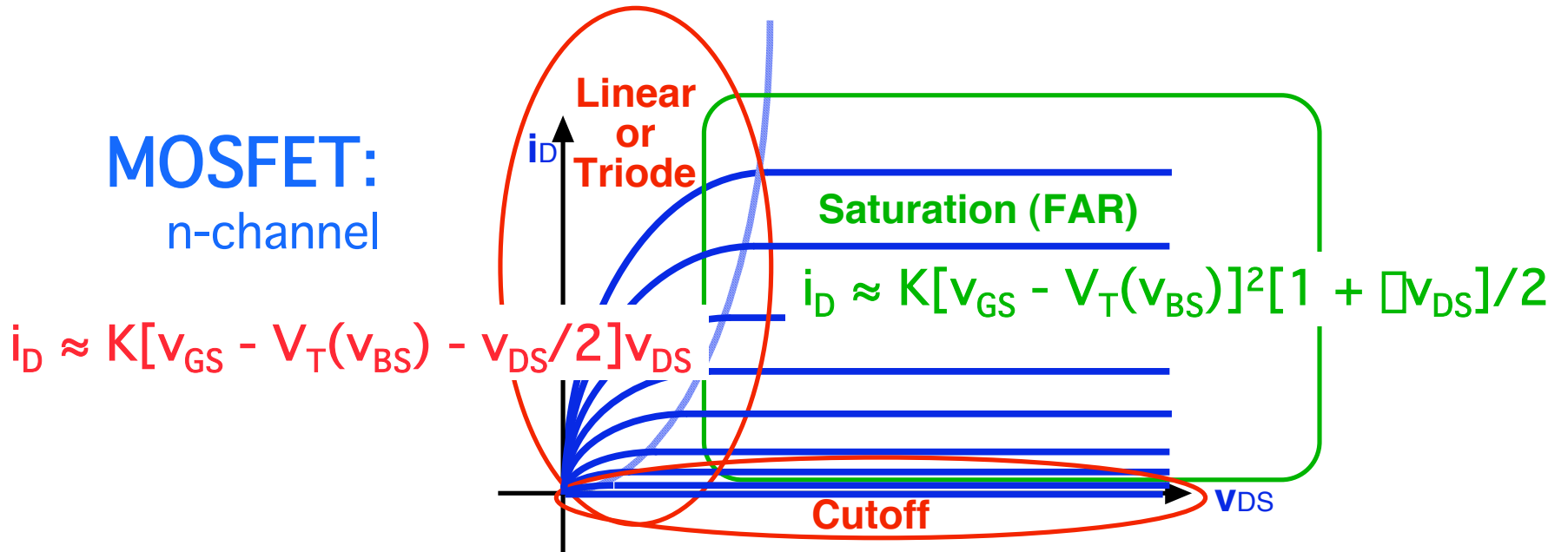
$$i_C \approx \alpha_{F0}(1 + \alpha v_{CE})i_B$$

Output Characteristics

BJT: npn



MOSFET:
n-channel



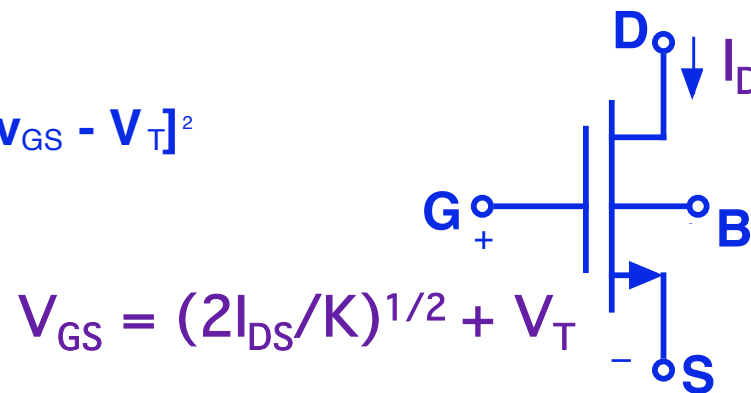
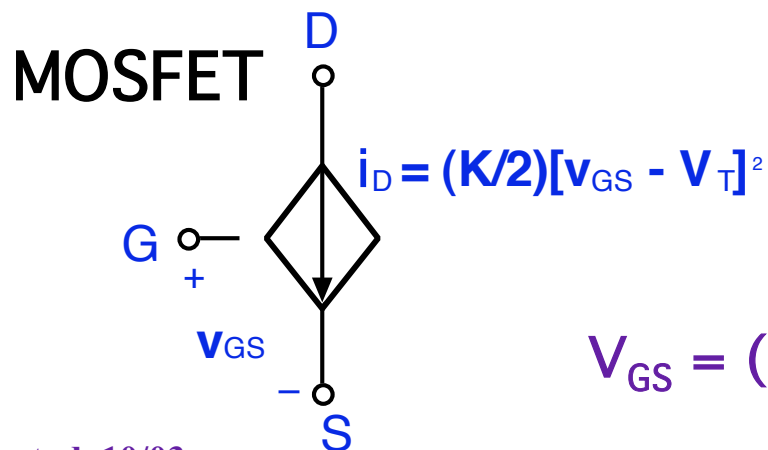
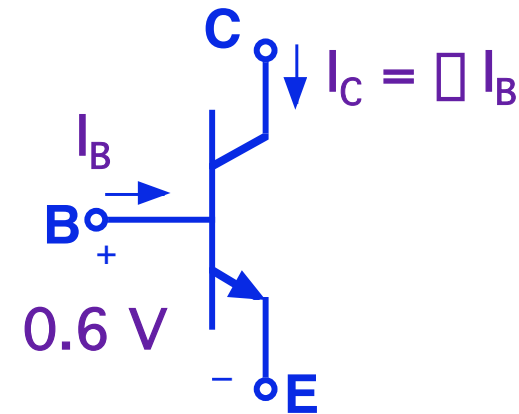
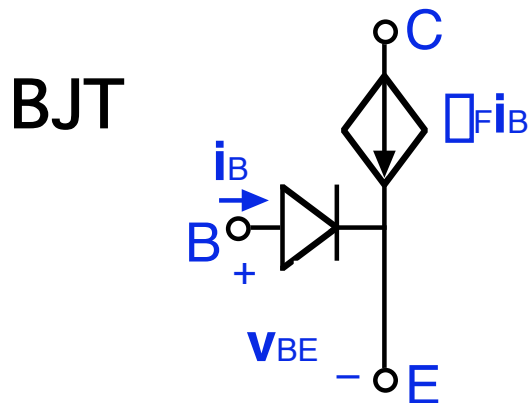
Large signal models: when will we use them?

Digital circuit analysis/design:

This requires use of the entire circuit, and will be the topic of the two lectures after the next (15 and 16).

Bias point analysis/design:

This uses the FAR models (lec. 17ff).



Lecture 13 - Large-Signal Models - Summary

- **Refined device models**

Charge stores:

1. Junction diodes - depletion and diffusion charge
2. BJTs - at EB junction: depletion and diffusion charge
at CB junction: depletion charge (focus on FAR)
3. MOSFETs - between B and S, D: depletion charge of n⁺-p junctions
between G and S, D, B: gate charge (the dominant store)
in cut-off: $C_{gs} \approx C_{gd} \approx 0$; all is C_{gb}
linear region: $C_{gs} = C_{gd} = W L C_{ox}^*/2$
in saturation region: $C_{gs} = (2/3) W L C_{ox}^*$
 $C_{gd} = 0$ (only parasitic overlap)

The Early Effect:

1. Base-width modulation in BJTs: $w_B(v_{CE})$
In the F.A.R.: $i_C \approx \beta_{F0}(1 + \beta_{V_{CE}})i_B$
2. Channel-length modulation in MOSFETs: $L(v_{DS})$
In saturation: $i_D \approx K_o (v_{GS} - V_T)^2 (1 + \beta_{V_{DS}})/2$

Extrinsic parasitics: Lead resistances, capacitances, and inductances