

## Lecture 26 - The Current State-of-the-Art - Outline

- **Announcements**

**Handouts - Lecture Outline and Summary, Life after 6.012**

**Final - Monday, Dec. 15, 9:00 am to 12 noon, duPont Gymnasium**

**Covering all the course; closed book; 4-5 excellent problems**

- **Review - Device transit times and quasi-statics**

**Device transit times and the quasi-static assumption: □**

$$\text{BJT: } \tau_B = q n'(x) / J_e = w_B^2 / 2D_e = w_B^2 / 2\mu_e V_{\text{Thermal}} \square$$

$$\text{MOSFET: } \tau_C = L / \mu_e E = L^2 / \mu_e (V_{GS} - V_T) \square$$

**Velocity saturation:  $\tau_B = w_B / s_{\text{sat}}$ ,  $\tau_C = L / s_{\text{sat}}$  (now only linear in dimension)**

- **Review - CMOS scaling**

- **The current state-of-the-art □**

**$f_T$ 's □**

**Scaling and microprocessor generations □**

- **Life after 6.012**

**Is there any? (or: "Where does one head after taking the header?")**

## Overview of CMOS Scaling □

- CMOS gate delay and power

Three key performance metrics: (We want to reduce them all.)

$$\text{Gate Delay} = 12 n L_{\min}^2 V_{DD} / \mu_n (V_{DD} - V_T)^2 \square$$

$$P_{\text{ave}} @ \text{max. f} \mu C_L V_{DD}^2 / \text{GD} = (W_n / L_{\min}) \mu_n C_{\text{ox}}^* V_{DD} (V_{DD} - V_T)^2 / 4 \square$$

$$P_{\text{density, max}} \mu P_{\text{ave, max}} / W_n L_{\min} = \mu_n \mu_{\text{ox}} V_{DD} (V_{DD} - V_T)^2 / 4 t_{\text{ox}} L_{\min}^2$$

- CMOS scaling rule

Scale all dimensions and all voltages by 1/s

- Results of scaling:

Reducing  $L_{\min}$ ,  $W$ ,  $t_{\text{ox}}$ ,  $V_{DD}$ , and  $V_T$  by 1/s

Results in: Density: increases by  $s^2$

$K$ : increases by  $s$

$C_{\text{ox}}^*$ : increases by  $s$

Gate delay,  $\square$  decreases by 1/s

$P_{\text{ave}}$ : decreases by 1/s<sup>2</sup>

$P_{\text{density}}$ : is unchanged

- Velocity saturation □

As  $L$  gets smaller, the fields may get bigger.

(...unless we scale perfectly)

When  $s \triangleright s_{\text{sat}}$ , then what?

# CMOS Scaling with velocity saturation

- CMOS characteristics, gate delay, and power w. vel. sat.:

**In saturation:**

$$i_D = \text{Channel charge} \times s_{sat}$$

$$= W C_{ox}^* [v_{GS} - V_T] s_{sat} = W C_{ox}^* [V_{DD} - V_T] s_{sat}$$

The performance metrics now turn out to be:

$$\tau_{Min.Cycle} \propto \frac{n L_{min} V_{DD}}{[V_{DD} - V_{Tn}] s_{sat}} \quad (\text{Now only decreases linearly with } L_{min}.)$$

$$P_{ave@Max.f} = C_L V_{DD}^2 f_{max} \propto \frac{W_{min} L_{min} C_{ox}^* V_{DD}^2}{\tau_{Min.Cycle}} \propto W_{min} s_{sat} \frac{\tau_{ox}}{V_{DD}} [V_{DD} - V_{Tn}]$$

$$PD_{ave@Max.f} = \frac{P_{ave@Max.f}}{\text{Inverter area}} \propto \frac{P_{ave@Max.f}}{W_{min} L_{min}} = \frac{s_{sat} \tau_{ox} V_{DD} [V_{DD} - V_{Tn}]}{\tau_{ox} L_{min}}$$

- CMOS scaling results w. velocity saturation:

<b>Scaling as:</b>	$L_{min} \propto L_{min} / s$	<b>Results in:</b>	$K \propto sK$
	$W_{min} \propto W_{min} / s$		$C_{ox}^* \propto sC_{ox}^*$
	$t_{ox} \propto t_{ox} / s$		$\tau_{Min.cycle} \propto \tau_{Min.cycle} / s$
	$V_{DD} \propto V_{DD} / s$		$P_{ave} \propto P_{ave} / s^2$
	$V_T \propto V_T / s$		$PD_{ave} \propto PD_{ave}$

These results are identical to what we had earlier.  
Scaling still works!

## An historical scaling example - Inside Intel □

<u>Parameter</u>	<u>386</u>	<u>486</u>	<u>Pentium</u>
Scaling factor, s	1	2	3
$L_{\min}$ ( $\mu\text{m}$ )	1.5	0.75	0.5
$W_n$ ( $\mu\text{m}$ )	10	5	3
$t_{\text{ox}}$ (nm)	30	15	9
$V_{\text{DD}}$ (V)	5	3.3	2.2
$V_T$ (V)	1	-	-
Fan out	3	3	3
$K$ ( $\mu\text{A}/\text{V}^2$ )	230	450	600
GD (ps)	840	400	250
$f_{\text{max}}$ (MHz)	29	50	100
$P_{\text{ave}}/\text{gate}$ (mW)	92	23	10
Density (kgates/cm <sup>2</sup> @ 20W/cm <sup>2</sup> max.)	220	880	2,000

Sources: Prof. Jesus del Alamo and Intel

## An second look inside Intel - a slightly different perspective □

<u>Parameter</u>	<u>486</u>	<u>Pentium generations</u>		
Scaling factor, s	-	1	1.6	2.3
$L_{\min}$ ( $\mu\text{m}$ )	1.0	0.8	0.5	0.35
SRAM cell area ( $\mu\text{m}^2$ )	-	111	44	21
Die size ( $\text{mm}^2$ )	170	295	163	91
$f_{\text{mzx}}$ (MHz)	38	66	100	200
$t_{\text{ox}}$ (nm)	20	10	8	6
Metal layers	2	3	4	4
Planarization	SOG	CMP	CMP	CMP
Poly type	n	n,p	n,p	n,p
Transistors	CMOS	BiCMOS	BiCMOS	BiCMOS

Source: Dr. Leon D. Yau, Intel, 10/8/96

For the very latest see the International Technology Roadmap for Semiconductors at <http://public.itrs.net> (click on "2002 Update", then on "ORTC")

## Trends:

The evolution of  
transistor  
technology and □  
Moore's Law - □  
transistor density □  
doubles every 1.5 □  
to 2 years. □

## LED Technology

### *Haitz's Law for LED Flux*

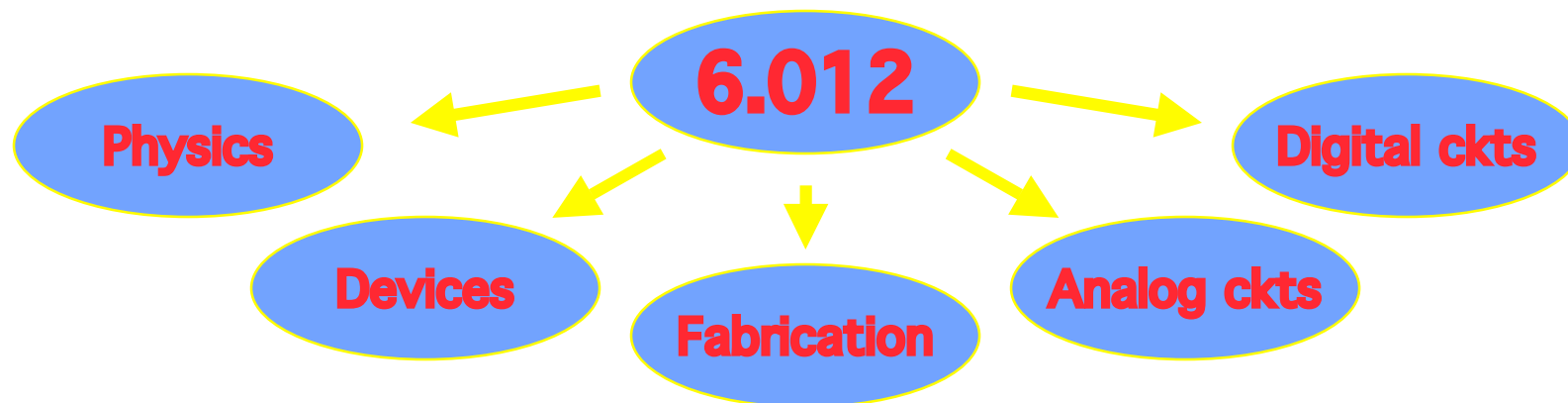
- LED Flux per package has doubled every 18-24 months for 30+ Years!!
- 1965 Moore's Law "# of Transistors/chip will double every 18-24 months!"

## High Power White LEDs

### *Lumileds 100 lumen Club!*

- These are the only LEDs that approach “Illumination” flux!
- A 15W Incandescent bulb is **ONLY** ~110lm of undirected white light!

## Life after 6.012 - "I've taken the header, so...where can I head?" □



- **Physics**

<u>6.728:</u> Applied quantum and statistical physics	H	G(F)
6.730: Physics for solid-state applications	H	G(S)
6.732: Physics of solids	H	G(F)
6.763: Applied superconductivity	H	G(F*)

- **Devices**

<u>6.720J:</u> Integrated microelectronic devices	H	G(F)
6.772: Compound semiconductor devices	H	G(S*)
6.777: Design and fabrication of microelectromechanical devices	H	G(S)

## Life after 6.012 - continued

- **Processing**

<u>6.152J</u> : Microelectronics processing technology		U(F,S)□
6.151: Microelectronics processing laboratory		U(S)□
6.773: Physics of fabrication: back-end processing	H	G(F*)□
6.774: Physics of fabrication: front-end processing	H	G(F*)□
6.778J: Materials and processes for MEMS	H	G(S)□
6.780: Semiconductor manufacturing	H	G(S*)□
6.781: Submicrometer and nanometer technology	H	G(S)□

- **Analog circuits**□

6.301: Solid-state circuits		G(S)□
6.302: Feedback systems		U(F)□
6.331: Advanced circuit techniques	H	G(S)□
6.334: Power electronics	H	G(S)□
6.376: Low Power Analog VLSI	H	G(F)□
<u>6.775</u> : Design of analog MOS LSI	H	G(F)□

- **Digital circuits**

<u>6.371</u> : Introduction to VLSI Systems	H	G(F*)□
6.374: Analysis and design of digital ICs	H	G(F)□

## Lecture 26 - The Current State-of-the-Art - Summary

- **The current state-of-the-art**

**Very small and blazingly fast**

**(and getting smaller and going faster every day)**

$L_{\min} = 1.0 \mu\text{m}$

▶  $0.75 \mu\text{m}$

▶  $0.5 \mu\text{m}$

▶  $0.35 \mu\text{m}$

▶  $0.25 \mu\text{m}$

▶  $0.18 \mu\text{m}$

▶  $0.13 \mu\text{m}$

▶  $0.10 \mu\text{m}$

▶  $0.08 \mu\text{m}$

▶  $0.05 \mu\text{m}$

▶  $0.035 \mu\text{m}$

▶  $0.025 \mu\text{m}$

**We're in this region now.**

- **Life after 6.012**

**Yes, Virginia, there is life after 6.012.**

▶ Physics

▶ Devices

▶ Processing

▶ Analog circuits

▶ Digital circuits