

YOUR NAME _____

*Department of Electrical Engineering and Computer Science
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6.012 Electronic Devices and Circuits

Exam No. 2

Notes:

1. Unless otherwise indicated, assume room temperature and that kT/q is 0.025 V. You may also approximate $[(kT/q) \ln 10]$ as 0.06 V.
2. Open book; 6.012 text and any other notes permitted.
3. All of your answers and any relevant work must appear on these pages. Any additional paper you hand in will not be graded.
4. Make reasonable approximations and assumptions. State and justify any such assumptions and approximations you do make.
5. Be careful to include the correct units with your answers when appropriate.
6. Be certain that you have all nine (9) pages of this exam booklet and make certain that you write your name at the top of this page in the space provided.

6.012 Staff Use Only	PROBLEM 1 _____	(36 maxium)
	PROBLEM 2 _____	(28 maxium)
	PROBLEM 3 _____	(36 maxium)
	TOTAL	(100 maxium)

Problem 1 continued

c) Now consider illuminating this diode with a narrow strip of light generating 10^{16} hole-electron pairs/cm²-s uniformly in the plane at $x = X$; the generation function, $g_L(x)$, can be modeled as a delta function at $x = X$, i.e., $g_L(x) = M \delta(x-X)$, with $M = 10^{16}$ cm⁻²-s⁻¹.

(i) With the diode terminals shorted together, i.e., $v_{AB} = 0$, what will be the approximate diode current, i_D , for each of the following values of X ? Either explain your answer if you can answer by inspection, or show your work; answers stated with no indication of where they came from will not receive credit. You may neglect the width of the depletion region on the p-side of the junction.

(A) $X = 0$

i_D _____

(B) $X = -2.5 \mu\text{m}$

i_D _____

(C) $X = 20 \mu\text{m}$

i_D _____

(D) $X = -1 \mu\text{m}$

i_D _____

(ii) With the diode illuminated at $x = -2.5 \mu\text{m}$ as in Part (c-i-B) above, but with the terminals open circuited, i.e., $i_D = 0$, answer the following questions concerning the terminal voltage, v_{AB} :

(A) Is the terminal voltage positive or negative, and why?

_____ $v_{AB} > 0$, _____ $v_{AB} < 0$, because:

Problem 1 continues on the next page

Problem 1 continued

(B) What is the terminal voltage? If you could not answer Part (c-i-B) above, assume that the answer there was I_D , and give your answer to this question in terms of I_D .

$$V_{AB} = \underline{\hspace{2cm}}$$

(iii) Consider the diode illuminated at the mid-point of the junction, i.e., $X = 0$. If a resistor is connected across the terminals, it will be heated because the fraction of the optical energy converted to electrical energy by the diode (acting as a solar cell) will be in turn converted to thermal energy (i.e., dissipated) in the resistor.

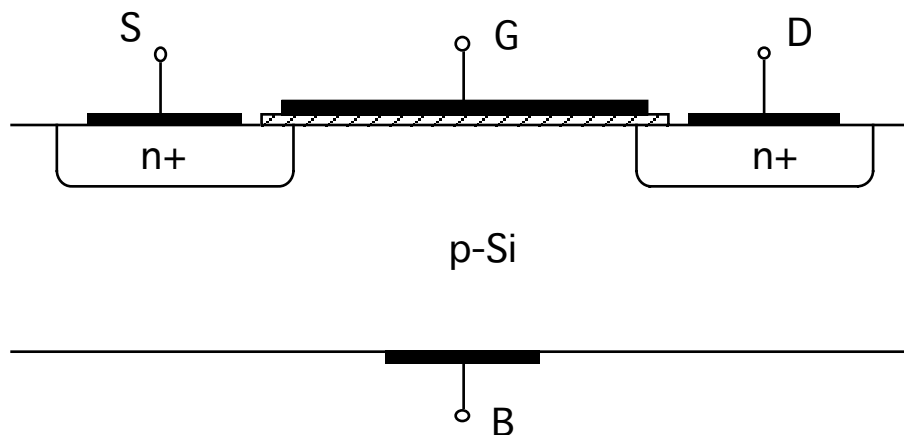
(A) What happens to this optical energy (i.e., the fraction converted to electrical energy) if the diode terminals are not connected to a resistor but rather are left open circuited?

(B) What happens to this optical energy if the diode terminals are short circuited?

End of Problem 1

Problem 2 (28 points)

The MOS capacitor in the gate of the n-channel silicon MOSFET illustrated below is ideal with no net charge in the oxide and a negligible density of interface states. The flatband voltage, V_{FB} , of this MOS capacitor is -0.5 V and the threshold voltage, V_T , (with $V_{BS} = 0$ V) is $+1.0$ V. The width of the gate is 100 μm and the gate length is 10 μm ; the thickness of the gate oxide, t_o , is 50 nm (5×10^{-6} cm); the mobility of electronics in the channel (in inversion) is 1000 $\text{cm}^2/\text{V}\cdot\text{s}$.



- (a) If this device is biased in saturation with the gate-to-source voltage, V_{GS} , equal to $+2.0$ V, and the substrate-to-source voltage, V_{BS} , equal to zero, what is the drain current, i_D ?

$$i_D = \underline{\hspace{2cm}}$$

- (b) This MOSFET is biased with $V_{GS} = -1$ V, and $V_{BS} = 0$ V.

- (i) What is the condition of the semiconductor surface at the oxide-silicon interface with this bias applied? Explain your answer.

accumulated depleted inverted
because

- (ii) What is the incremental capacitance that would be measured on the capacitor, e.g., between the gate and substrate terminals, with this bias applied? Take 3.5×10^{-13} coul/V-cm (or F/cm) as the dielectric constant of the oxide.

$$C_{gs} = \underline{\hspace{2cm}}$$

Problem 2 continues on the next page

Problem 2 continued

(c) The manufacturer of this MOSFET is having difficulty controlling the oxide thickness, t_o . In one process run, for example, t_o turned out to be 60 nm, rather than 50 nm. Which of the following quantities will be different for transistors from this run, and how will they compare to the same parameters for the devices with $t_o = 50$ nm?

(i) The flatband voltage, V_{FB} :

V_{FB} ($t_o = 60$ nm) is [greater than, less than, equal to] (circle one) V_{FB} ($t_o = 50$ nm),
because:

(ii) The threshold voltage, V_T :

V_T ($t_o = 60$ nm) is [greater than, less than, equal to] (circle one) V_T ($t_o = 50$ nm),
because:

(iii) The incremental transconductance, g_m , at a bias point in saturation with $I_D = 10 \mu\text{A}$.

g_m ($t_o = 60$ nm) is [greater than, less than, equal to] (circle one) g_m ($t_o = 50$ nm),
because:

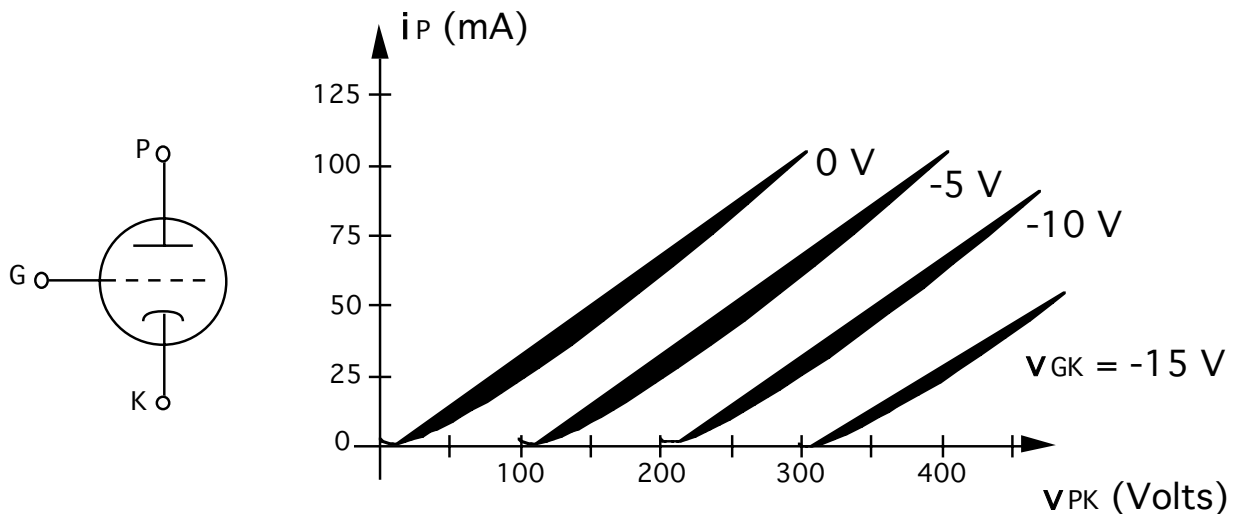
(iv) The incremental gate-to-source capacitance, C_{gs} , for a bias point in saturation.

C_{gs} ($t_o = 60$ nm) is [greater than, less than, equal to] (circle one) C_{gs} ($t_o = 50$ nm),
because:

End of Problem 2

Problem 3 (36 points)

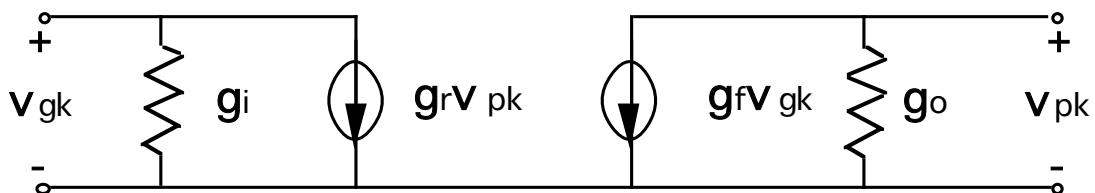
Several three-terminal devices (e.g., vacuum tube triodes, static induction transistors, field-emitter display pixels) have characteristics like those illustrated below;



$$i_G = I_G(e^{qV_{GK}/kT} - 1)$$

$$i_P = G (M v_{PK} + v_{GK})^{3/2} \quad \text{with } G = 2 \text{ mA/V}^{3/2}, M = 0.05, \text{ and } I_G = 10^{-6} \text{ A.}$$

(a) An incremental model for a device with these characteristics is illustrated below. Write mathematical expressions for each of the parameters in the incremental model and evaluate them at the bias point, Q, such that $V_{GK} = -4 \text{ V}$, and $V_{PK} = 160 \text{ V}$.

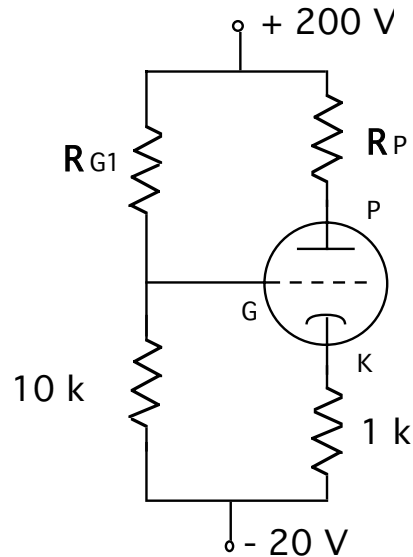


	Expression	Value at Q
$g_i =$	_____	= _____
$g_r =$	_____	= _____
$g_f =$	_____	= _____
$g_o =$	_____	= _____

Problem 3 continues on the next page

Problem 3 continued

- (b) This device is biased using the resistor biasing circuit illustrated below:



- (i) Select R_{G1} and R_P to achieve the bias point specified in Part (a), i.e., $V_{GK} = -4.0$ V and $V_{PK} = 160$ V.

$$R_{G1} = \underline{\hspace{2cm}}$$

$$R_P = \underline{\hspace{2cm}}$$

- (ii) Use up to three capacitors to couple a voltage source, v_{in} , and a load resistor, R_L , to the circuit illustrated above, and to create a common-cathode amplifier (the cathode is the terminal labeled "K"). Sketch your answer on the circuit above.

- (iii) In the space provide below sketch the mid-band linear equivalent circuit for this amplifier valid for operation about the operating point Q ($V_{PK} = 160$ V, $V_{GK} = -4$ V).

Problem 3 continued

(iv) Calculate the midband voltage gain, A_v ($\equiv v_{\text{out}}/v_{\text{in}}$), for this amplifier at this bias point, where v_{out} is the voltage across R_L .

$$A_v = \underline{\hspace{2cm}}$$

End of Problem 3

End of Exam