

YOUR NAME _____

*Department of Electrical Engineering and Computer Science
Massachusetts Institute of Technology*

6.012 Electronic Devices and Circuits

Exam No. 2

Notes:

1. Unless otherwise indicated, assume room temperature and that kT/q is 0.025 V. You may also approximate $[(kT/q) \ln 10]$ as 0.06 V.
2. Closed book; one sheet (2 pages) of notes permitted (to be handed in with exam).
3. All of your answers and any relevant work must appear on these pages. Any additional paper you hand in will not be graded.
4. Make reasonable approximations and assumptions. State and justify any such assumptions and approximations you do make.
5. Be careful to include the correct units with your answers when appropriate.
6. Be certain that you have all nine (9) pages of this exam booklet and the formula sheet, and make certain that you write your name at the top of this page in the space provided.

6.012 Staff Use Only	PROBLEM 1	_____	(out of a possible 35)
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	PROBLEM 2	_____	(out of a possible 35)
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	PROBLEM 3	_____	(out of a possible 30)
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	TOTAL		
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Problem 1 (35 points)

You are given a packaged npn silicon bipolar junction transistor (BJT) and are told that it is a well-designed, high performance device with $w_E = 2w_B$ and $w_C = 10w_B$, long minority carrier diffusion lengths, and $N_{DE} \gg N_{AB} \gg N_{DC}$. You are told which lead is the base, but you are not told which is the emitter lead and which is the collector lead. This problem concerns a number of possible measurements you might do to distinguish between the emitter lead and the collector lead.

- (a) [4 pts] Which BJT junction, emitter-base or collector base, if any, has the smallest reverse-bias breakdown voltage and why?

Emitter-base junction Collector-base junction No difference

because

- (b) [4 pts] Which BJT junction, if any, has the largest zero-bias depletion capacitance and why? Assume comparable junction areas.

Emitter-base junction Collector-base junction No difference

because

- (c) (i) [4 pts] At which BJT junction, if any, is there more reduction of the effective base width (i.e. base width modulation) when the junction is reverse biased, and why?

Emitter-base junction Collector-base junction No difference

because

Problem 1 continues on the next page

Problem 1 continued

(ii) [3 pts] If the junction you identified Part (c) (i) is used as the collector-base junction, would one find an Early voltage that is larger or smaller in magnitude than one would find if the other junction had been used as the collector-base junction, and why?

Larger $|V_A|$ Smaller $|V_A|$ No difference

because

(d) [4 pts] Which BJT junction, if any, has the largest reverse saturation current, I_S , when the other junction is short circuited, and why?

Emitter-base junction Collector-base junction No difference

because

You may have been able to find the right terminals but suppose your friend could not and decided to try to figure out the proper connection by using the transistor in a circuit in each of the two possible connections. He biased the BJT with a current of 1 mA into what he assumed was the collector and measured the incremental parameters of the device. He then switched the device around so he was using the other lead as the collector and re-measured the parameters.

(e) [4 pts] For which, if any, connection is the transconductance, $g_{m'}$ largest and why?

Proper connection Reversed Connection No difference

because

Problem 1 continues on the next page

Problem 1 continued

- (f) [4 pts] For which connection, if any, is the input resistance, r ($\equiv 1/g$) largest and why?

Proper connection Reversed Connection No difference

because

- (g) [4 pts] For which connection, if any, is the output conductance, g_o ($\equiv 1/r_o$), largest and why?

Proper connection Reversed Connection No difference

because

- (h) [4 pts] For which connection, if any, is the diffusion capacitance component of C_p largest, and why?

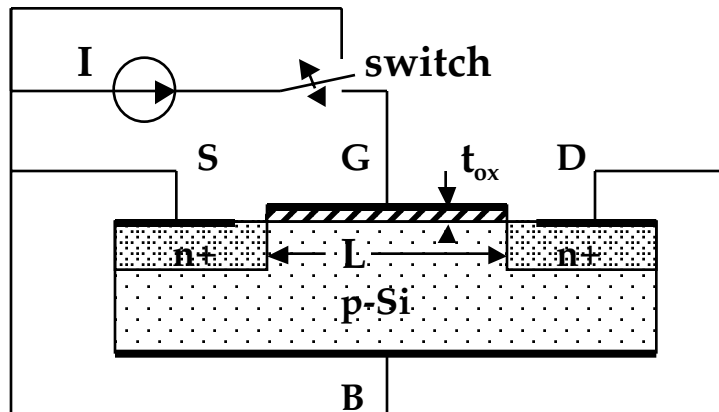
Proper connection Reversed Connection No difference

because (you may want to provide sketches of p' and n' through the device)

End of Problem 1

Problem 2 (35 points)

(a) The first portion of this problem deals with the MOSFET illustrated below. The gate metal electrostatic potential relative to intrinsic Si, ϕ_{mv} is 0.5 V, and the gate oxide thickness, t_{ox} is 5 nm (5×10^{-7} cm). The gate (and channel) length, L , is $0.5 \mu\text{m}$, and the gate (and channel) width is $10 \mu\text{m}$. The bulk silicon wafer is doped p-type with $N_{Ap} = 10^{17} \text{cm}^{-3}$.



Initially the back contact, B, the drain contact, D, and the source contact, S, are connected together so that $v_{BS} = v_{DS} = 0$. The gate contact is connected to the current source and switch circuit as shown. The switch is closed long enough to charge the gate up with an amount of charge per unit area Q_G^* , and is then opened.

- (i) [5 pts] What density of charge, Q_G^* , must be put on the gate to place the surface of the semiconductor under the gate just at threshold, i.e. to make $\phi(0) = -\phi_p$?

$$Q_G^* = \text{_____ Coul/cm}^2.$$

- (ii) [5 pts] If the charge in Part (a)(i) is supplied by a $10 \mu\text{A}$ current source, how long will it take to charge up the gate with Q_G^* ?

$$t = \text{_____ s.}$$

- (iii) [5 pts] How much charge in addition to Q_G^* would have to be put on the gate of this MOSFET to induce an inversion layer with a charge density of $-10^{-7} \text{ coul/cm}^2$ under the gate?

$$Q_{TOT}^* - Q_G^* = \text{_____ Coul/cm}^2.$$

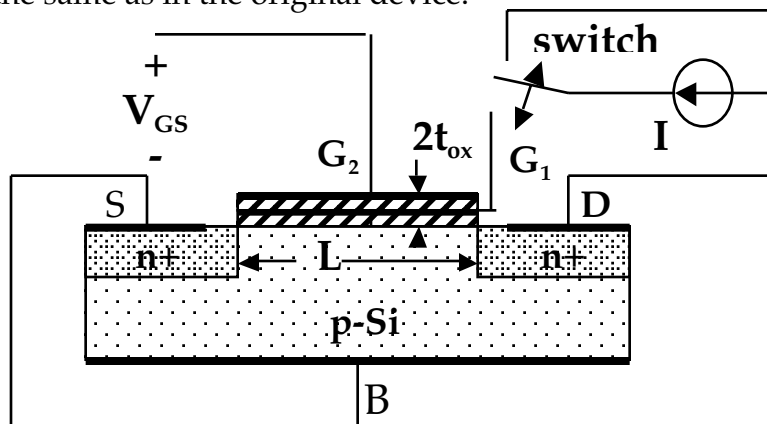
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Problem 2 continued

- (iv) [4 pts] What is $(v_{GS} - V_T)$, the difference between the gate to source voltage, v_{GS} , and the threshold voltage, V_T , in the situation described in Part (a)(iii)?

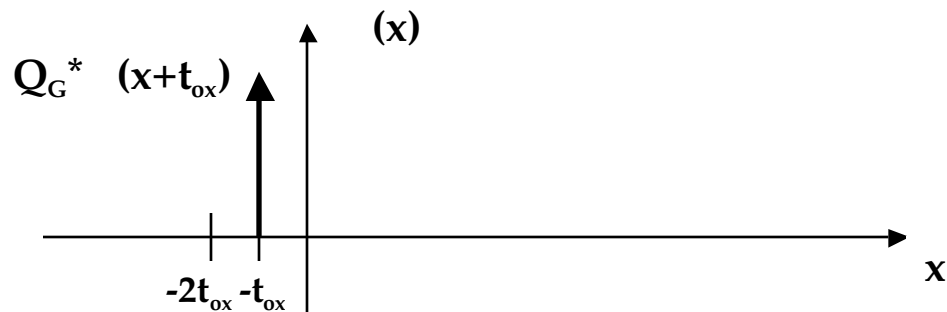
$(v_{GS} - V_T) = \text{_____ Volts.}$

(b) Now consider the situation illustrated below in which a second layer of insulator and a second gate electrode are added to the structure. The metal used to make the second gate, and its dimensions are identical to the first gate; the second layer of insulator and its thickness are also the same as in the original device.



The upper gate, G_2 , is shorted to the source, $V_{GS} = 0$, and the switch is closed to again charge the first gate, G_1 , with the same amount of charge, Q_G^* , as in Part (a)(i). After gate G_1 is charged, the switch is left open and sufficient voltage, V_{GS} , is applied between the upper gate, G_2 , and source to reach the flatband condition [i.e., $\psi(0) = \psi_p$].

- (i) [4 pts] On the axes provided below sketch the net charge distribution through this structure from the upper gate to the p-Si bulk, when the upper gate, G_2 is biased as just described [i.e., so that $\psi(0) = \psi_p$]. The net charge density on the isolated gate is already drawn.



Problem 2 continues on the next page

Problem 2 continued

- (ii) [4 pts] On the axes provided below sketch the electrostatic potential, $\phi(x)$, in the situation described in Part (b)(i) from the metal contact on the second gate, G_2 , to the metal contact at the back of the device. Assume the contact and gate metals are the same material. Remember that the gate, G_2 , is biased with V_{GS} and the semiconductor is in its flatband condition.



- (iii) [4 pts] What is the flatband voltage of this structure? Give a numerical value and give an expression for the flatband voltage as a function of Q_G^* .

$$V_{FB} = \text{_____ Volts} = \text{_____}.$$

- (c) [4 pts] The type of stacked-gate MOSFET you considered in Part (c) is functionally similar to those used in flash memories. In a flash memory charge can be put on an isolated gate, as in this device, and the presence or absence of the charge is used represent a "one" or a "zero", respectively.

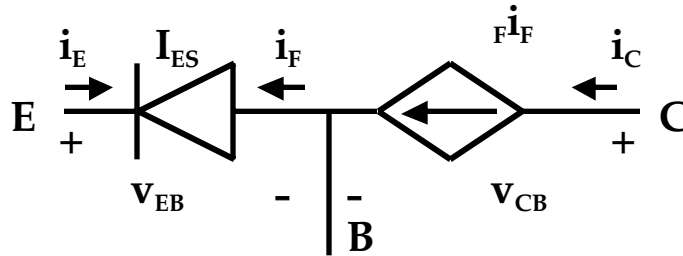
Must Q_G^* be positive or negative to make the threshold voltage of the stacked-gate MOSFET more positive than it is when Q_G^* is zero? Explain your answer.

Positive Negative because

End of Problem 2

Problem 3 - (30points)

Our large signal forward active region model for an npn bipolar junction transistor is drawn in the common-base configuration below. Notice that in this configuration the base terminal is common to both the input and output circuits.



In this model $\beta_F \approx [1 - (1 - \beta_{CB}) / \beta_{FO}]$, and β_{FO} , β_{CB} , and I_{ES} are not functions of v_{EB} or v_{CB} .

- (a) [6 pts] Write expressions for the two terminal currents, i_E and i_C , as functions of the terminal voltages, v_{EB} and v_{CB} .

$$i_E(v_{EB}, v_{CB}) = \underline{\hspace{10cm}}$$

$$i_C(v_{EB}, v_{CB}) = \underline{\hspace{10cm}}$$

- (b) [12 pts] For incremental operation about a bias point in the forward active region the small signal currents and voltages are approximately linearly related as:

$$i_e \approx g_i v_{eb} + g_r v_{cb} \quad \text{and} \quad i_c \approx g_f v_{eb} + g_o v_{cb}$$

Find approximate expressions for g_i , g_r , g_f and g_o in terms of the bias point voltages and currents.

(i) g_i :

(ii) g_r :

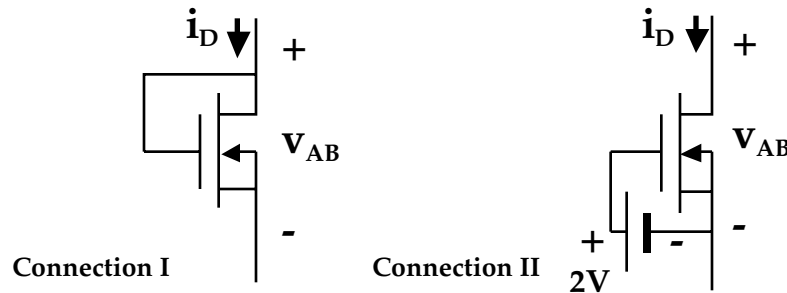
(iii) g_f :

(iv) g_o :

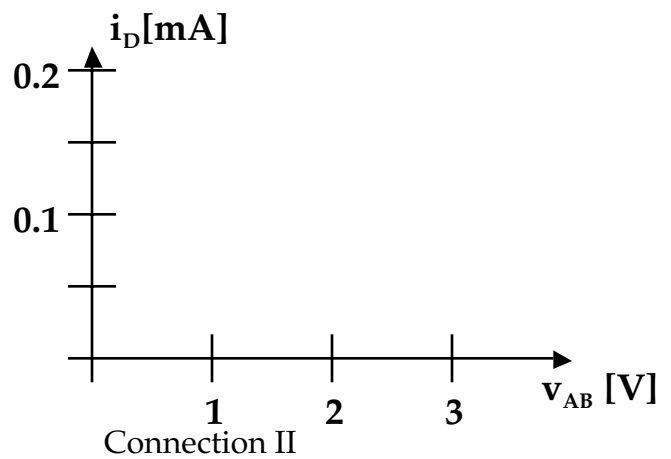
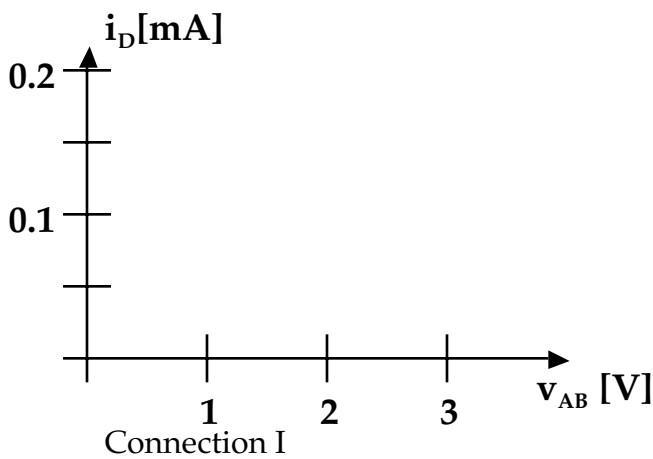
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Problem 3e continued

Consider connecting n-channel enhancement mode MOSFETs as "diodes". Two possible connections are shown below. For these MOSFETs K is 0.1 mA/V^2 , V_T is 1 V , and $|V_A|$ is 5 V .



- c) [6 pts] On the axes provided below sketch and dimension i_D vs v_{AB} for $v_{AB} \geq 0$ for each connection. Give expressions for $i_D(v_{AB})$ in each of the regions of your sketches.



- d) In the spaces provided below sketch small signal linear equivalent circuit models for each of these connections that are valid when $V_{AB} > |V_T|$, and indicate how the values of all parameters in your models depend on the bias point.

(i) [3 pts] Connection I:

(ii) [3 pts] Connection II: