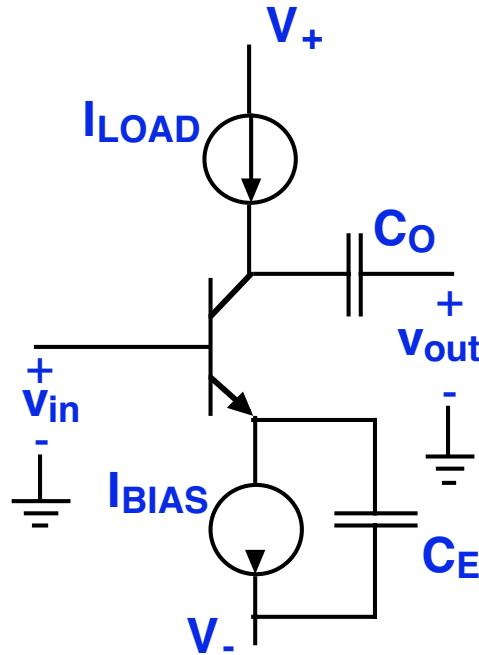


## Lecture 21 - Linear Amp. Analysis and Design II - Outline

- **Announcements**
  - Handouts - Lecture Outline and Summary
  - Design Problem - Answer sheet and final specs out Wed.
- **Review - Non-linear and active loads**
  - Non-linear loads: large  $r_{\text{eff}}$  @ large I, small  $V$  (Use biased BJT or MOSFET)
  - Active loads: current mirror, Lee load (Reduced common-mode gain)
  - Expressing gain in terms of device parameters and constraints
- **General Multi-stage Amplifiers - using design problem as example**
  - Gain and bias analysis
  - Input and output voltage swings
  - Output stages: output resistance, loading on gain stage
- **Specialty stages**
  - Emitter-/source-coupled pairs (diff amps)
  - Push-pull or Totem pole output
  - Cascode
  - Darlington

# Current Source Loads: a higher maximum gain

- current source loads eliminate the compromise between voltage gain and output voltage swing



## Maximum Voltage gain

$$\text{Bipolar : } |A_{v,\max}| = \frac{g_m}{g_{oL} + g_{oQ}} = \frac{qI_C/kT}{I_C/V_{AL} + I_C/V_{AQ}} = \frac{V_{A,\text{eff}}}{V_{\text{thermal}}}$$

$$\text{MOSFET* : } |A_{v,\max}| = \frac{g_m}{g_{oL} + g_{oQ}} = \frac{2I_D/[V_{GS} - V_T]}{I_D/V_{AL} + I_D/V_{AQ}} = \frac{2V_{A,\text{eff}}}{[V_{GS} - V_T]_{\min}}$$

$$\text{with } V_{A,\text{eff}} \equiv \frac{V_{AL}V_{AQ}}{[V_{AL} + V_{AQ}]}$$

Typically  $V_{A,\text{eff}} \gg [I R_L]_{\max}$

# Achieving the maximum gain: Comparing linear resistors, current sources, and active loads

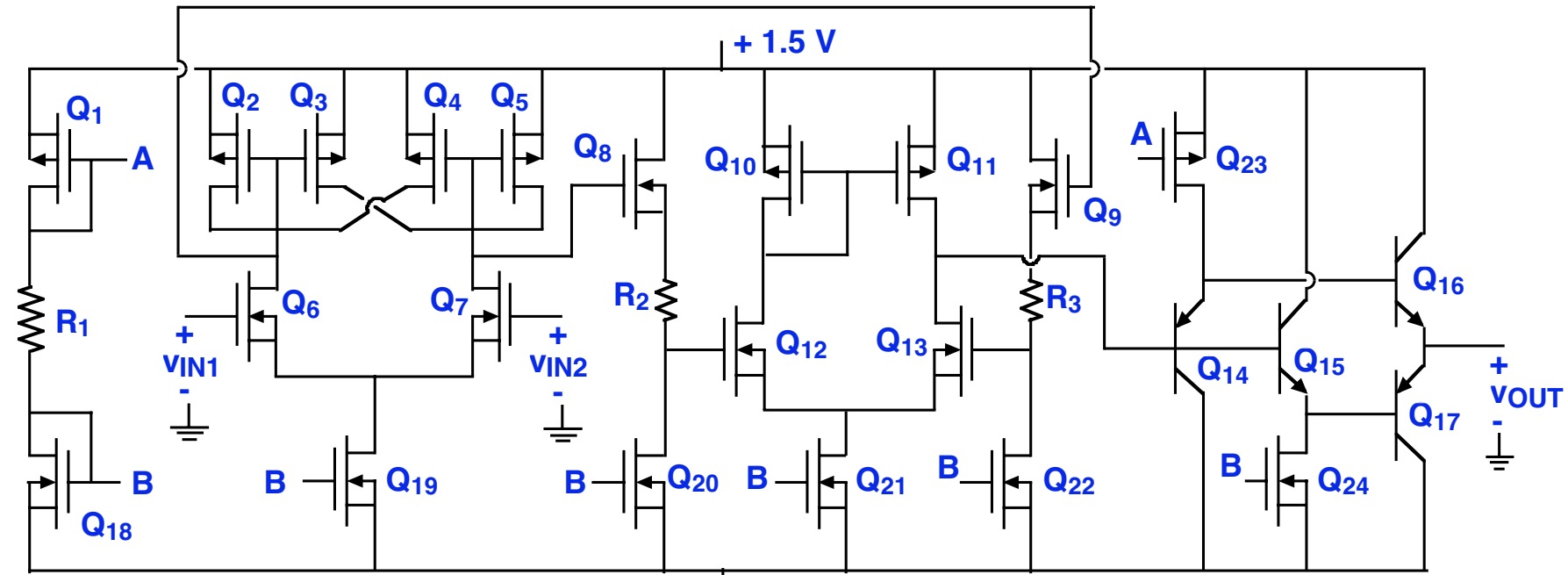
MAXIMUM GAIN	<u>Bipolar</u>	<u>MOSFET</u>
<u>Linear resistor loads</u>	$\frac{[I_C R_L]_{\max}}{V_{thermal}}$	$\frac{[I_D R_L]_{\max}}{[V_{GS} - V_T]_{\min}}$
<u>Current source loads</u>	$\frac{2V_{A,eff}}{V_{thermal}}$	$\frac{2V_{A,eff}}{[V_{GS} - V_T]_{\min}}$
Difference mode	$\mu \frac{V_{A,eff}}{V_{thermal}}$	$\mu \frac{V_{A,eff}}{[V_{GS} - V_T]_{\min}}$
<u>Active loads</u>		
Common mode	$\mu \frac{V_{thermal}}{V_{A,bias}}$	$\mu \frac{[V_{GS} - V_T]_{\min}}{V_{A,bias}}$

## Observations:

- Non-linear (current source) loads typically yield higher gain than linear resistors, i.e.  $V_{A,eff} \gg [I_D R_L]_{\max}$
- Bias level is not important to BJT stage gain
- A MOSFET should be biased at low level for high gain
- For active loads what increases  $A_{vd}$ , decreases  $A_{vc}$

6.012 - Electronic Devices and Circuits  
**Fall 2003 Design Problem Circuit**

**Full schematic**



Bias chain

Common-source  
gain stage with  
Lee load

Source-  
follower  
stage with  
degeneration  
to provide  
level shift

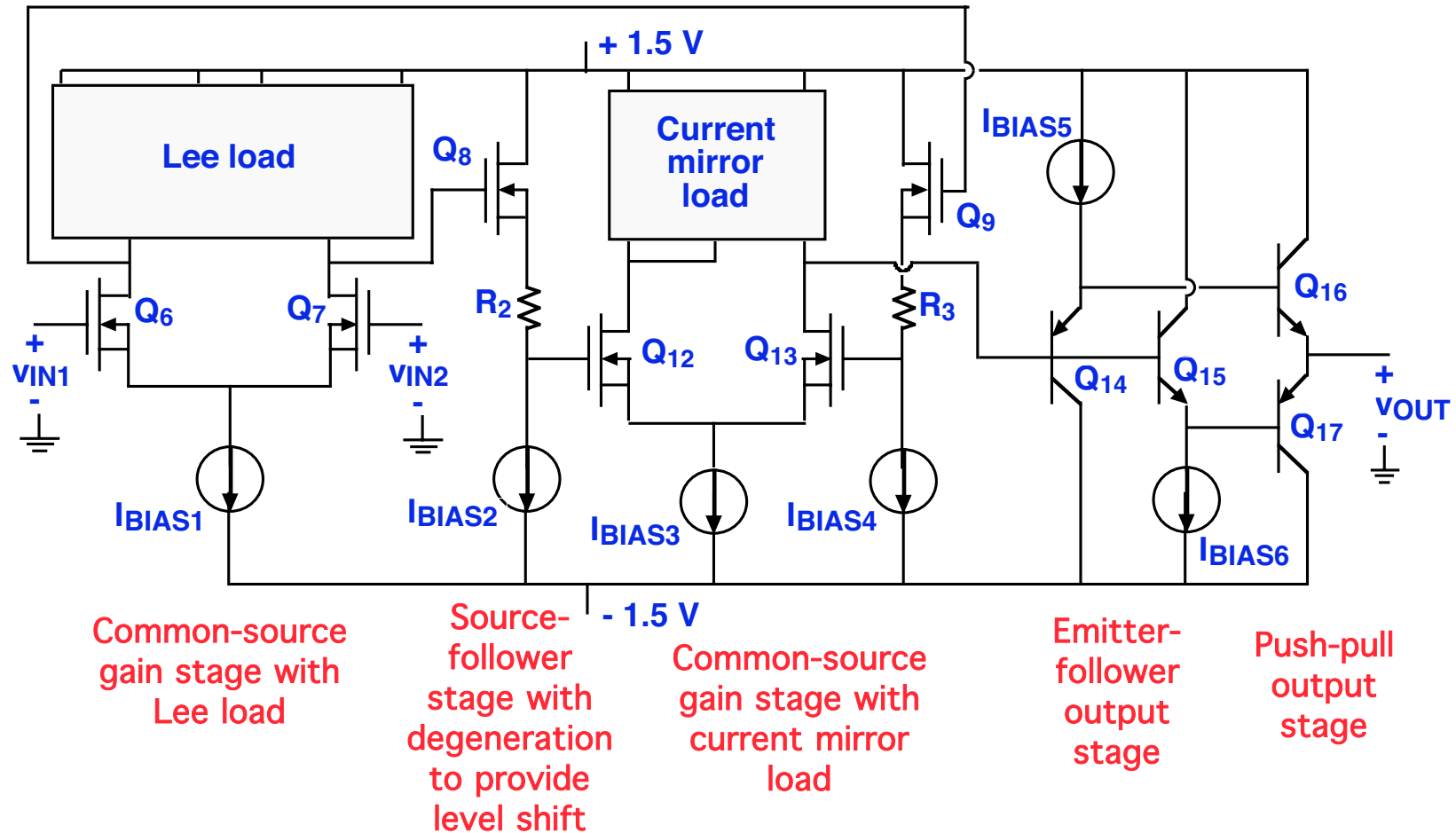
Common-source  
gain stage with  
current mirror  
load

Emitter-  
follower  
output  
stage

Push-pull  
output  
stage

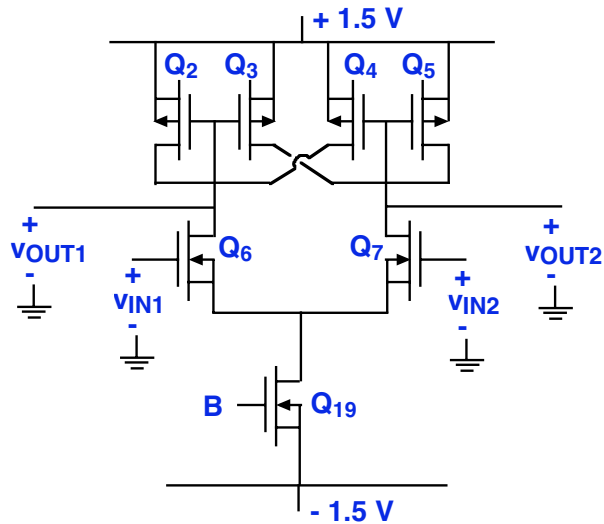
# Fall 2003 Design Problem Circuit

## Conceptual schematic: full circuit

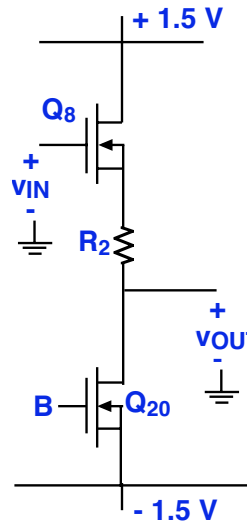


# Fall 2003 Design Problem Analysis

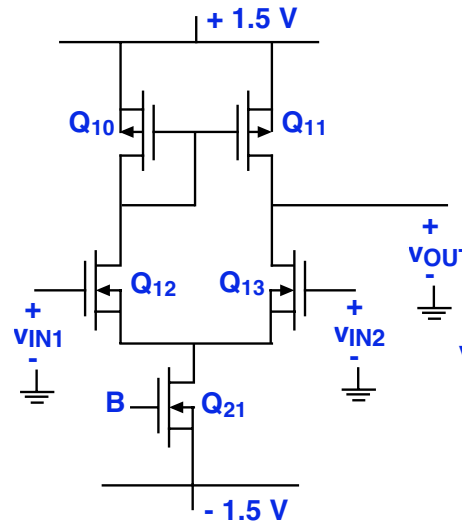
## Breaking out the individual stages



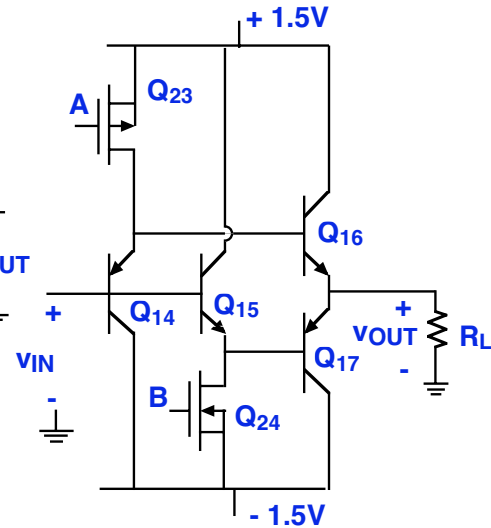
Common-source gain stage with Lee load



Source-follower stage with degeneration to provide level shift



Common-source gain stage with current mirror load



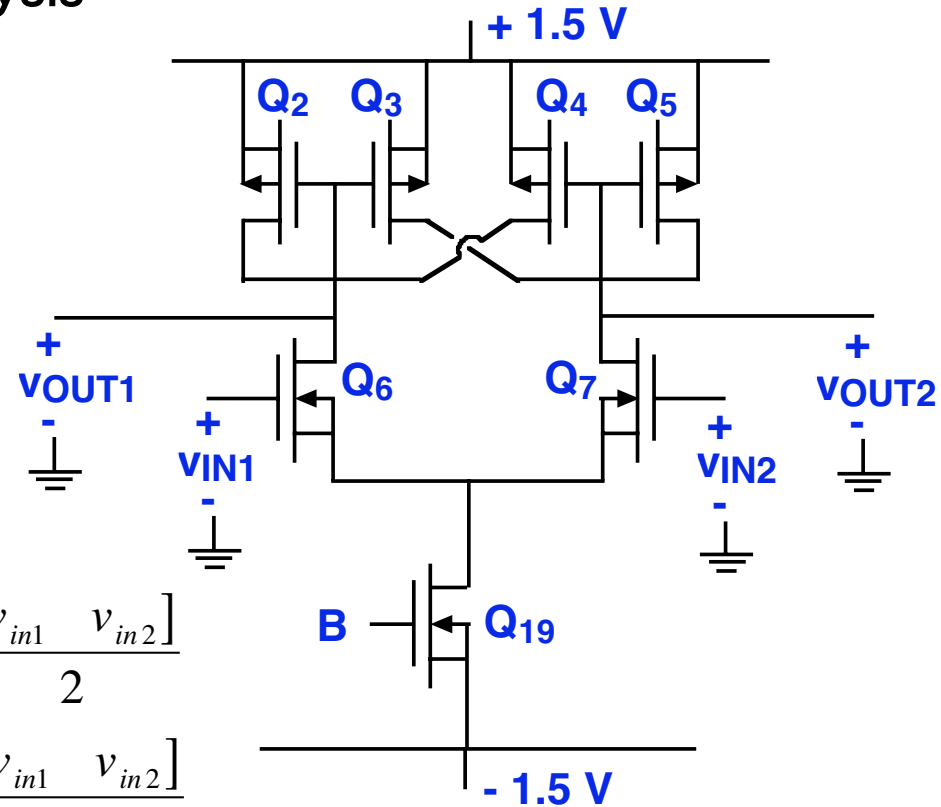
Emitter-follower output stage

Push-pull output stage

We'll next look at the issues associated with each stage.

# Fall 2003 Design Problem Analysis

The first stage:  
uses the Lee Load to get large common-mode rejection in a fully-differential stage



We find:

$$v_{out1} = \frac{g_{o19}}{4g_{m2}} \frac{[v_{in1} + v_{in2}]}{2} + \frac{g_{m6}}{g_{o6} + 2g_{o2}} \frac{[v_{in1} - v_{in2}]}{2}$$

$$v_{out2} = \frac{g_{o19}}{4g_{m2}} \frac{[v_{in1} + v_{in2}]}{2} - \frac{g_{m6}}{g_{o6} + 2g_{o2}} \frac{[v_{in1} - v_{in2}]}{2}$$

And also see:

$$\frac{g_{o19}}{4g_{m2}} = \frac{I_{D19}/V_{A19}}{4 \cdot 2I_{D2}/[V_{SG2} - V_T]} = \frac{[V_{SG2} - V_T]}{2V_{A19}}$$

$$\frac{g_{m6}}{g_{o6} + 2g_{o2}} = \frac{2I_{D6}/[V_{GS6} - V_T]}{I_{D6}/V_{A6} + 2I_{D2}/V_{A2}} = \frac{2V_{A6}}{[V_{GS6} - V_T]} \cdot \frac{1}{1 + V_{A6}/V_{A2}}$$

There is only so much you can do (but you can do a few things)!

# Fall 2003 Design Problem Analysis

## The second stage:

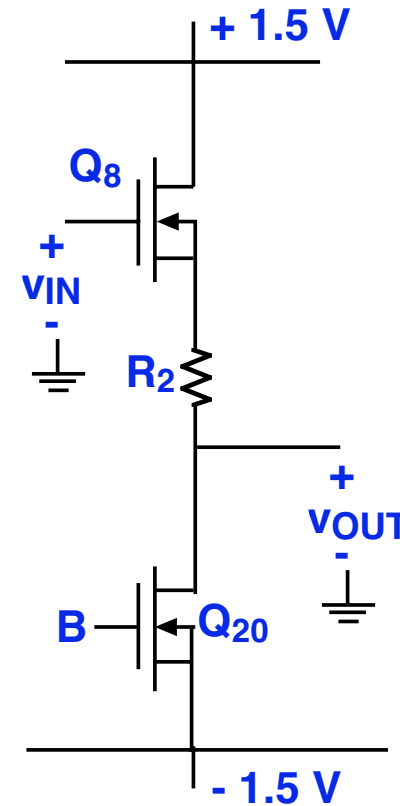
a source-follower with degeneration to shift the level of the input to the third stage.

We find the voltage gain of this stage is:

$$V_{out} = \frac{r_{o20}}{r_{o20} + R_2}$$

Hopefully this can be made close to one.

The DC level shift is:  $V_{OUT} = V_{IN} + [V_{GS8} - V_T] - R_2 I_{D20}$

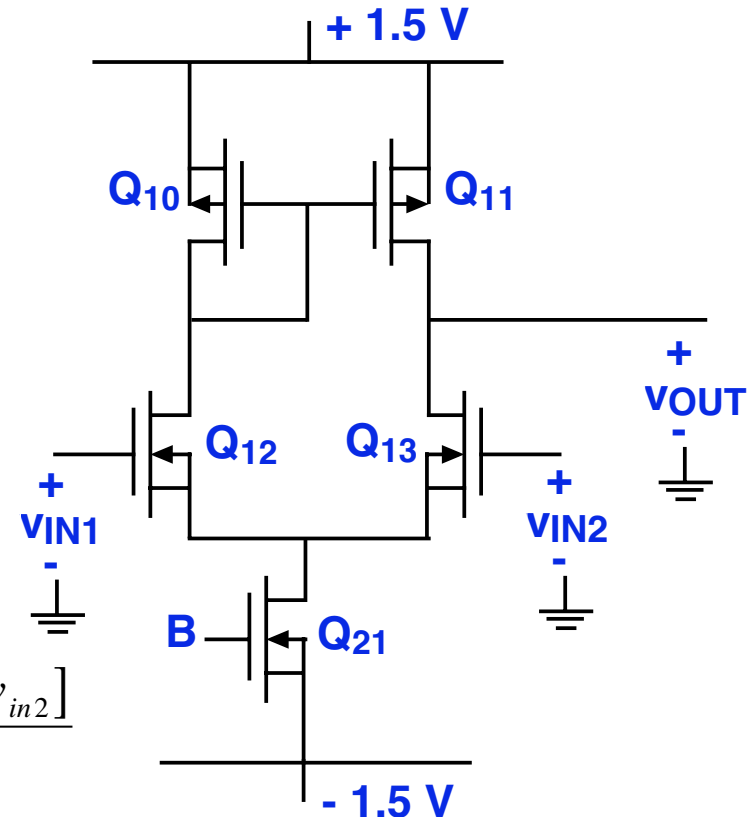


Your job is to figure out why you want to shift the level, and by how much.

## Fall 2003 Design Problem Analysis

### The third stage:

uses the Current Mirror Load to convert efficiently from a double-ended to single-ended output and to get more differential gain and common-mode rejection.



We find:

$$v_{out} = \frac{g_{o21}}{2g_{m10}} \frac{[v_{in1} + v_{in2}]}{2} + \frac{2g_{m13}}{g_{o13} + g_{o11} + G_{L3}} \frac{[v_{in1} - v_{in2}]}{2}$$

$$\text{and: } \frac{g_{o21}}{2g_{m10}} = \frac{I_{D21}/V_{A21}}{2 \cdot 2I_{D10}/[V_{SG10} - V_T]} = \frac{[V_{SG10} - V_T]}{2V_{A21}}$$

$$\frac{2g_{m13}}{g_{o13} + g_{o11} + G_{L3}} = \frac{2 \cdot 2I_{D13}/[V_{GS13} - V_T]}{I_{D13}/V_{A13} + I_{D11}/V_{A11} + G_{L3}} = \frac{4V_{A13}}{[V_{GS13} - V_T]} \cdot \frac{1}{1 + V_{A13}/V_{A11} + V_{A13}G_{L3}/I_{D11}}$$

To maximize this gain we make  $V_{A11}$  larger and the bias current  $I_{D13}$  large to reduce the impact of  $G_{L3}$ .

## Fall 2003 Design Problem Analysis

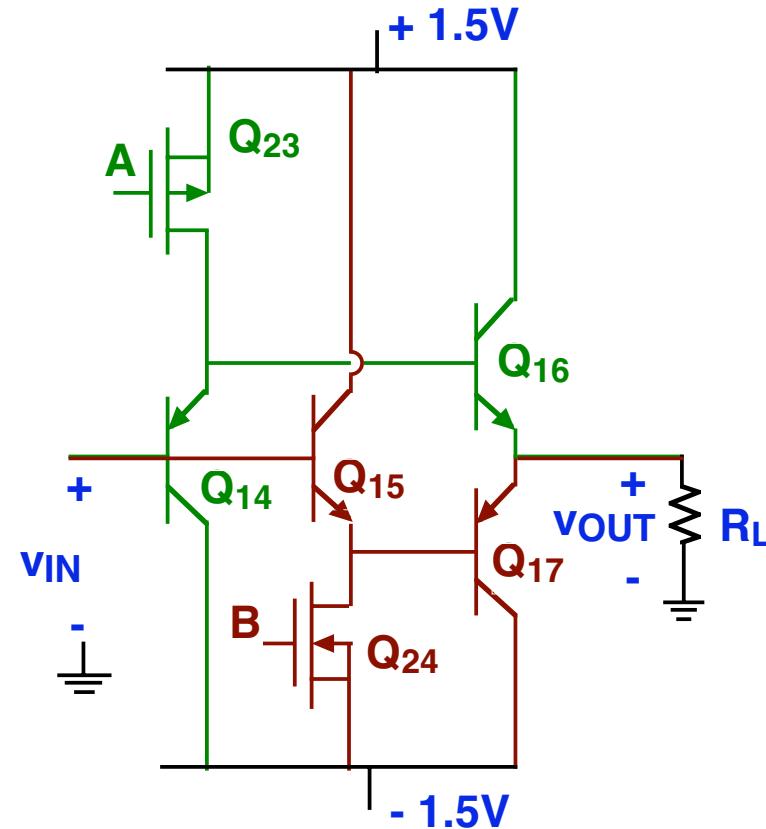
### The fourth and fifth stages:

Two parallel paths, one active when the output goes positive, the other when it goes negative. Each path consists of two emitter follower stages.

You will find that these two stages impact many aspects of your design, including:

1. The DC level at the output
2. The output voltage swing
3. The output resistance
4. The load seen by stage 3
5. The power dissipation

To begin,  $Q_{16}$  and  $Q_{17}$  have to be large enough to supply the current needed to  $R_L$  at a modest  $v_{BE}$ , and the current sources  $Q_{23}$  and  $Q_{24}$  need to be large enough to supply the base currents  $Q_{16}$  and  $Q_{17}$  demand when at peak swing.



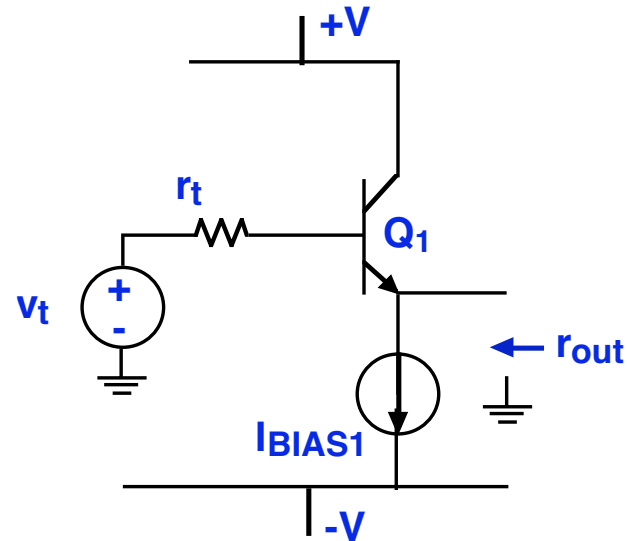
# Fall 2003 Design Problem Analysis

## Output resistance:

we begin with a single emitter follower

We have

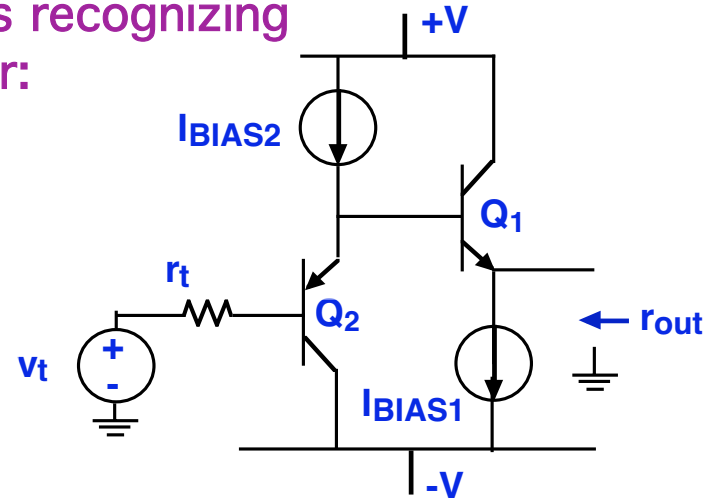
$$r_{out} = \frac{r_1 + r_t}{\beta_1 + 1}$$



Next look at the pair of emitter followers recognizing that the  $r_{out}$  of one is the  $r_t$  of the other:

now:

$$r_{out} = \frac{r_1 + \frac{r_2 + r_t}{\beta_2 + 1}}{\beta_1 + 1} = \frac{r_1}{\beta_1 + 1} + \frac{r_2}{\beta_1 \beta_2 + 1} + \frac{r_t}{\beta_1 \beta_2 + 1}$$



In the design problem we have two paths in parallel and thus have:

$$r_{out} = \frac{r_{16}}{16} + \frac{r_{14}}{16 \cdot 14} \parallel \left( \frac{r_{17}}{17} + \frac{r_{15}}{17 \cdot 15} + \frac{r_t}{16 \cdot 14} \right) \quad \text{with} \quad r_t \equiv \frac{1}{g_{o11} + g_{o13}}$$

## Fall 2003 Design Problem Analysis

### Load resistance on Stage 3: again begin with a single emitter follower

We have

$$r_{in} = r_1 + [1 + 1]R_L = r_1 + 1R_L$$

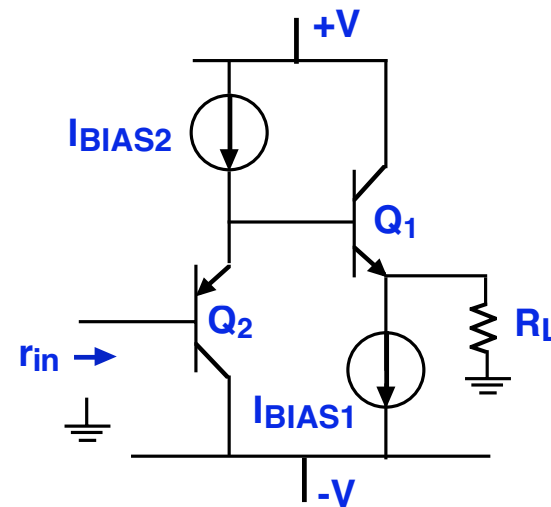
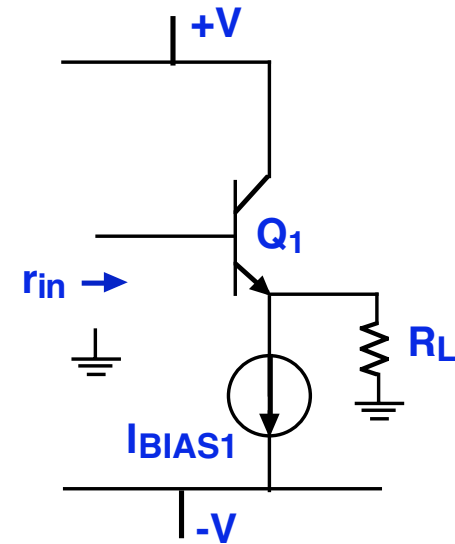
Next look at the pair of emitter followers recognizing that the  $r_{in}$  of one is the  $R_L$  of the other:

$$\begin{aligned} \text{now: } r_{in} &= r_2 + [2 + 1]\{r_1 + [1 + 1]R_L\} \\ &= r_2 + [2 + 1]r_1 + [2 + 1][1 + 1]R_L \\ &= r_2 + 2r_1 + 1 \cdot 2R_L \end{aligned}$$

In the design problem we again have two paths in parallel and thus have:

$$R_{L3} = \{r_{14} + [14 + 1]r_{16}\} \parallel \{r_{15} + [15 + 1]r_{17}\} + [16 + 1][14 + 1]R_L$$

Notice that some of what makes  $R_{L3}$  big, makes  $r_{out}$  big also, so compromise may be needed.



# Fall 2003 Design Problem Analysis

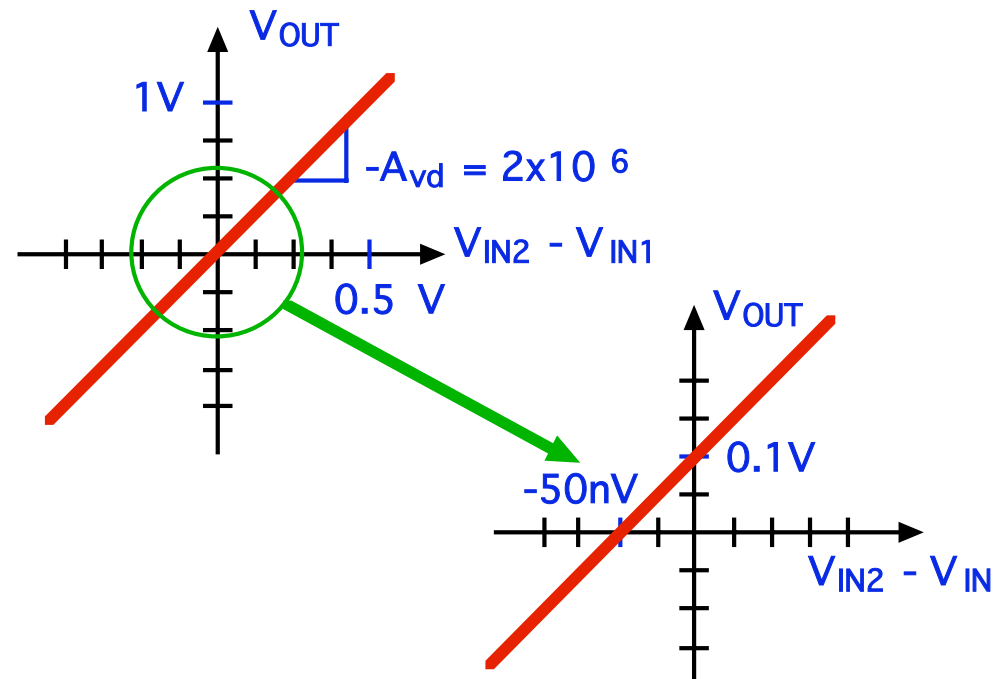
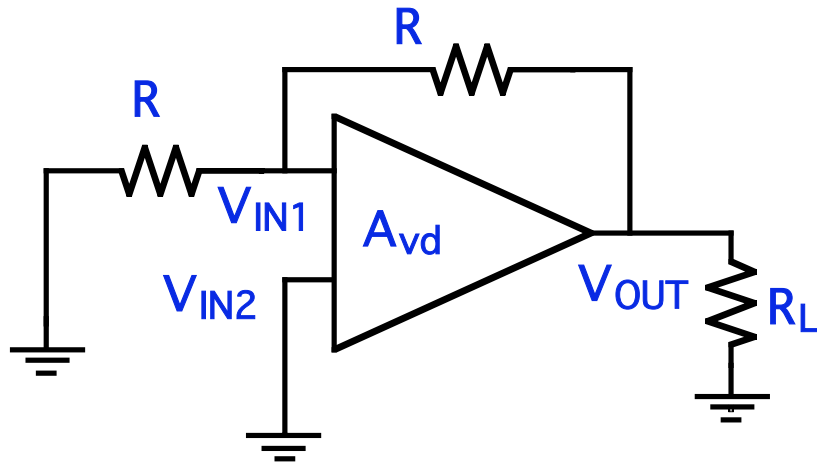
## DC off-set at the output:

### DC off-set:

The transfer characteristic,  $V_{OUT}$  VS  $V_{IN1} - V_{IN2}$ , will not in general go through the origin, i.e.,

$$V_{OUT} = A_{vd}(V_{IN1} - V_{IN2}) + V_{OFFSET}$$

In the example in the figure  $A_{vd}$  is  $-2 \times 10^6$ , and  $V_{OFFSET}$  is 0.1 V.

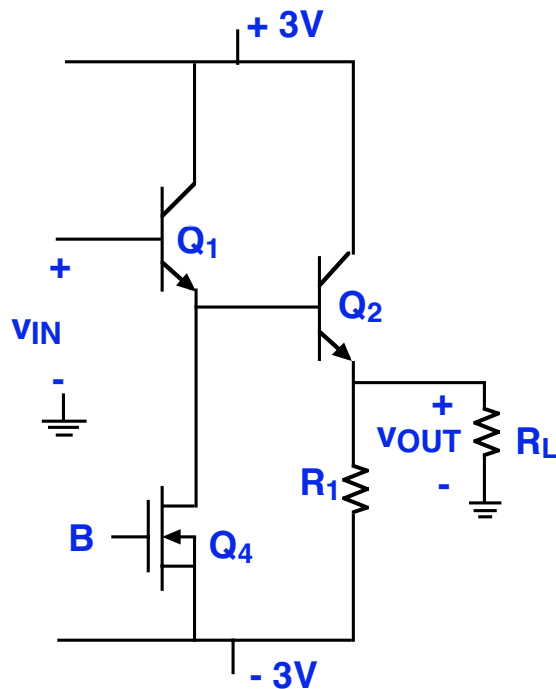


In use (with shunt feedback, for example) the off-set with zero input is negligible. In this example, with  $R = R$ ,  $V_{OUT}(0)$  is only 0.1 mV.

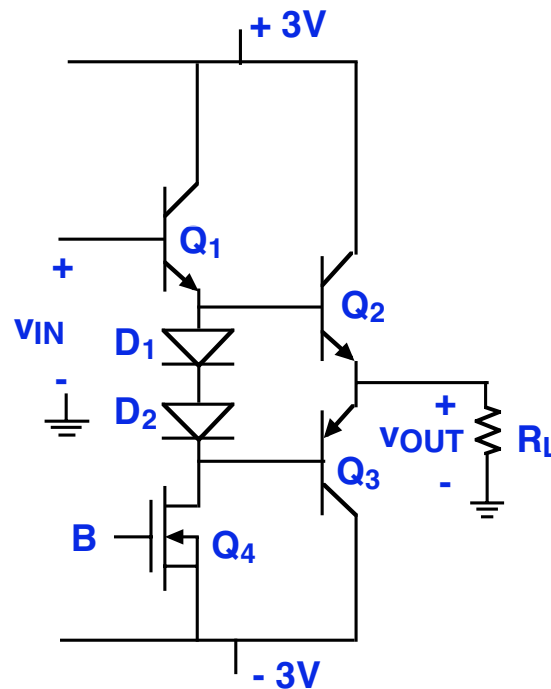
# Multi-stage amplifier analysis/design - special pair stages

## Push-pull output stages:

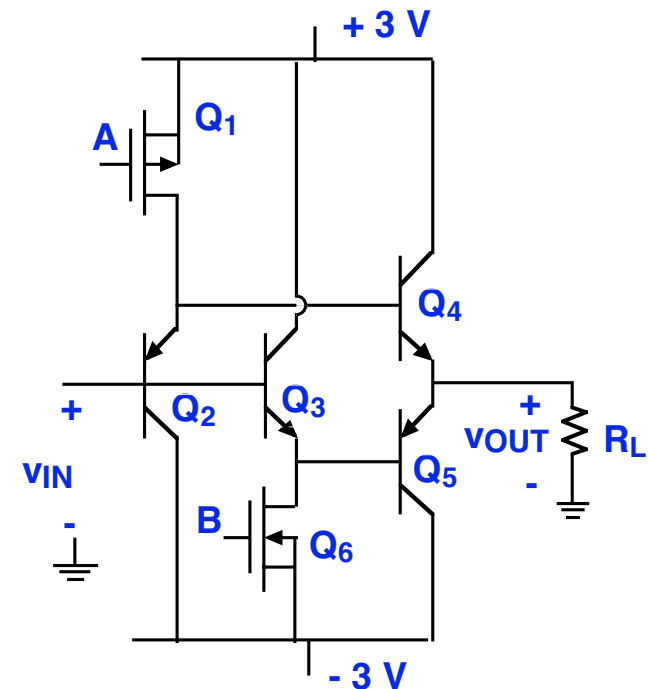
High input resistance, low output resistance, large drive capability



Emitter-follower output:  
negative swing imposes  
constraint on DC power.



Conventional push-pull:  
limited in voltage swing by  
the two B-E diode drops.



Variation on push-pull: larger  
voltage swing possible; some  
power cost.

## Multi-stage amplifier analysis/design - special pair stages

The Darlington connection:  
A bipolar stage used to get a high input resistance

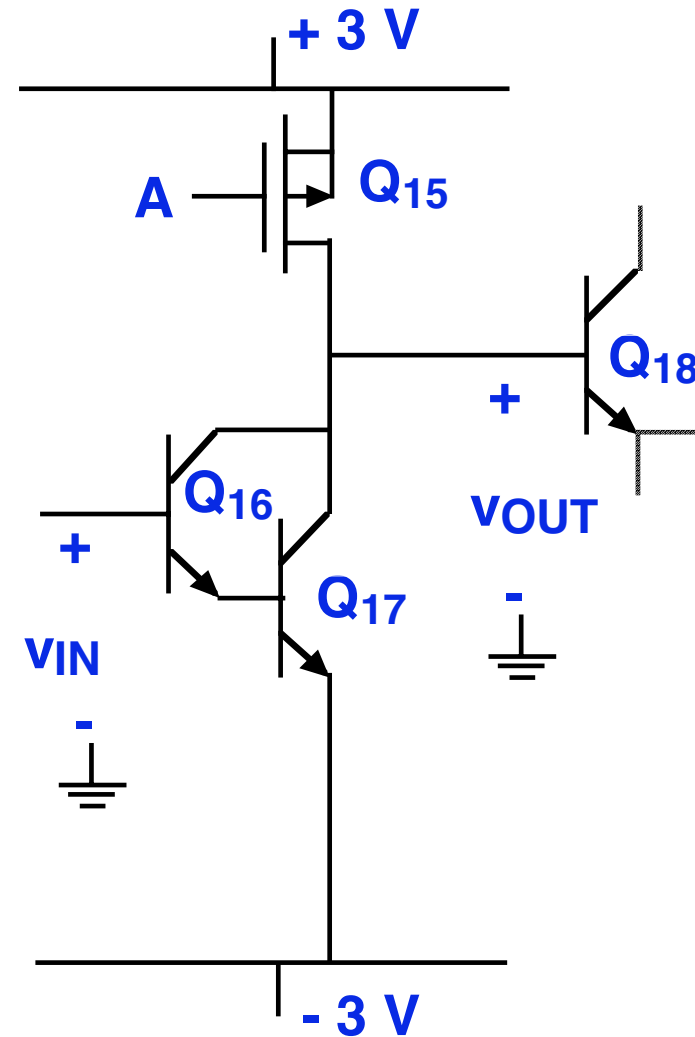
$$r_{in} \approx 2 r_{17} = 2 \beta^2 / g_{m17}$$

$$r_{out} \approx 1 / (1.5 g_{o17} + g_{o15})$$

$$v_{out} = -(g_{m17} / 2 [1.5 g_{o17} + g_{o15} + g_{in18}]) v_{in}$$

where

$$g_{in18} = 1 / [r_{18} + (\beta + 1) r_{19} + (\beta + 1)^2 R_{LOAD}]$$



## Lecture 21 - Linear Amp. Analysis and Design II - Summary

- **The Design Problem Circuit - continued discussion**
  - Gains: expressing gain in terms of bounds on devices (Identifying the constraints)
  - Output specs: increased bias currents and larger device sizes in output stages
  - Input/output swings: transistors must remain active
- **General Multi-stage Amplifier Design -**
  - Issues/stage choices: matching DC levels, loading, buffering
  - Examples: the A 741, design problem circuit
- **Specialty stages**
  - Emitter-/source-coupled pairs
    - our familiar differential amplifier building block
  - Push-pull
    - large output swing with reduced quiescent power
  - Cascode
    - used to get large  $R_{out}$ ; also good high freq. Performance
    - will discuss more in Lecture 23
  - Darlington
    - used to get large  $R_{in}$  bipolar stages