

YOUR NAME _____

*Department of Electrical Engineering and Computer Science
Massachusetts Institute of Technology*

6.012 Electronic Devices and Circuits

Exam No. 2

Notes:

1. Unless otherwise indicated, assume room temperature and that kT/q is 0.025 V. You may also approximate $[(kT/q) \ln 10]$ as 0.06 V.
2. Open book: 6.012 text and up to one shopping cart full of notes permitted.
3. All of your answers and any relevant work must appear on these pages. Any additional paper you hand in will not be graded.
4. Make reasonable approximations and assumptions. State and justify any such assumptions and approximations you do make.
5. Be careful to include the correct units with your answers when appropriate.
6. Be certain that you have all nine (9) pages of this exam booklet and make certain that you write your name at the top of this page in the space provided.

6.012 Staff Use Only	PROBLEM 1	_____	(out of a possible 40)
	PROBLEM 2	_____	(out of a possible 30)
	PROBLEM 3	_____	(out of a possible 30)
	TOTAL		

Problem 1 - (40 points)

For Parts a, b, and c, you are given an MOS capacitor made on uniformly doped silicon and you are told that its flat-band voltage, V_{FB} , is + 1 V, and that its threshold voltage, V_T , is + 3 V. You are also told that the thickness, t_{ox} , of the gate insulator is 80 nm (8×10^{-6} cm) with a dielectric constant, ϵ_{ox} , of 3.2×10^{-13} coul/V-cm.

a) What is the doping type of the silicon, n-type or p-type? Explain your answer.

n-type p-type indeterminate, because

b) What is the condition of the oxide-silicon interface when v_{GB} , the voltage on gate relative to the silicon, is zero volts? Explain your answer.

inverted depleted accumulated, because

c) For what range of v_{GB} is the silicon surface depleted?

_____ < v_{GB} < _____

For parts d, e, f, and g, you have an n-channel silicon MOSFET and a p-channel silicon MOSFET which have the same value of K-factor in their large signal models [where the K-factor is defined as $(W/L)\mu(\epsilon_{ox}/t_{ox})$]. The transistors are identical in all dimensions and doping level magnitudes except that the gate length, L , of one of the devices is twice that of the other. The β -factor for each device is one.

d) Which transistor, if either, would you expect to be the one with the longer gate length, and why?

n-channel p-channel neither, because

e) What is the ratio of the electron to hole mobility in these transistors (i.e., what is the ratio of the mobility of the electrons in the channel of the n-channel MOSFET to that of the holes in the channel of the p-channel MOSFET)? Explain your answer.

Ratio = _____ because

Problem 1 continues on the next page

Problem 1 continued

- f) i) Which transistor, if either, has the larger small-signal gate-to-source capacitance in saturation, C_{gs} ? Explain your answer.

n-channel p-channel they are similar, because

- ii) Which transistor, if either, has the larger small-signal gate-to-drain capacitance in saturation, C_{gd} ? Include parasitic effects. Explain your answer.

n-channel p-channel they are similar, because

- g) i) Which transistor, if either, has the larger Early effect, where by a larger Early effect we mean a greater slope in the output characteristics, i.e., in i_D vs v_{DS} ? Explain your answer.

n-channel p-channel they are similar, because

- ii) If Transistor A has a larger Early effect, as defined immediately above, than Transistor B, for which transistor is the magnitude of the Early voltage, V_A , largest?

Transistor A Transistor B the V_A 's are similar, because

For parts h, i, and j, you again have an n-channel silicon MOSFET and a p-channel silicon MOSFET which have the same value of K-factor in their large signal models. Again the transistors are identical in all dimensions and doping level magnitudes except that now the gate width, W , of one of the devices is twice that of the other.

- h) Which transistor, if either, would you expect to be the one with the larger gate width, and why?

n-channel p-channel indeterminate, because

Problem 1 continues on the next page

Problem 1 continued

i) These two transistors are biased in saturation with the same magnitude of quiescent (i.e., bias) drain current, $|I_D|$. Which device, if any, has the larger transconductance, g_m , for small signal operation about this bias point? Explain your answer.

n-channel p-channel they are similar, because

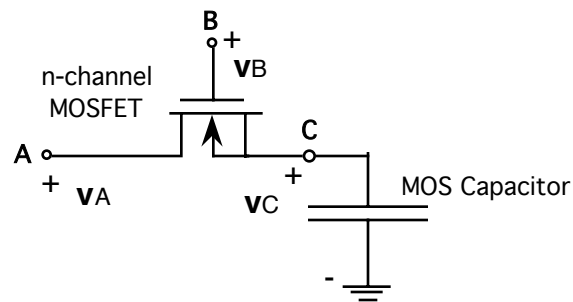
j) These two transistors are again biased in saturation with the same magnitude of quiescent (i.e., bias) drain current, $|I_D|$. Which device, if any, has the larger output conductance, g_o , for small signal operation about this bias point? Explain your answer.

n-channel p-channel they are similar, because

End of Problem 1

Problem 2 (30 points)

The circuit below contains an n-channel, enhancement mode MOSFET and an MOS capacitor. The MOSFET has a threshold voltage of 1 V, a K-factor of 0.1 mA/V^2 , and an β -factor of one. The MOS capacitor is fabricated on the same silicon wafer as the MOSFET and with the same gate oxide as used in the MOSFET gate. The thickness of the gate oxide is 30 nm ($3 \times 10^{-6} \text{ cm}$) and its dielectric constant is $3.2 \times 10^{-13} \text{ coul/V-cm}$. The capacitor area is $100 \mu\text{m}$ by $100 \mu\text{m}$ (10^4 cm^2). The voltages v_A , v_B , and v_C are measured relative to ground.



a) i) A voltage v_C is applied sufficient to place the silicon in the MOS capacitor in accumulation at the oxide-semiconductor interface. What value of small signal capacitance, dq/dv , would you measure for this capacitor?

$$C = \underline{\hspace{2cm}}$$

ii) If the voltage v_C is changed so that the semiconductor of the MOS capacitor is depleted at the oxide-semiconductor interface, is the capacitance you would measure larger or smaller than it was in (i)?

Larger Smaller Similar, because

b) Now suppose v_C is 3 Volts, i.e., ($V_T + 2$ Volts).

i) Is the surface of the silicon at the oxide-semiconductor interface in the MOS capacitor accumulated, depleted, or inverted?

Accumulated Depleted Inverted, because

ii) What type of carriers comprise the mobile charge at this interface?

Electrons Holes None, because

Problem 2 continues on the next page

Problem 2 continued

iii) How much mobile charge is there at this interface?

Total mobile charge at oxide-semiconductor interface: _____

iv) Is the magnitude of the total charge on the metal electrode of the MOS capacitor greater than, less than, or equal to the magnitude of the charge you found in (iii)? Explain your answer.

Greater than Less than Equal to, because

c) Suppose that for $t < 0$, the capacitor in the circuit pictured on the preceding page is discharged, and that v_A , v_B , and v_C are all zero. At $t = 0$, constant voltages V_A and V_B are applied to the terminals A and B, and V_A and V_B are chosen so that the MOSFET will be turned on and the capacitor will charge up to a voltage, V_C , of 3 Volts.

i) What are the minimum values that V_A and V_B can have for this to happen, i.e., for V_C to reach 3 V?

$$V_A \geq \underline{\hspace{2cm}}$$

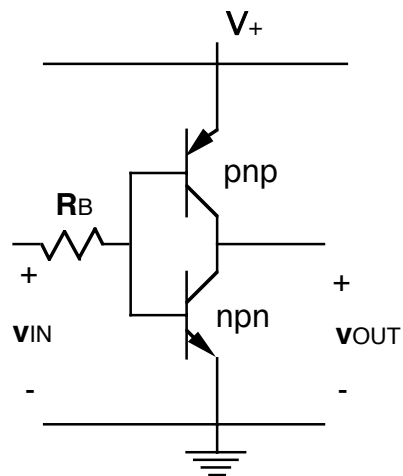
$$V_B \geq \underline{\hspace{2cm}}$$

ii) Write the nonlinear first order differential equation one would have to solve to calculate $v_C(t)$ for $t > 0$. For simplicity, assume that the capacitance of the MOS capacitor is a constant, C_L (this is an approximation). Assume also that $V_A = V_B = 5 \text{ V}$.

End of Problem 2

Problem 3 (30 points)

A bipolar transistor manufacturer who is both impressed by CMOS inverters and fearful of the threat they pose to his business, has developed a complementary bipolar logic family he calls CBL. The basic CBL inverter stage is illustrated below. The uppermost transistor is a pnp BJT and the lower transistor is an npn BJT. The transistors are designed to be symmetrical and to have the same saturation currents and alphas; thus for both $I_{ES} = I_{CS} = 10^{-14}$ A and $\beta_F = \beta_R = 0.9$. You may use $|V_{BE,ON}| \approx 0.6$ V and $|V_{CE,SAT}| \approx 0.2$ V when appropriate.



a) Check to see if the stage illustrated above actually functions as an inverter. Determine the state of each transistor with low and high inputs as directed below and indicate whether or not this stage is an inverter.

i) What is the state of each transistor with $v_{IN} = V_+$, where $V_+ = 1$ V, and is v_{OUT} low or high, and what is its approximate value?

pnp: Cutoff Active Saturated, because

npn: Cutoff Active Saturated, because

v_{OUT} : High Low, with value \approx _____ because

ii) Repeat part (i) with $v_{IN} = 0$ V.

pnp: Cutoff Active Saturated, because

npn: Cutoff Active Saturated, because

v_{OUT} : High Low, with value \approx _____ because

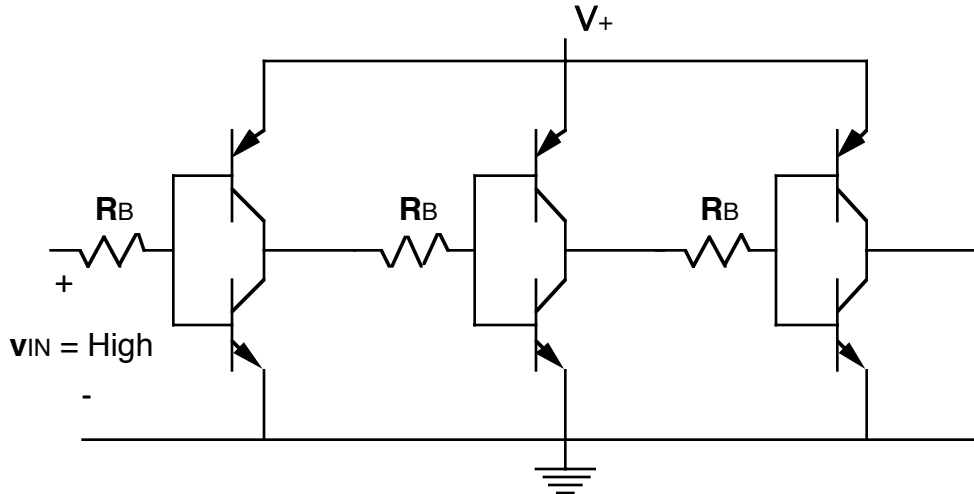
Problem 3 continues on the next page

Problem 3 continued

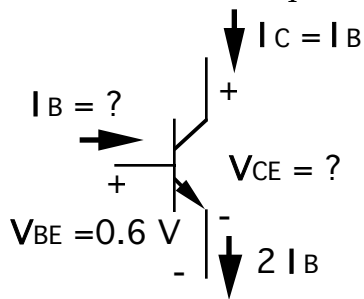
iii) Does this stage function properly as an inverter? Explain your answer

Yes No, because

b) On the string of inverters below indicate with arrows all of the current paths by which current flows from the power supply to ground when the input on the left is high. (It may help you to label which transistors are on and which are off, and which outputs and inputs are high and low on the figure.)



c) i) Use the Ebers-Moll model to determine the values of the base current, I_B , base-collector voltage, V_{BC} , and collector-emitter voltage, V_{CE} , of an npn transistor like the ones used in CBL when a voltage of 0.6V is applied between its base and emitter and the collector current equals the base current, i.e., $i_C = i_B$, as shown below:



$I_B =$ _____

$V_{BC} =$ _____

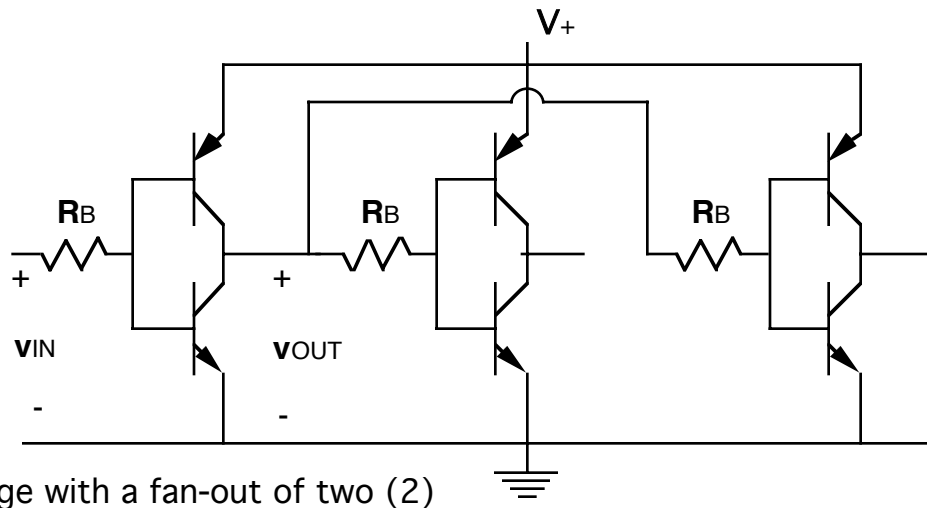
$V_{CE} =$ _____

Problem 3 continues on the next page.

Problem 3 continued

ii) In the space below explain briefly (25 words or less) the relevance of your calculation above to the inverter chain in Part b.

d) Next we want to consider the impact of fan-out on the low and high output voltage levels of CBL inverter stages. Consider a CBL inverter whose output is taken to two stages, i.e. a stage with a fan-out of two (2), as illustrated below.



With a fan-out of two (2) is the low output value (i.e., v_{OUT} with v_{IN} high) higher or lower than it is with a fan-out of one (1)?

Low output value: Lower Higher No different, because

(e) Finally, in the space provided below, briefly explain (25 words or less) why we never worried about the impact of fan-out on the voltage levels of CMOS inverters.

End of Problem 3

End of Exam