

## Lecture 20 - Linear Amp. Analysis and Design I - Outline

- **Announcements**

  - Handouts - Lecture Outline and Summary

  - Announcements - Design Problem due in under two weeks

- **Review - Differential Amplifier Basics**

  - Difference- and common-mode signals:

$$v_{ID} = v_{IN1} - v_{IN2} \text{ and } v_{IC} = (v_{IN1} + v_{IN2})/2 \quad [v_{IN1} = v_{IC} + v_{ID}/2, v_{IN2} = v_{IC} - v_{ID}/2]$$

  - Half-circuits: half of original with wires shorted or broken (familiar, easy analyses)

- **Performance metrics - specific to diff. amps.**

  - Difference- and common-mode gains

  - Common-mode rejection ratio

  - Input and output resistances

  - Common-mode input voltage swing; output voltage swing and DC value

- **Non-linear loads**

  - The limitation of resistive loads: Gain limited by voltage supply

  - Non-linear loads: High incremental resistance w. small voltage drop

- **Active loads**

  - Current mirror load

  - Lee load

# Differential Amplifiers - what's the big deal?

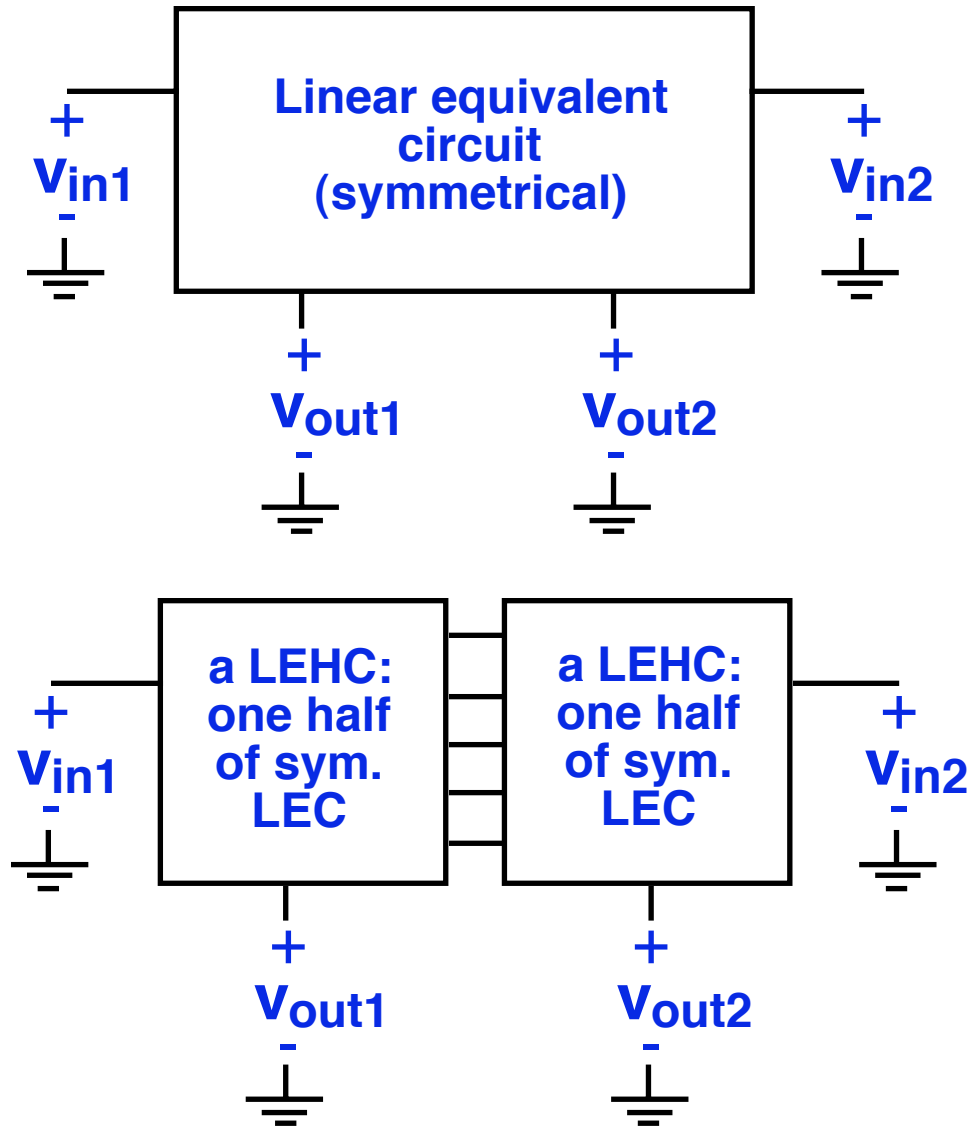
## Intrinsic advantages and features:

- large difference mode gain
- small common mode gain
- easy to cascade stages without coupling capacitors
- no emitter/source capacitor required in CE/CS stages

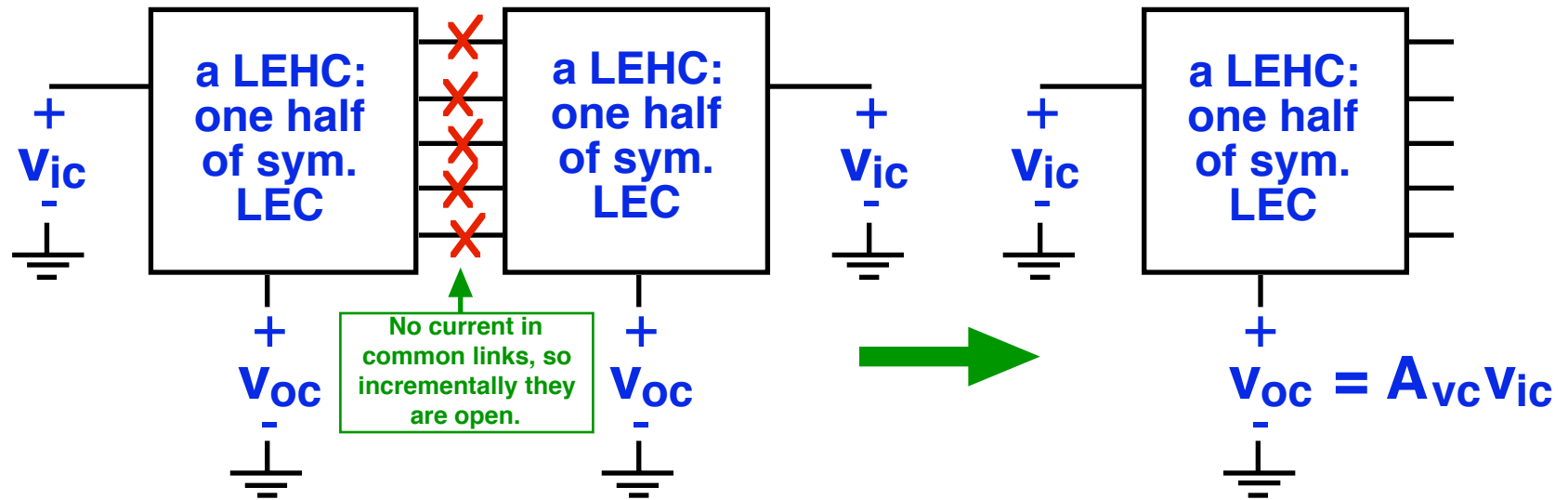
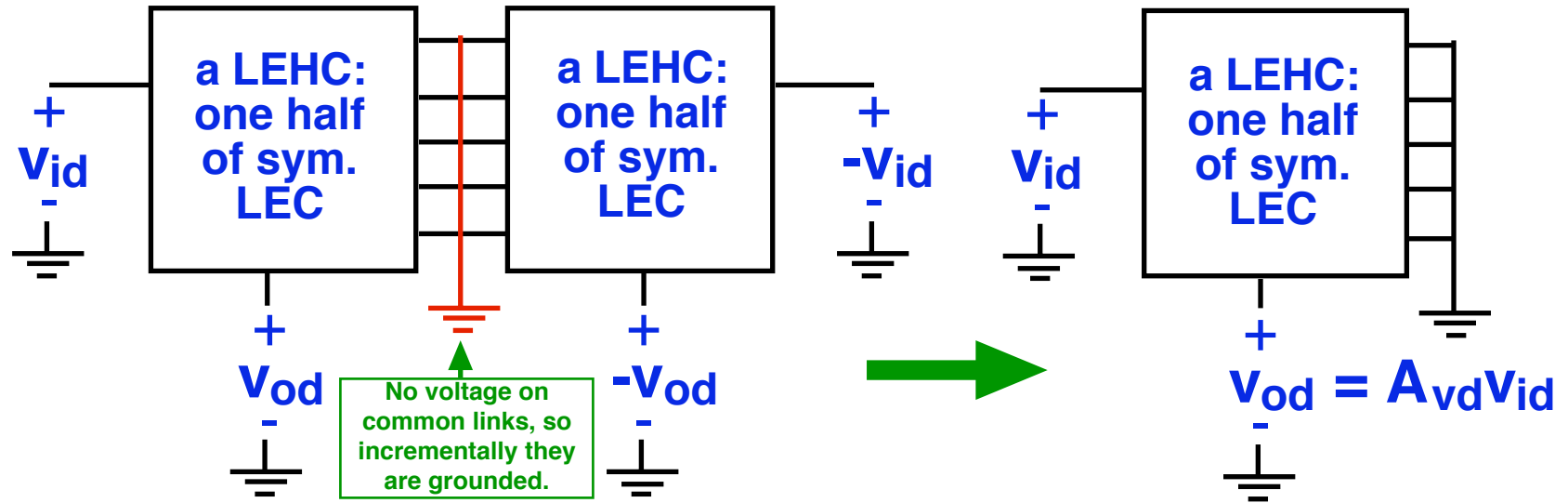
## Performance metrics:

- difference mode voltage gain,  $A_{vd}$
- common mode voltage gain,  $A_{vc}$
- common mode rejection ratio, CMRR
- input resistance,  $R_{in}$
- output resistance,  $R_{out}$
- common mode input voltage range
- output voltage swing
- DC offset on output

# Differential Amplifier Analysis - incremental analysis exploiting symmetry and superposition

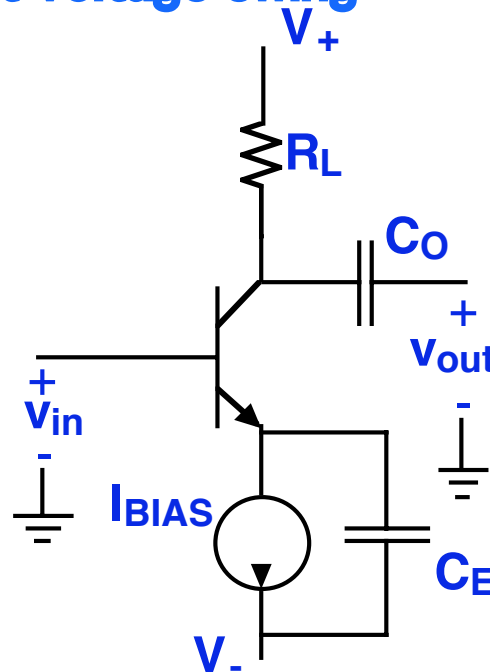


# Differential Amplifier Analysis - incremental analysis exploiting symmetry and superposition



# Resistor Loads: the limit on maximum gain

- linear resistor loads require a compromise between voltage gain and output voltage swing



## Maximum Voltage gain

$$\text{Bipolar: } |A_{v,\max}| = g_m R_L = \frac{qI_C R_L}{kT} \square \frac{[I_C R_L]_{\max}}{V_{\text{thermal}}}$$

$$\text{MOSFET*}: |A_{v,\max}| = g_m R_L = \frac{2I_D R_L}{[V_{GS} - V_T]} \square \frac{2[I_D R_L]_{\max}}{[V_{GS} - V_T]_{\min}}$$

What are  $[I_C R_L]_{\max}$ ,  $[I_D R_L]_{\max}$ , and  $[V_{GS} - V_T]_{\min}$  ?

## Resistor Loads: cont.

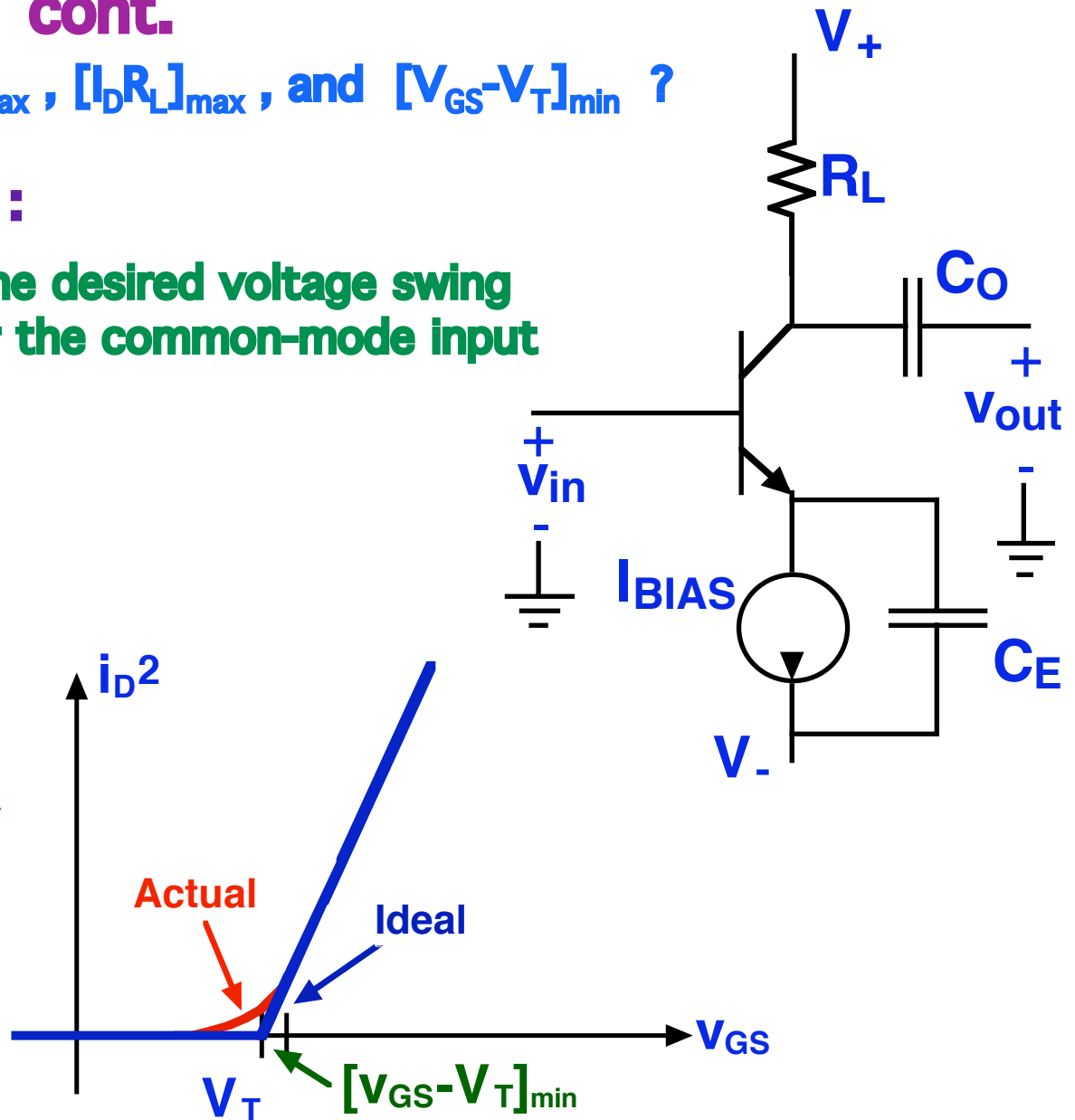
- What are  $[I_C R_L]_{\max}$ ,  $[I_D R_L]_{\max}$ , and  $[V_{GS} - V_T]_{\min}$  ?

$[I_C R_L]_{\max}$ ,  $[I_D R_L]_{\max}$  :

Determined by the desired voltage swing at output and/or the common-mode input voltage range

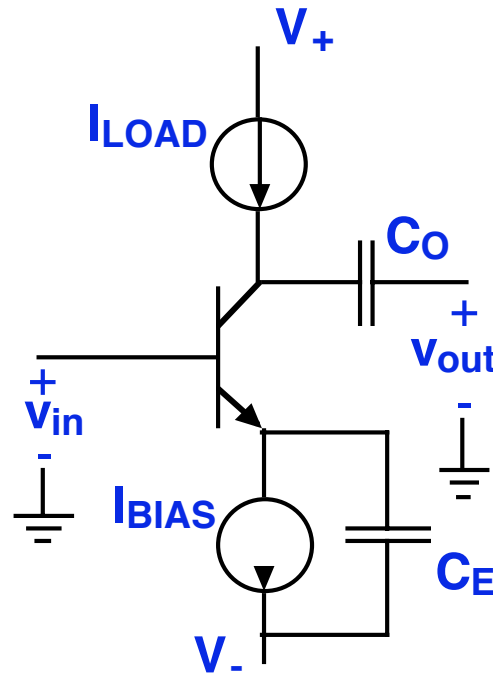
$[V_{GS} - V_T]_{\min}$  :

Determined by the process spread in  $V_T$ , and by how close to threshold the gate can safely be biased before the depletion approximation model fails.



# Current Source Loads: the limit on maximum gain

- current source loads eliminate the compromise between voltage gain and output voltage swing



## Maximum Voltage gain

$$\text{Bipolar: } |A_{v,\max}| = \frac{g_m}{g_{oL} + g_{oQ}} = \frac{qI_C/kT}{I_C/V_{AL} + I_C/V_{AQ}} = \frac{V_{A,\text{eff}}}{V_{\text{thermal}}}$$

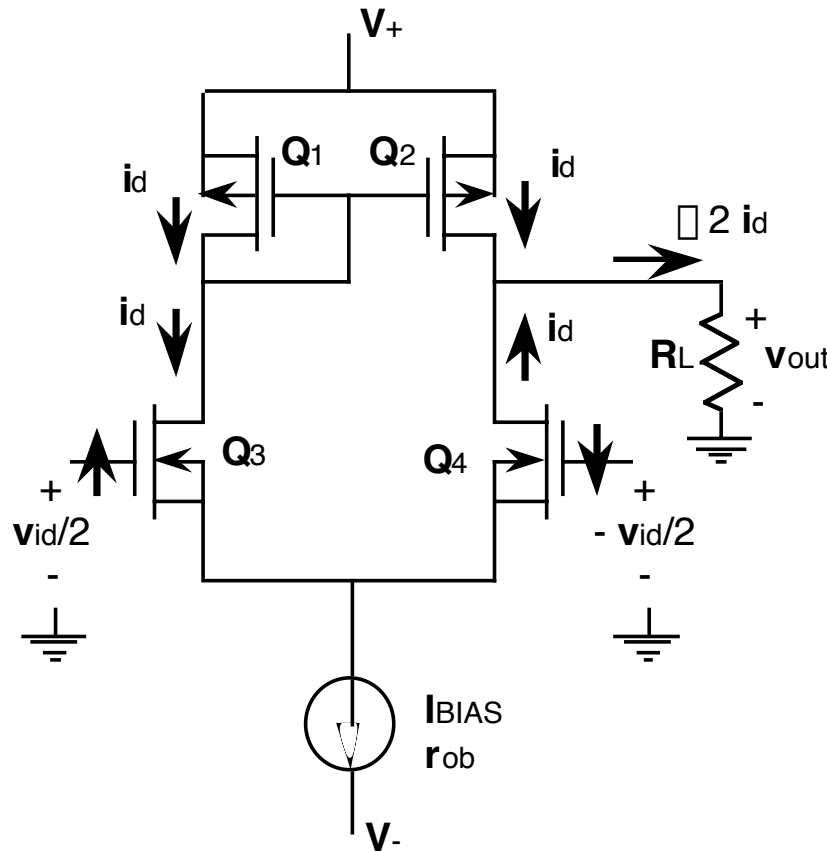
$$\text{MOSFET*}: |A_{v,\max}| = \frac{g_m}{g_{oL} + g_{oQ}} = \frac{2I_D/[V_{GS} - V_T]}{I_D/V_{AL} + I_D/V_{AQ}} \approx \frac{2V_{A,\text{eff}}}{[V_{GS} - V_T]_{\min}}$$

$$\text{with } V_{A,\text{eff}} \equiv \frac{V_{AL}V_{AQ}}{[V_{AL} + V_{AQ}]}$$

Typically  $V_{A,\text{eff}} \gg [I R_L]_{\max}$

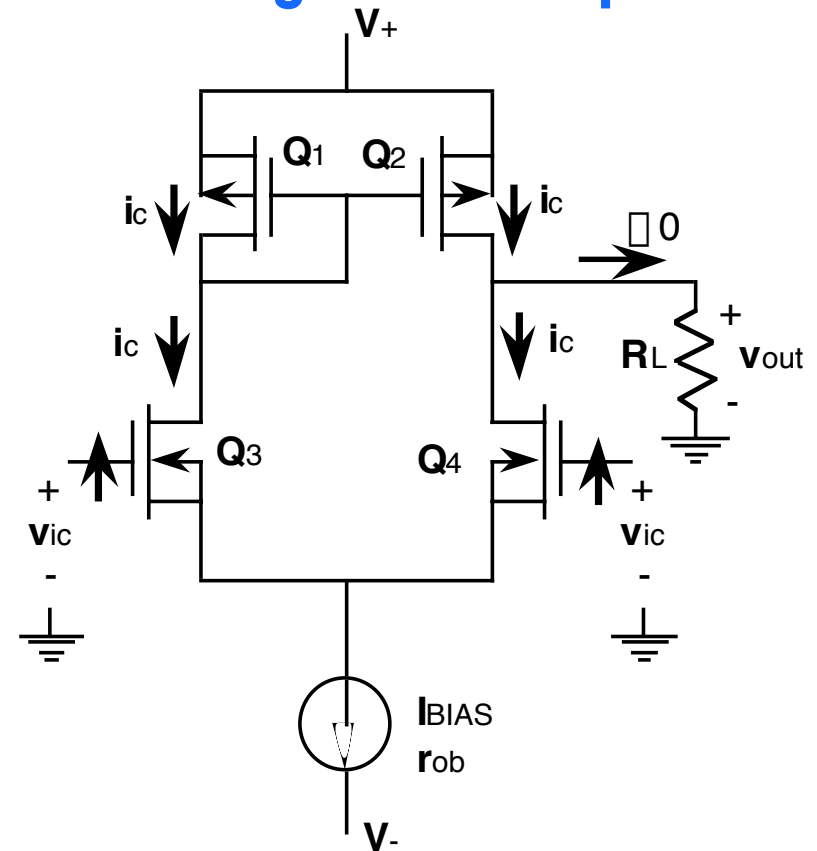
# Active Loads: The current mirror load

- large R in difference-mode and small R in common mode
- efficient conversion from double-ended to single-ended output



## Difference-mode inputs

$$v_{out} = [2g_{m3}/(g_{o2}+g_{o4}+G_L)]v_{id}/2$$



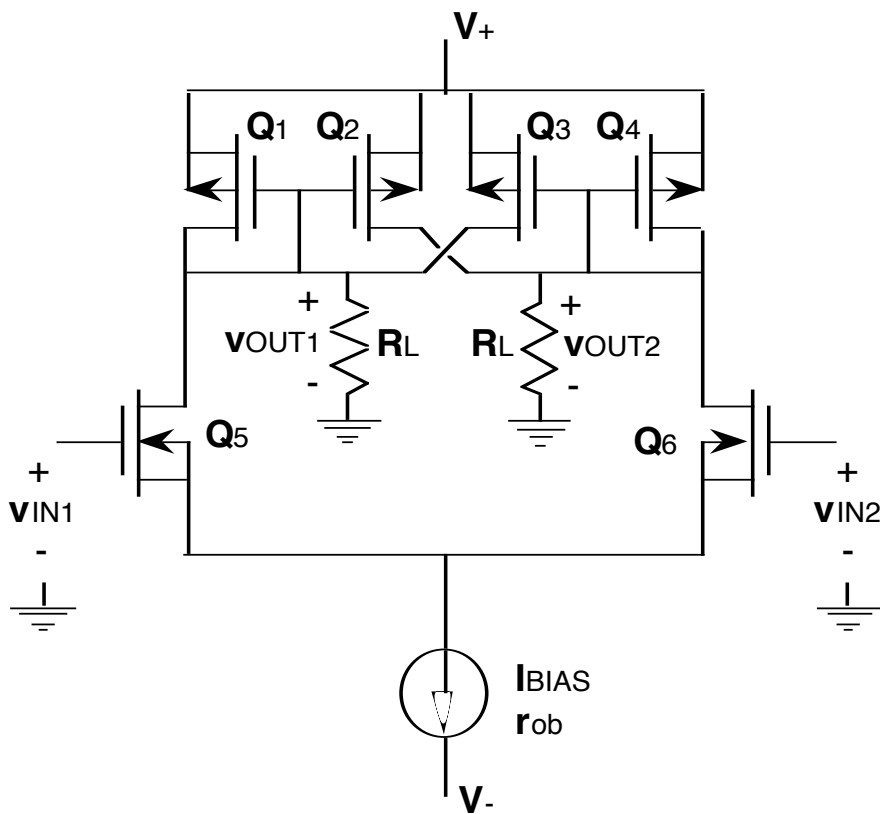
## Common-mode inputs

$$v_{out} = [g_{ob}/2(g_{m2}+g_{o4}+G_L)]v_{ic} \approx g_{ob}/2g_{m2}v_{ic}$$

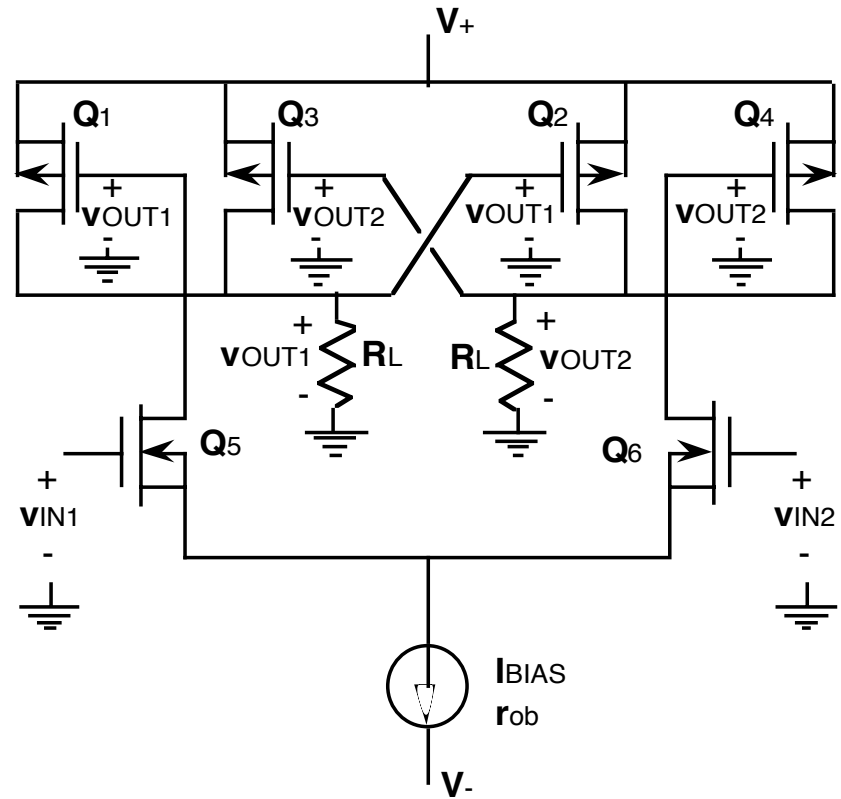
**With both inputs:**  $v_{out} \approx [2g_{m3}/(g_{o2}+g_{o4}+G_L)]v_{id}/2 + g_{ob}/2g_{m2}v_{ic}$

# Active Loads - The Lee load

a load for a fully-differential stage that looks like a large resistance in difference-mode and small resistance in common-mode

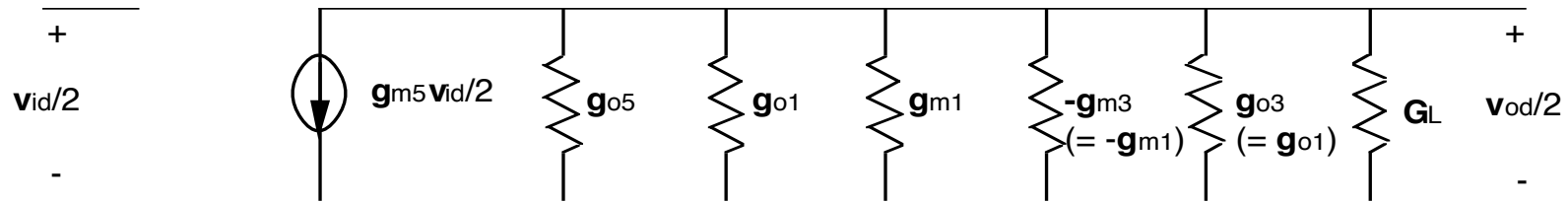
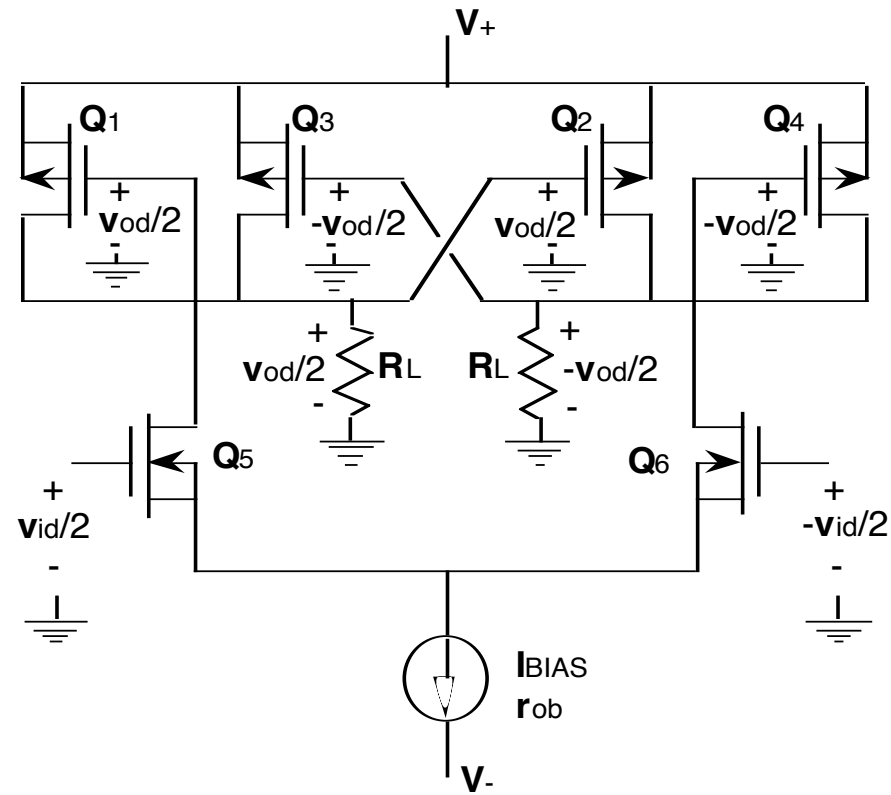


Normal format



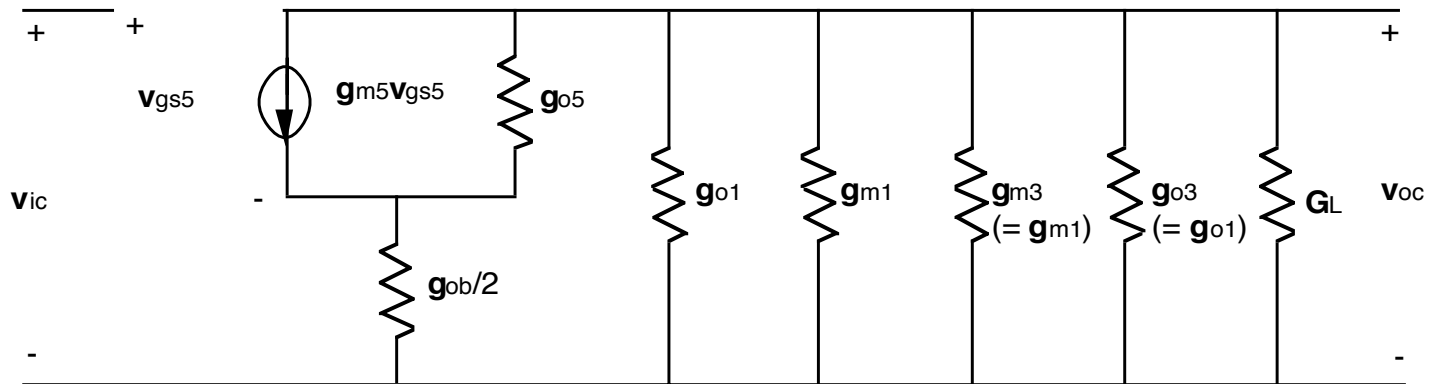
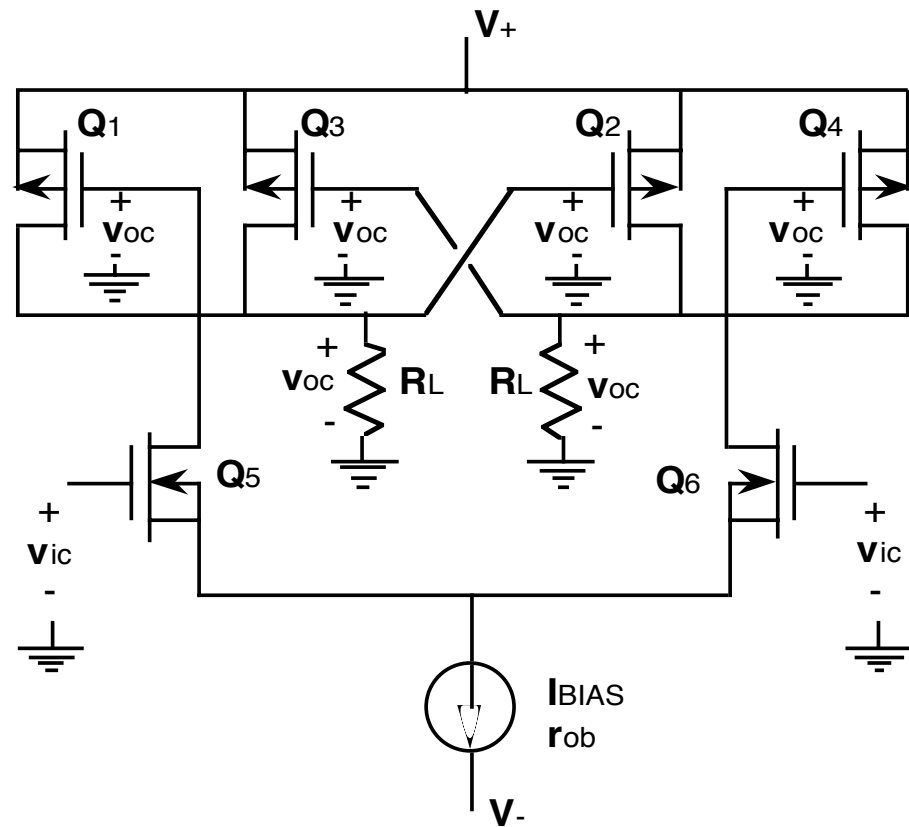
Drawn to highlight cross-coupling

**The Lee load:**  
analysis for  
difference-mode  
inputs



**Difference mode:**  $A_{vd} = v_{od}/v_{id} = g_{m5}/(g_{o5} + 2g_{o1} + G_L)$

**The Lee load:  
analysis for  
common-mode  
inputs**



**Common mode:**  $A_{vc} = v_{oc}/v_{ic} = g_{ob}/2(2g_{o1} + 2g_{m1} + G_L) \approx g_{ob}/4g_{m1}$

# Achieving the maximum gain: Comparing linear resistors, current sources, and active loads

## MAXIMUM GAIN

Linear resistor loads

Current source loads

Difference mode

Active loads

Common mode

Bipolar  
ipolar

$$\square \frac{[I_C R_L]_{\max}}{V_{thermal}}$$

$$\square \frac{2V_{A,eff}}{V_{thermal}}$$

$$\frac{V_{A,eff}}{V_{thermal}}$$

$$\frac{V_{thermal}}{V_{A,bias}}$$

$$V_{A,bias}$$

MOSFET

$$\square \frac{[I_D R_L]_{\max}}{[V_{GS} - V_T]_{\min}}$$

$$\square \frac{2V_{A,eff}}{[V_{GS} - V_T]_{\min}}$$

$$\frac{V_{A,eff}}{[V_{GS} - V_T]_{\min}}$$

$$\frac{[V_{GS} - V_T]_{\min}}{[V_{GS} - V_T]_{\min}}$$

$$\frac{[V_{GS} - V_T]_{\min}}{[V_{GS} - V_T]_{\min}}$$

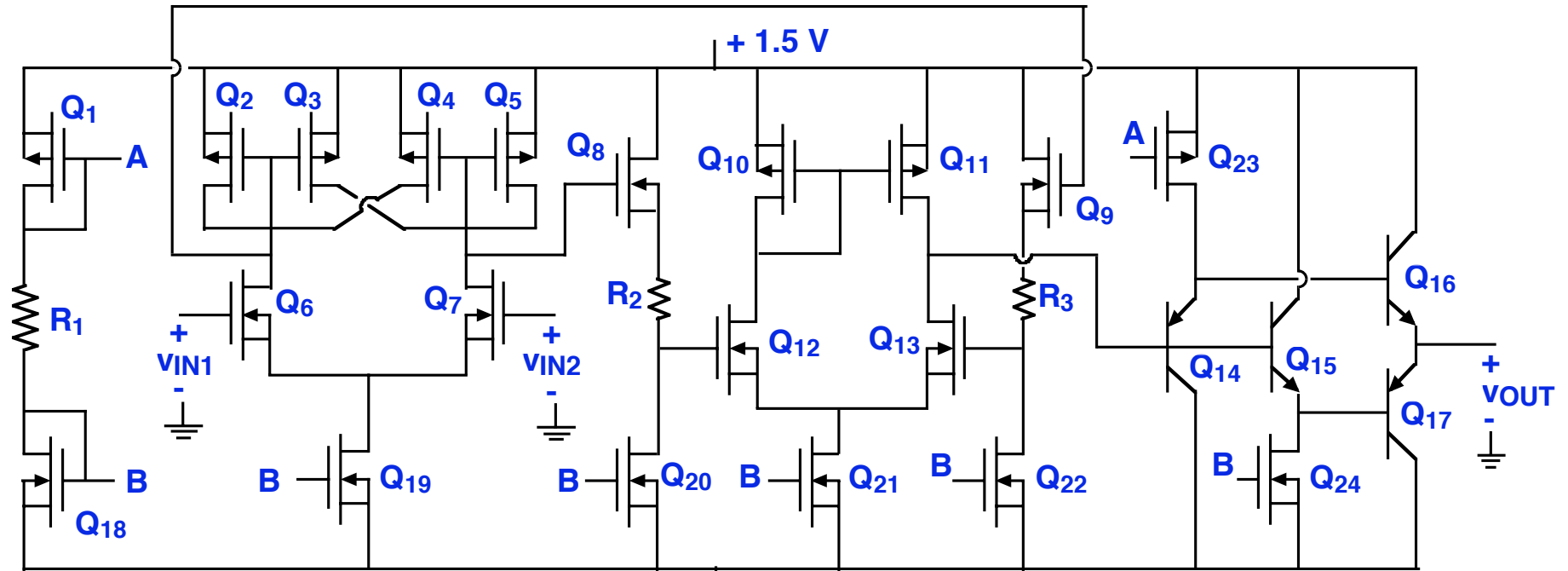
$$V_{A,bias}$$

## Observations:

- Non-linear (current source) loads typically yield higher gain than linear resistors, i.e.  $V_{A,eff} \gg [I_D R_L]_{\max}$
- Bias level is not important to BJT stage gain
- A MOSFET should be biased at low level for high gain
- For active loads what increases  $A_{vd}$ , decreases  $A_{vc}$

6.012 - Electronic Devices and Circuits  
**Fall 2003 Design Problem Circuit**

**Full schematic**



**Bias chain**

**Common-source  
gain stage with  
Lee load**

**Source-  
follower  
stage with  
degeneration  
to provide  
level shift**

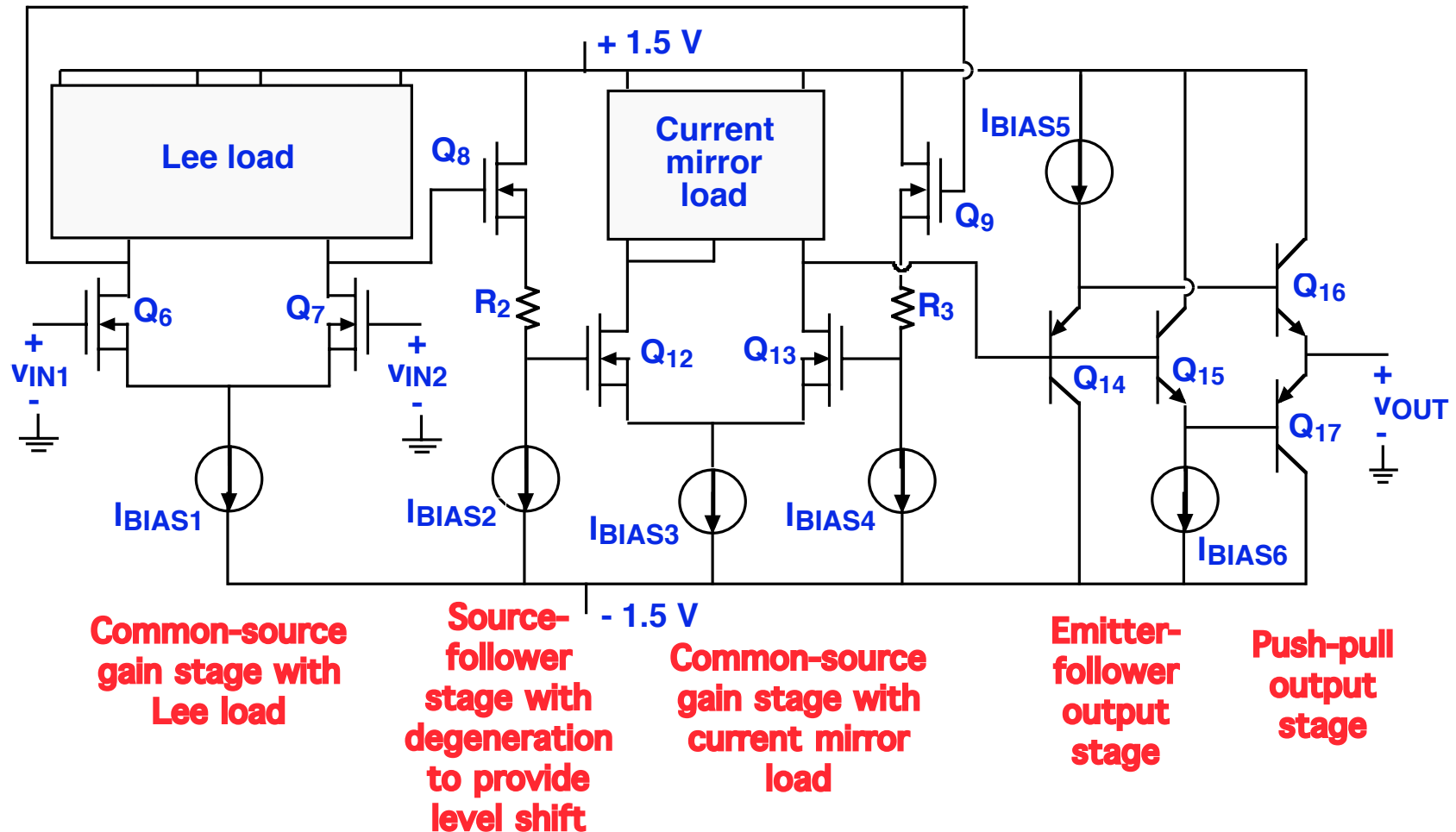
**Common-source  
gain stage with  
current mirror  
load**

**Emitter-  
follower  
output  
stage**

**Push-pull  
output  
stage**

6.012 - Electronic Devices and Circuits  
**Fall 2003 Design Problem Circuit**

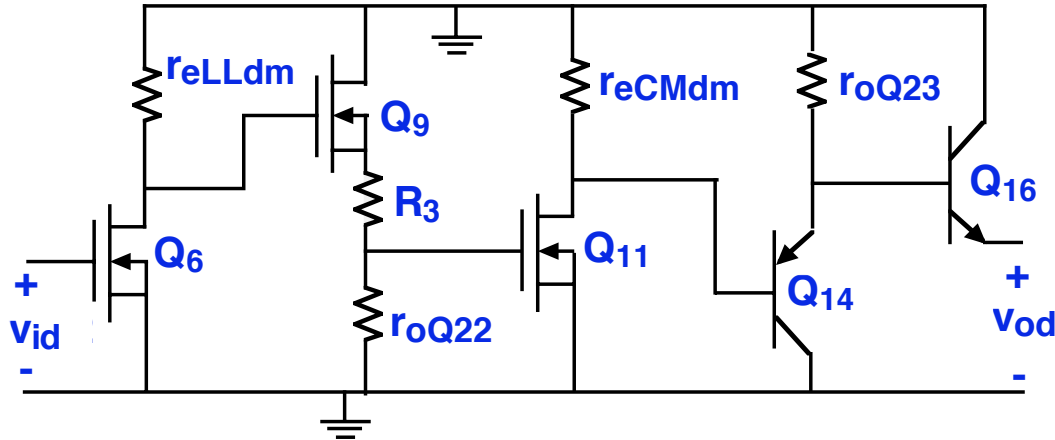
**Conceptual schematic: full circuit**



6.012 - Electronic Devices and Circuits  
**Fall 2003 Design Problem Circuit**

**Conceptual schematic**

**Difference-mode inputs**



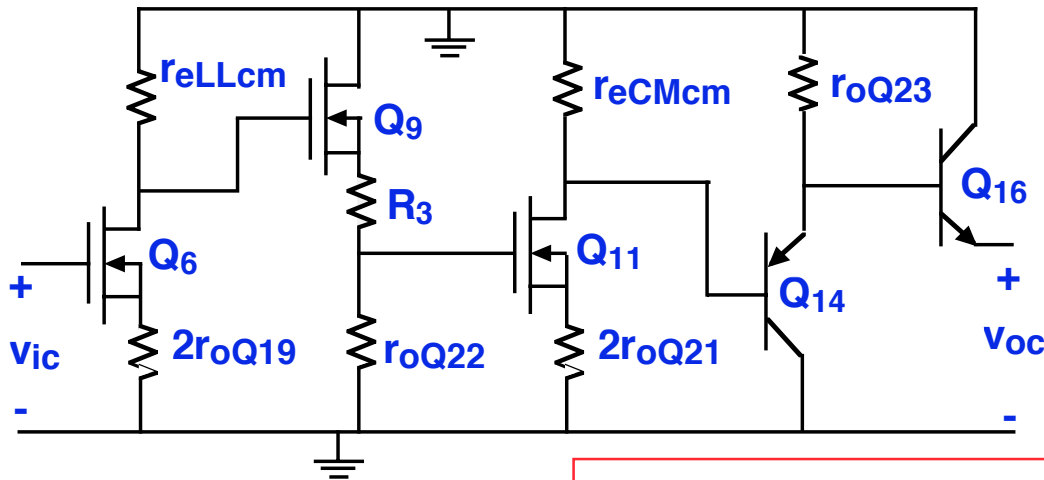
$$V_{in1} = V_{ic} + V_{id}/2$$

$$V_{in2} = V_{ic} - V_{id}/2$$

$$V_{out} = V_{oc} + V_{od}$$

$$V_{od} = A_{vd} V_{id}$$

**Common-mode inputs**



$$V_{oc} = A_{vc} V_{ic}$$

$$V_{out} = A_{vc} V_{ic} + A_{vd} V_{id}$$

## Lecture 20 - Linear Amp. Analysis and Design I - Summary

- **Performance metrics - specific to diff. amps.**
  - Difference- and common-mode gains:  $A_{vd} = v_{od}/v_{id}$ ,  $A_{vc} = v_{oc}/v_{ic}$
  - Common-mode rejection ratio:  $CMRR = A_{vd}/A_{vc}$
  - Input and output resistances
  - Common-mode input voltage swing
- **Non-linear loads**
  - Transistors biased in their constant current regions
    - BJTs in their FAR
    - MOSFETs in saturation
  - Optimum bias point for high gain: MOSFET at low  $I_D$ , BJT at any  $I_C$
- **Active loads**
  - Current mirror load
    - Achieves double- to single-ended conversion without loss of gain
    - Has high resistance for difference-mode signals
    - Has low resistance for common-mode signals
  - Lee Load
    - Maintains differential signals
    - Has high resistance for difference-mode signals
    - Has low resistance for common-mode signal