6.012 - Electronic Devices and Circuits

# Lecture 16 - Digital Circuits: CMOS - Outline

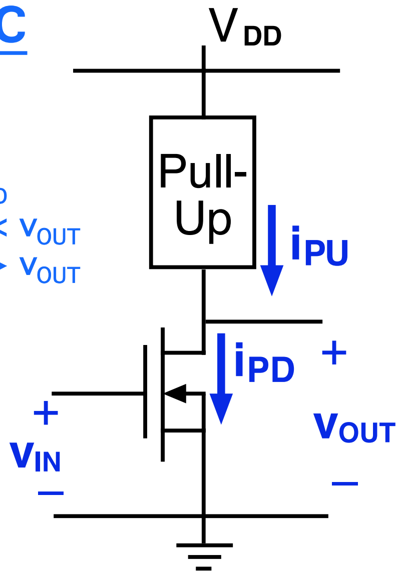
- **Announcements**
  - Handout; Web posting - Lecture Outline and Summary; two readings
  - Exam 2 - Wednesday, Nov. 5, 7:30-9:30 pm, Room 10-250; closed book
  - HSPICE - nice, but more useful when combined with insight and intuition
- **Review - Inverter performance metrics**
  - Transfer characteristic: logic levels and noise margins
  - Power: $P_{ave, static} + P_{ave, dynamic}$ $(= I_{ON} V_{DD}/2 + f\, C_L V_{DD}^{\,2})$
  - Switching speed: charge thru pull-up, discharge thru pull-down
    - If can model load as linear C: $dv_{OUT}/dt = i_{CH}(v_{OUT})/C_L;\ = i_{DCH}(v_{OUT})/C_L$
    - If can say $i_{CH}$, $i_{DCH}$ constant: $_{HI\text{-}LO} = C_L(V_{HI}-V_{LO})/I_{CH}$ ; $_{HI\text{-}LO} = C_L(V_{HI}-V_{LO})/I_{DCH}$
      (often only 10 to 90% swings)
  - Fan-out, fan-in
  - Manufacturability
- **CMOS**
  - Transfer characteristic
  - Gate delay expressions
  - Power and speed-power product
- **Digital circuits**
  - Multiple input CMOS gates: NAND and NOR
  - Output buffering
  - Memory cells

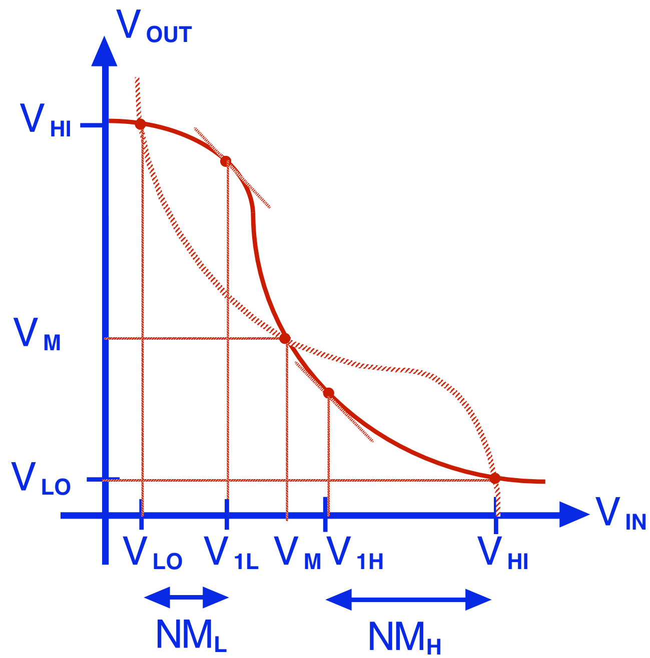
# Transfer characteristic

Node equation: $i_{PD} = i_{PU}$

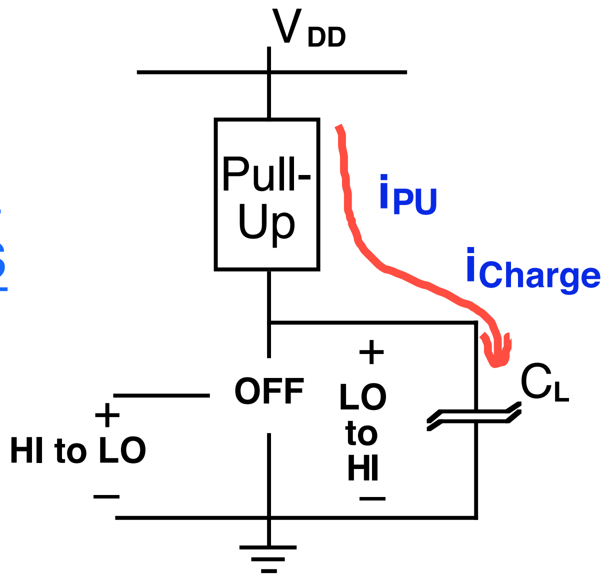
$$i_{PD} = \begin{cases} 0 & v_{IN} < V_{T,PD} \\ K_{PD}(v_{IN}-V_{T,PD})^2/2 & v_{IN}-V_{T,PD} < v_{OUT} \\ K_{PD}(v_{IN}-V_{T,PD}-v_{OUT}/2)\, v_{OUT} & v_{IN}-V_{T,PD} > v_{OUT} \end{cases}$$

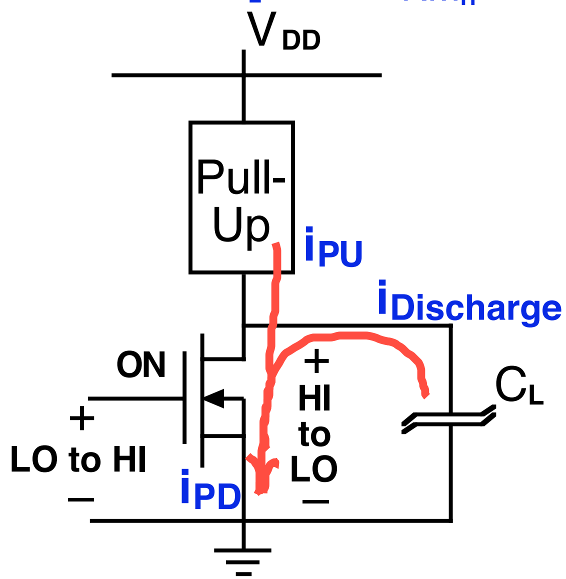
$i_{PU}$: Depends on the device used




# Switching transients



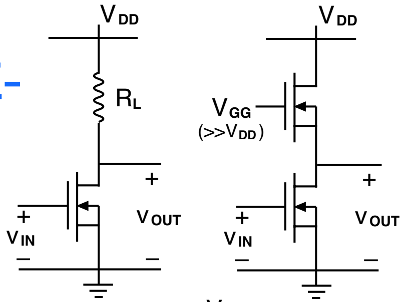



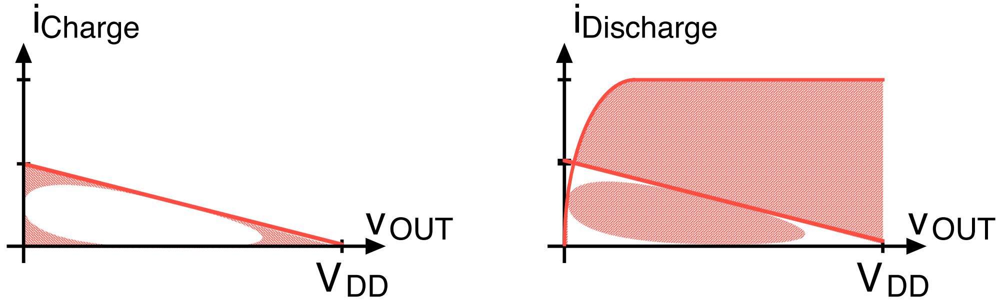

Charging cycle: $i_{Charge} = i_{PU}$

Discharging cycle: $i_{Discharge} = i_{PD} - i_{PU}$

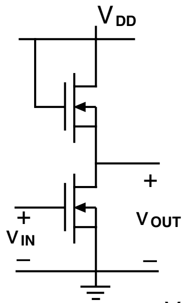
# Switching transients: summary of charge/discharge currents

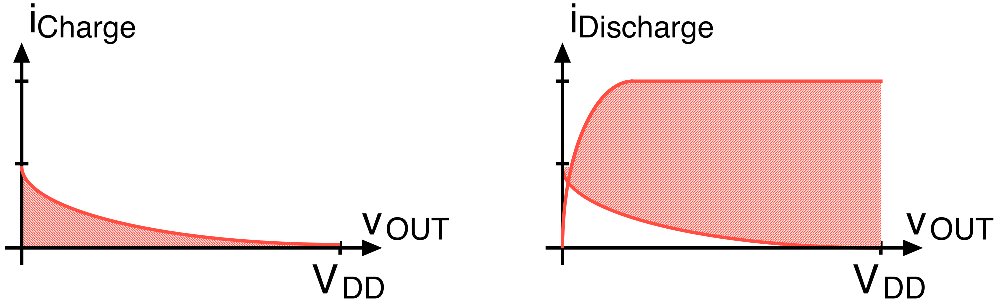
## Resistor and E-mode pull-up ($V_{GG}$ on gate)



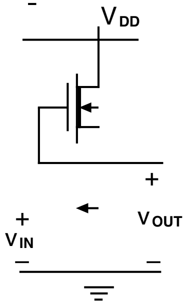



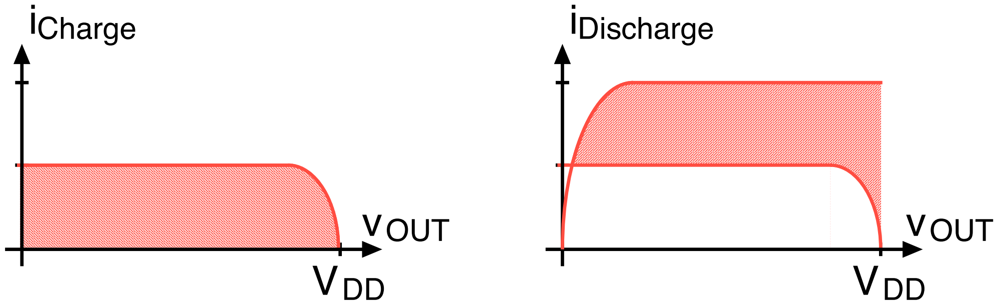

## E-mode pull-up ($V_{DD}$ on gate)



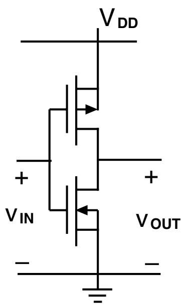



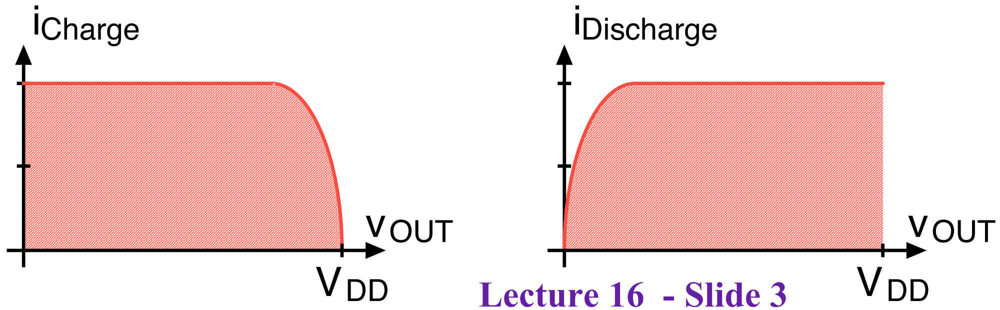

## D-mode pull-up (called "n-MOS")



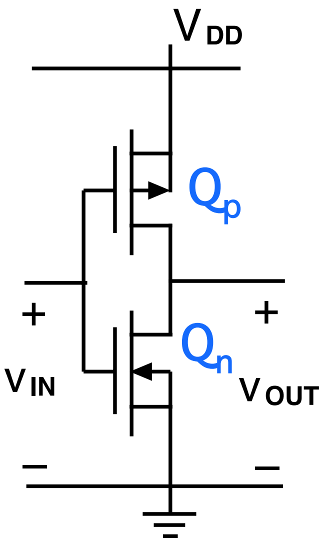



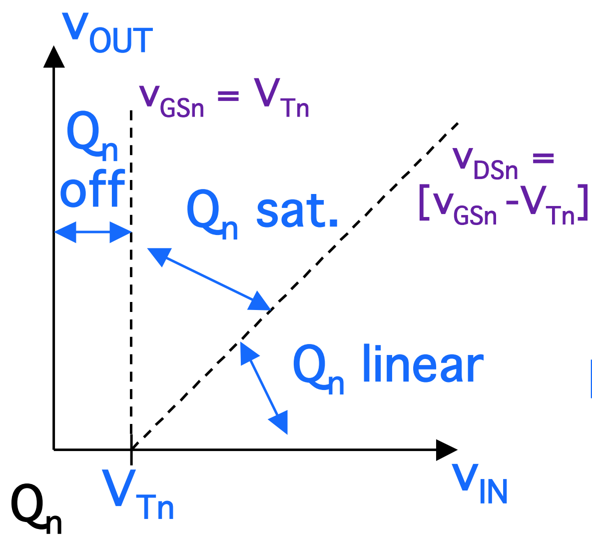

## CMOS

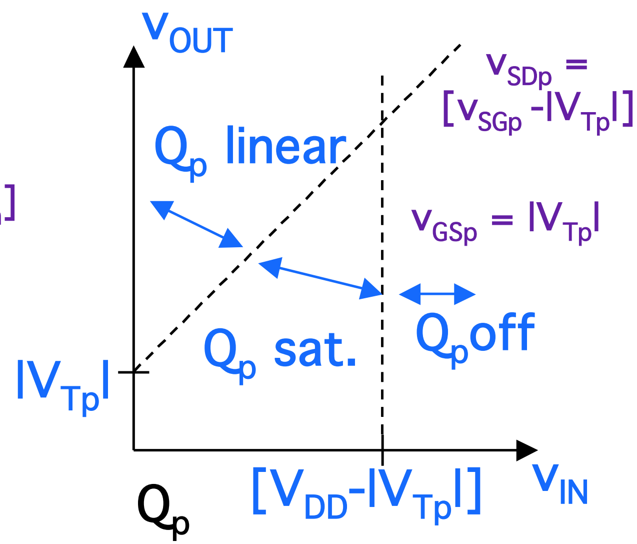


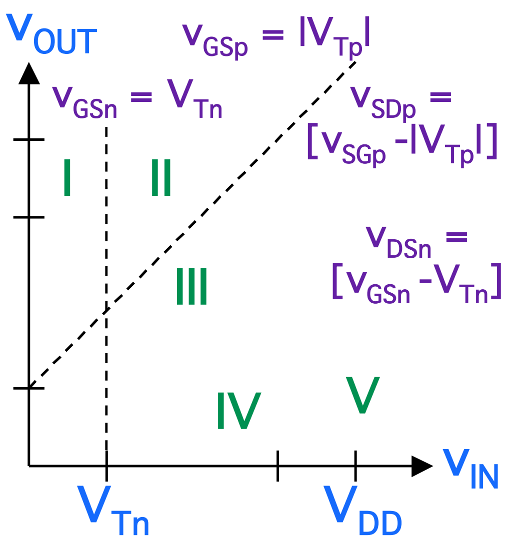



# CMOS: transfer characteristic calculation



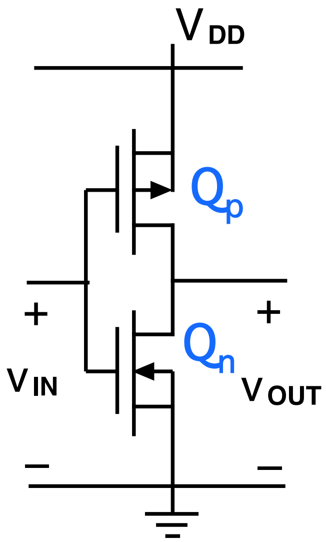



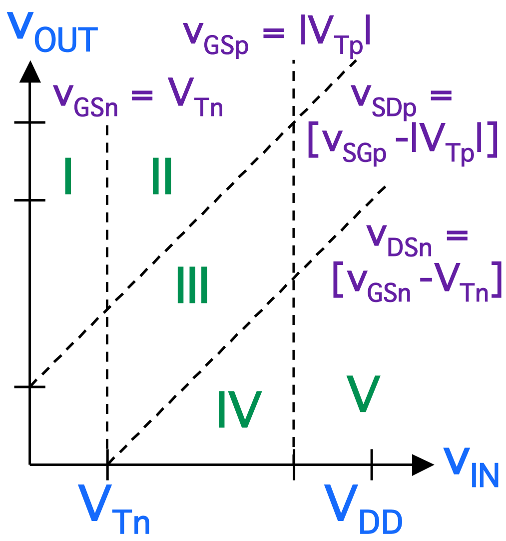




Transistor operating condition in each region:

| Region | $Q_n$ | $Q_p$ |
|---|---|---|
| I | cut-off | linear |
| II | saturation | linear |
| III | saturation | saturation |
| IV | linear | saturation |
| V | linear | cut-off |

# CMOS: transfer characteristic calculation, cont.




**Region I:**

$$i_{Dn} = 0 \quad \text{and} \quad i_{Dp} = K_p \; V_{DD} \quad v_{IN} \quad \left|V_{Tp}\right| \quad \frac{(V_{DD} \quad v_{OUT})}{2} (V_{DD} \quad v_{OUT})$$

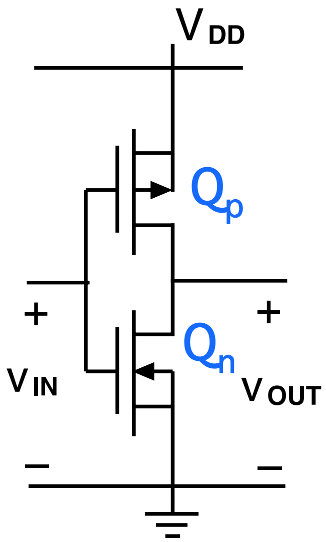
$$i_{Dn} = i_{Dp} \qquad v_{OUT} = V_{DD}$$

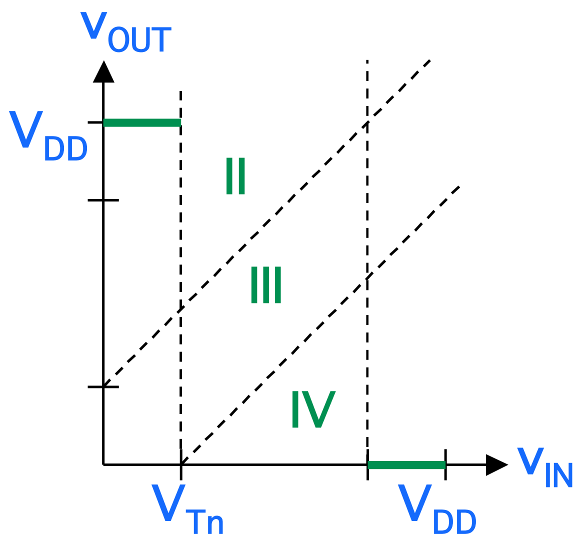
**Region V:**

$$i_{Dn} = K_n \; v_{IN} \quad V_{Tn} \quad \frac{v_{OUT}}{2} v_{OUT} \quad \text{and} \quad i_{Dp} = 0$$

$$i_{Dn} = i_{Dp} \qquad v_{OUT} = 0$$

# CMOS: transfer characteristic calculation, cont.




**Region III:**

$$i_{Dn} = \frac{K_n}{2}\left[v_{IN} - V_{Tn}\right]^2 \quad \text{and} \quad i_{Dp} = \frac{K_p}{2}\left[V_{DD} \quad v_{IN} \quad \left|V_{Tp}\right|\right]^2$$

$$i_{Dn} = i_{Dp} \qquad v_{IN} = \frac{V_{DD} \quad \left|V_{Tp}\right| + V_{Tn}\sqrt{K_n/K_p}}{1+\sqrt{K_n/K_p}}$$

To achieve symmetry, make $K_p = K_n$ and $\left|V_{Tp}\right| = V_{Tn}$

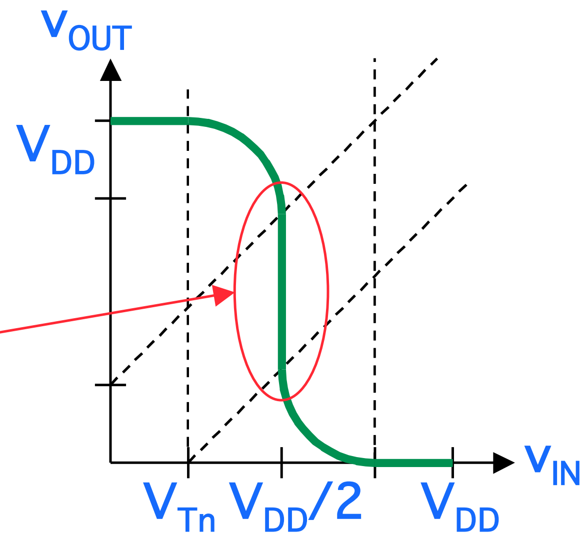
With this: $v_{IN} = \frac{V_{DD}}{2}$ and $\frac{V_{DD}}{2} - V_{Tn} \quad v_{OUT} \quad \frac{V_{DD}}{2} + \left|V_{Tp}\right|$

**Regions II and IV:** Parabolic sections connecting smoothly with straight line sections (see course text).

# CMOS: transfer characteristic calculation, cont.

Our calculation says that the transfer characteristic is vertical in Region III.

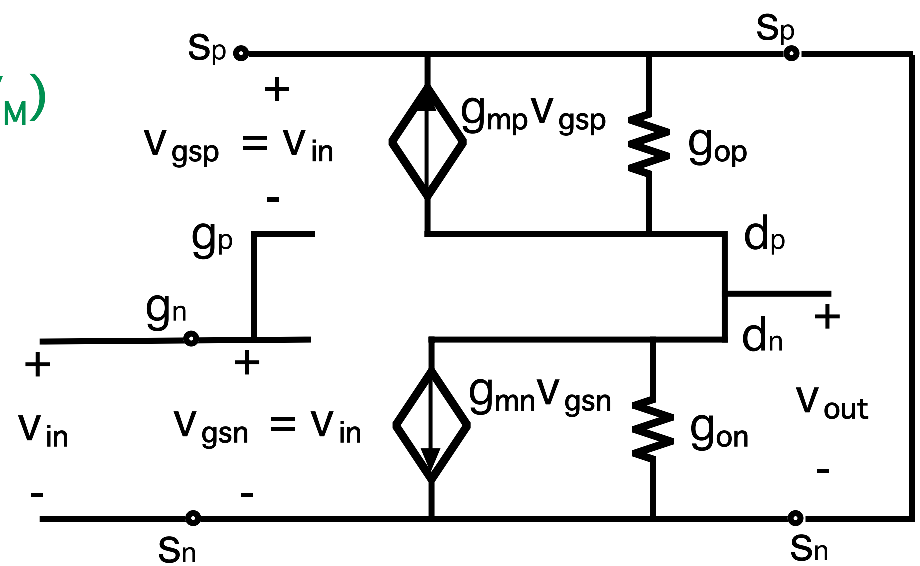
We know it will have some slope, but what is it?




To see, calculate the small signal gain about the bias point:

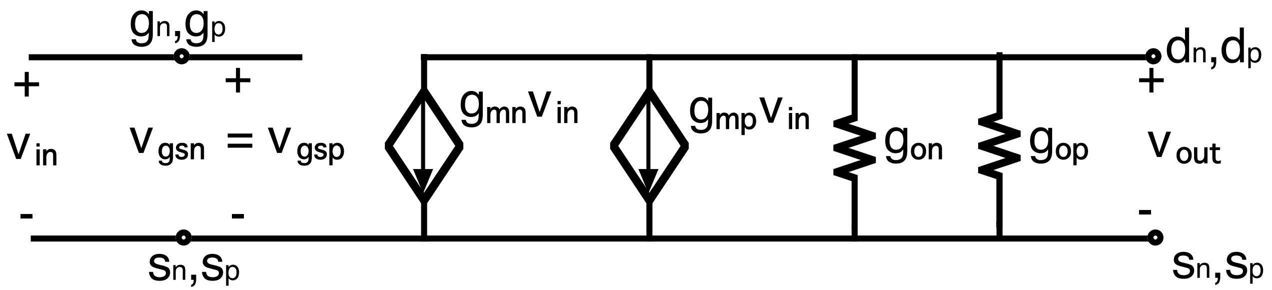
$V_{IN} = V_{OUT} = V_{DD}/2\ (= V_M)$

Begin with the small signal model:



# CMOS: transfer characteristic calculation, cont.

Redrawing the circuit, we get




from which we see immediately that:

$$A_v \equiv \left.\frac{\partial v_{OUT}}{\partial v_{IN}}\right|_Q = \frac{v_{out}}{v_{in}} = \frac{[g_{mn} + g_{mp}]}{[g_{on} + g_{op}]}$$

Writing the conductances in terms of the bias point, as

$$g_{mn} = \sqrt{2K_n I_{Dn}}, \quad g_{mp} = \sqrt{2K_p |I_{Dp}|} = g_{mn}, \quad g_{on} = \;_n I_{Dn}, \quad g_{op} = \;_p I_{Dp} = \;_p I_{Dn}$$

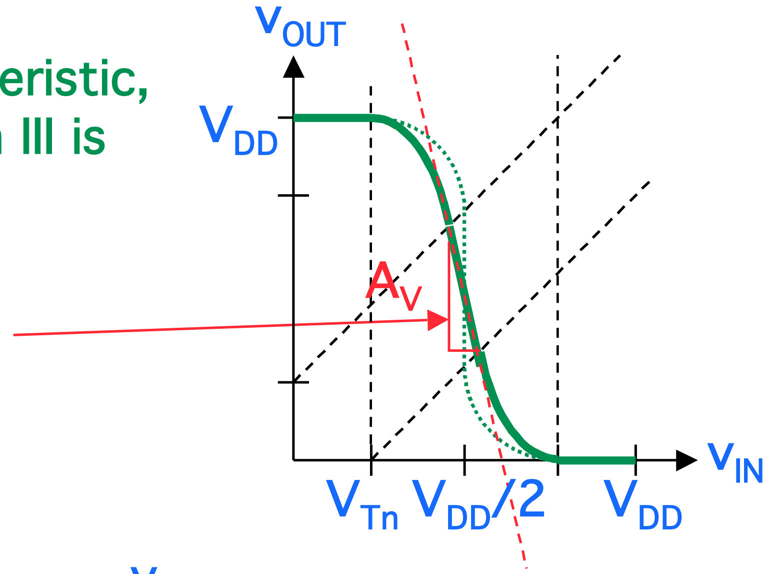
we get our final result:

$$A_v \equiv \left.\frac{\partial v_{OUT}}{\partial v_{IN}}\right|_Q = \frac{2\sqrt{2K_n I_{Dn}}}{[\;_n + \;_p] I_{Dn}} = \frac{2\sqrt{2K_n}}{[\;_n + \;_p]\sqrt{I_{Dn}}}$$

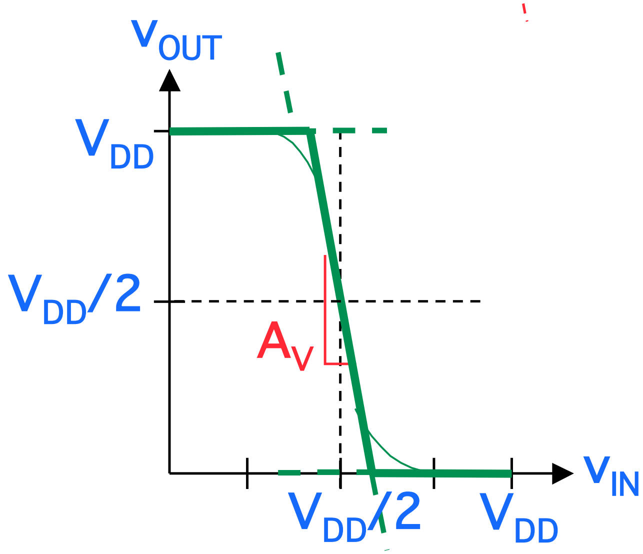
# CMOS: transfer characteristic calculation, cont.

Returning to the transfer characteristic, we see that the slope in Region III is not infinite, but is instead:

$$A_v \equiv \left.\frac{\partial v_{OUT}}{\partial v_{IN}}\right|_Q = \frac{2\sqrt{2K_n}}{\left[\ _n + \ _p\right]\sqrt{I_{Dn}}}$$




Final comment: A quick and dirty way to approximate the transfer curve of a CMOS gate is to simply draw the three straight line portions in Regions I, III, and V:



# CMOS: switching speed; minimum cycle time

## The load capacitance, $C_L$

- Assume to be linear
- Is proportional to MOSFET gate area
- In channel: $\mu_e = 2\,\mu_h$ so to have $K_n = K_p$ we must have $W_p/L_p = 2W_n/L_n$
  Typically $L_n = L_p = L_{min}$, and $W_n = W_{min}$, so we also have $W_p = 2\,W_{min}$.

$$C_L \quad n\left[W_n L_n + W_p L_p\right] C_{ox}^* = n\left[W_{\min} L_{\min} + 2W_{\min} L_{\min}\right] C_{ox}^* = 3\,n\,W_{\min} L_{\min}\, C_{ox}^*$$

## Charging cycle

$v_{IN}$: Hi to Lo; $Q_n$ off, $Q_p$ on; $v_{OUT}$: Lo to Hi

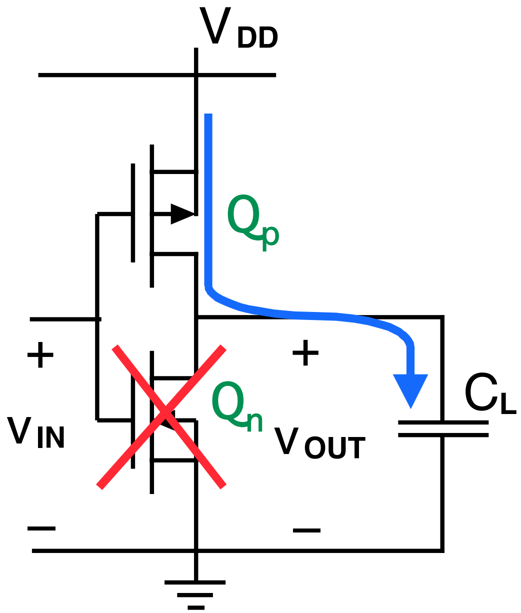
- Assume charged by constant $i_{D,sat}$

$$i_{Charge} = i_{Dp} \quad \frac{K_p}{2}\left[V_{DD} \quad \left|V_{Tp}\right|\right]^2 = \frac{K_n}{2}\left[V_{DD} \quad V_{Tn}\right]^2$$

$$q_{Charge} = C_L\, V_{DD}$$

$$_{Charge} = \frac{q_{Charge}}{i_{Charge}} = \frac{2\,C_L\,V_{DD}}{K_n\left[V_{DD} \quad V_{Tn}\right]^2}$$

$$= \frac{6\,n\,W_{\min} L_{\min} C_{ox}^* V_{DD}}{\frac{W_{\min}}{L_{\min}} \quad {}_e C_{ox}^*\left[V_{DD} \quad V_{Tn}\right]^2} = \frac{6\,n\,L_{\min}^2 V_{DD}}{{}_e\left[V_{DD} \quad V_{Tn}\right]^2}$$



# <u>CMOS</u>: switching speed; minimum cycle time, cont.

## Discharging cycle

$v_{IN}$: Lo to Hi; $Q_n$ on, $Q_p$ off; $v_{OUT}$: Hi to Lo

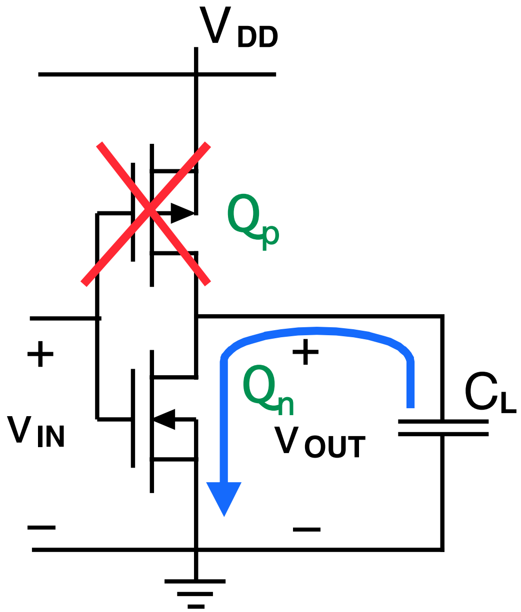
- Assume discharged by constant $i_{D,sat}$

$$i_{Discharge} = i_{Dn} \quad \frac{K_n}{2}[V_{DD} \quad V_{Tn}]^2$$

$$q_{Discharge} = C_L V_{DD}$$

$$_{Discharge} = \frac{q_{Discharge}}{i_{Discharge}} = \frac{2 C_L V_{DD}}{K_n [V_{DD} \quad V_{Tn}]^2}$$

$$= \frac{6 n W_{min} L_{min} C^*_{ox} V_{DD}}{\frac{W_{min}}{L_{min}} \; _e C^*_{ox} [V_{DD} \quad V_{Tn}]^2} = \frac{6 n L^2_{min} V_{DD}}{_e [V_{DD} \quad V_{Tn}]^2}$$




## Minimum cycle time

$v_{IN}$: Lo to Hi to Lo; $v_{OUT}$: Hi to Lo to Hi

$$_{Min.Cycle} = \; _{Charge} + \; _{Discharge} \quad \frac{12 n L^2_{min} V_{DD}}{_e [V_{DD} \quad V_{Tn}]^2}$$

# CMOS: power dissipation - total and per unit area

## Average power dissipation

All dynamic

$$P_{ave} = C_L V_{DD}^2 f = 3 n W_{\min} L_{\min} C_{ox}^* V_{DD}^2 f$$

## Average power at maximum data rate

Maximum f will be 1/ $_{\text{Min Cycle}}$

$$P_{ave @ Max.f} = 3 n W_{\min} L_{\min} C_{ox}^* V_{DD}^2 \frac{{}_e [V_{DD} \quad V_{Tn}]^2}{12 n L_{\min}^2 V_{DD}}$$

$$= \frac{1}{4} \frac{W_{\min}}{L_{\min}} {}_e C_{ox}^* V_{DD} [V_{DD} \quad V_{Tn}]^2 = \frac{1}{4} K_n V_{DD} [V_{DD} \quad V_{Tn}]^2$$

## Average power density at maximum data rate

Assume that the area per inverter will be proportional to $W_{min}L_{min}$

$$PD_{ave @ Max.f} = \frac{P_{ave @ Max.f}}{\text{Inverter area}} \mu \frac{P_{ave @ Max.f}}{W_{\min} L_{\min}} = \frac{{}_e C_{ox}^* V_{DD} [V_{DD} \quad V_{Tn}]^2}{4 L_{\min}^2}$$

# CMOS: design for high speed

## Maximum data rate

Proportional to 1/ $_{\text{Min Cycle}}$

$$f_{max}\ \mu\ 1/\ \ _{Min.Cycle} = \frac{\ _e\,[V_{DD}\quad V_{Tn}]^2}{12\,n\,L_{min}^2 V_{DD}}$$

Teaches us to make $L_{min}$ small and/or $V_{DD}$ large

**Note:** As we reduce $L_{min}$ we must also reduce $t_{ox}$, but $t_{ox}$ doesn't enter directly in $f_{max}$ so it doesn't impact us here.

## Average power density at maximum data rate

Assumes area per inverter is proportional to $W_{min}L_{min}$

$$PD_{ave@Max.f} = \frac{P_{ave@Max.f}}{\text{Inverter area}}\ \mu\ \frac{P_{ave@Max.f}}{W_{min}L_{min}} = \frac{\ _e\quad _{ox} V_{DD}\,[V_{DD}\quad V_{Tn}]^2}{4\ t_{ox}\ L_{min}^2}$$

Teaches us PD increases very quickly as we reduce $L_{min}$ unless we also reduce $V_{DD}$ (which reduces $f_{max}$).

**Note:** Now $t_{ox}$ appears so the impact of reducing $L_{min}$, and therefore also $t_{ox}$, is even more dramatic!

How do we make $f_{max}$ larger without melting the silicon?
Through CMOS scaling rules - the topic of Lecture 25.

# Lecture 16 - Digital Circuits: CMOS - Summary

- **CMOS**

**Transfer characteristic: symmetric**

$V_{LO} = 0$, $V_{HI} = V_{DD}$, $I_{ON} = 0$

$N_{ML} = N_{MH}$ implies $K_n = K_p$, $|V_{Tp}| = V_{Tn} \equiv V_T$

$L_n = L_p = L_{min}$, $W_p = (\ _e/\ _h)W_n$

**Gate delay expressions**

$_{LO\text{-}HI} = \ _{HI\text{-}LO} = 2V_{DD}C_L/K_n(V_{DD} - V_T)^2$

Gate delay (GD) $= \ _{LO\text{-}HI} + \ _{HI\text{-}LO} = 4V_{DD}C_L/K_n(V_{DD} - V_T)^2$

If $C_L = n(W_nL_n + W_pL_p)C_{ox}^* = 3n\ W_nL_{min}C_{ox}^*$ (Assumes $_n = 2\ _p$)

then $GD = 12\ n\ L_{min}^2\ V_{DD}/\ _e(V_{DD} - V_T)^2$ (Shows merit of reducing $L_{min}$)

**Power and speed-power product**

$P_{ave} = f\ C_L V_{DD}^{\ 2}$

$P_{ave}$@max. $f\ \mu\ C_L V_{DD}^2/GD = K_n V_{DD}(V_{DD} - V_T)^2/4$ (Shows merit of reducing $V_{DD}$)

(NOTE: We will return to CMOS design trade-offs and scaling rules in Lecture 25)

- **Digital circuits**

**Multiple input CMOS gates:**

NOR: n-channels in series, p-channels in parallel

NAND: p-channels in series, n-channels in parallel

**Output buffering** (Problem 3 on PS #8)

**Memory cells** (Check out Sec. 15.4)