

YOUR NAME \_\_\_\_\_

*Department of Electrical Engineering and Computer Science  
Massachusetts Institute of Technology*

## **6.012 Electronic Devices and Circuits**

### **FINAL EXAMINATION**

**Open book.**

Notes:

1. Unless otherwise indicated, assume room temperature and that  $kT/q$  is 0.025 V.
2. This test is designed so that most parts can be worked independently of the others.
3. All of your answers and any relevant work must appear on these pages. Any additional paper you hand in will not be graded.
4. Make reasonable approximations and assumptions. State and justify any such assumptions and approximations.
5. Be certain that you have all fifteen (15) pages of this exam booklet and make certain that you write your name at the top of this page in the space provided.
6. Your final grade can be obtained after 9 am Friday, December 22. You may see your final exam beginning January 8, 1996.

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For staff use only

Problem 1	_____
Problem 2	_____
Problem 3	_____
Problem 4	_____
Problem 5	_____

**TOTAL**

**Problem 1** (20 points)

Warm-up questions, 2 points each subsection (i.e. i, ii, etc.):

a) A specimen of gallium arsenide, GaAs, is doped with  $10^{16} \text{ cm}^{-3}$  zinc atoms replacing gallium in the lattice and  $5 \times 10^{16} \text{ cm}^{-3}$  selenium atoms replacing arsenic. In GaAs  $n_i$  is  $10^7 \text{ cm}^{-3}$  at 300 K.

i) What are the equilibrium carrier concentrations,  $n_0$  and  $p_0$ , in this sample at room temperature?

$$n_0 = \underline{\hspace{2cm}}$$

$$p_0 = \underline{\hspace{2cm}}$$

ii) What is the electrostatic potential,  $\phi$ , in this sample at room temperature relative to intrinsic gallium arsenide.

$$\phi = \underline{\hspace{2cm}}$$

b) A n-type silicon sample ( $\mu_e = 1500 \text{ cm}^2/\text{V-s}$ ,  $\mu_h = 600 \text{ cm}^2/\text{V-s}$ ,  $n_i = 10^{10} \text{ cm}^{-3}$ ) with equilibrium carrier concentrations  $n_0 = 10^{15} \text{ cm}^{-3}$  and  $p_0 = 10^5 \text{ cm}^{-3}$  is illuminated with an intense light generating  $G$  hole-electron pairs/ $\text{cm}^3\text{-s}$  throughout its bulk such that  $n' = p' = 10^{17} \text{ cm}^{-3}$ .

i) What is the thermal equilibrium conductivity,  $\sigma_0$ , of this sample?

$$\sigma_0 = \underline{\hspace{2cm}}$$

ii) What is the conductivity,  $\sigma$ , of the illuminated sample?

$$\sigma = \underline{\hspace{2cm}}$$

iii) How (approximately) are  $n'$  and  $p'$  related to  $G$ ? Explain.

$$n', p' \propto \sqrt{G}$$

$$n', p' \propto G$$

$$n', p' \propto G^2$$

Because

**Problem 1 continues on the next page.**

### Problem 1 continued

c) When we want a diode in an bipolar integrated circuit, we use one of the junctions in an npn transistor. Consider a BJT with  $N_{DE} = 10 N_{AB} = 100 N_{DC}$ ,  $w_E = w_B = 0.2 w_C$ ,  $\tau_e = 2.5 \tau_h$ ,  $I_{CS} = 10^2 I_{ES}$ , and  $\beta_F = 100$ .

i) Which junction should be used to get the largest reverse breakdown voltage, and why?

Emitter-base      Collector-base,      because:

ii) Which junction has the greatest minority carrier storage with a forward bias of 0.6 V? Explain your answer.

Emitter-base      Collector-base,      because:

iii) What is the bias on the collector-base junction if the emitter-base junction is forward biased and the collector terminal is open-circuited?

Forward bias      Reverse bias      Zero bias,      because:

d) You are in charge of a CMOS fabrication line and you have a problem because the thresholds of your n- and p-channel devices, which are supposed to be +1 V and -1 V, respectively, are turning out to be +3 V and +1 V, respectively instead. You suspect the interface between the silicon and the 40 nm thick oxide is contaminated by ions.

i) What type of device is each transistor with its new threshold?

p-channel MOSFET:      Enhancement-mode      Depletion-mode

n-channel MOSFET:      Enhancement-mode      Depletion-mode

ii) If you are right about the ions being the problem, what sign must they have, and what is their sheet density? Use  $\epsilon_{ox} = 3.5 \times 10^{-13} \text{ F/cm}$ .

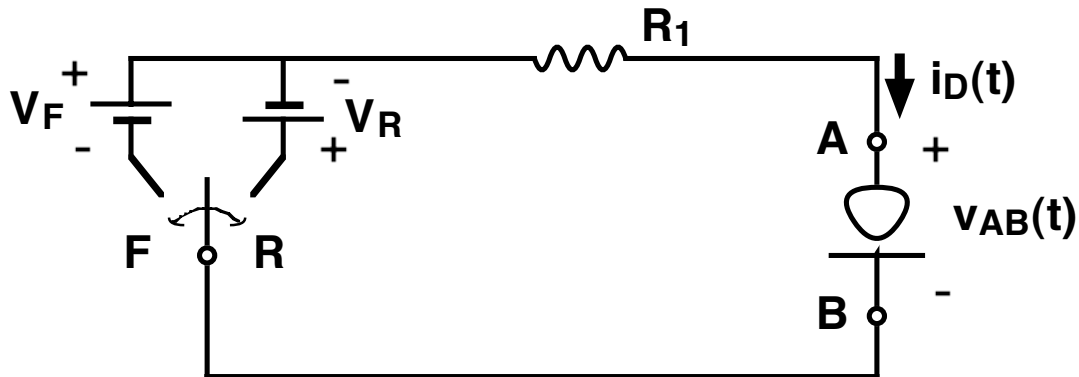
Positive      Negative

Sheet Density = \_\_\_\_\_  $\text{cm}^{-2}$

**End of Problem 1**

**Problem 2** (20 points)

You have used a circuit similar to the one illustrated below to look at the transients seen in turning a diode **off**. In this problem you are asked to use it to look at turning a diode **on**. The diode is an abrupt n<sup>+</sup>-p diode with  $N_{Dn} = 10^{18} \text{ cm}^{-3}$  and  $N_{Ap} = 10^{16} \text{ cm}^{-3}$ . The minority carrier lifetime on the n-side,  $\tau_h$ , is  $10^{-8} \text{ s}$ , and on the p-side,  $\tau_e$ , is  $10^{-6} \text{ s}$ . Throughout the diode:  $\mu_e = 1,440 \text{ cm}^2/\text{V}\cdot\text{s}$ ,  $\mu_h = 640 \text{ cm}^2/\text{V}\cdot\text{s}$ ,  $n_i = 10^{10} \text{ cm}^{-3}$ ,  $\epsilon_{si} = 10^{-12} \text{ F/cm}$ . The cross-sectional area is  $1 \text{ cm}^2$ ;  $w_n = 0.5 \text{ m}$ ,



and  $w_p = 5 \text{ m}$ .

- a) What are the minority carrier diffusion lengths on the n- and p-sides of this diode, and what is the built-in potential at the junction,  $\phi_b$ ? Use  $\frac{kT}{q} \ln 10 = 60 \text{ mV}$ .

$$\text{n-side: } L_h = \underline{\hspace{2cm}}$$

$$\text{p-side: } L_e = \underline{\hspace{2cm}}$$

$$\phi_b = \underline{\hspace{2cm}}$$

For the rest of this problem assume that the diode is best modeled by the short-base approximation, independent of what you answered above.

- b) You are told that the total width of the depletion region of this diode when it is unbiased (i.e.  $V_{AB} = 0$ ) is  $0.32 \text{ m}$ . What are the corresponding widths of the depletion regions on the n- and p-sides?

$$x_n(V_{AB} = 0) = \underline{\hspace{2cm}}$$

$$x_p(V_{AB} = 0) = \underline{\hspace{2cm}}$$

**Problem 2 continues on the next page.**

## Problem 2 continued

- c) For  $t < 0$ , the switch is in Position R so that the diode is reverse biased. For  $V_R = 6 \text{ V}$  and  $R_1 = 1 \text{ k}$ , what is  $i_D$  and what is  $v_{AB}$ ? Give numerical values; ignore the depletion region widths relative to  $w_n$  and  $w_p$ .

$$i_D = \underline{\hspace{2cm}}$$

$$v_{AB} = \underline{\hspace{2cm}}$$

- d) How much charge,  $Q_D$ , is stored in the depletion region of this diode with the reverse bias of Part (c)? (If you could not answer Part (c), assume this bias is  $-V_1$  for your answer in this part and below.)

$$Q_D = \underline{\hspace{2cm}}$$

- e) At  $t = 0$ , the switch is moved to Position F, where  $V_F = 6 \text{ V}$ ,  $R_1 = 1 \text{ k}$ , and the diode will be forward biased for  $t \gg 0$ .

- i) What is the diode voltage immediately after  $t = 0$ ,  $v_{AB}(0^+)$ ?

$$v_{AB}(0^+) = \underline{\hspace{2cm}}$$

- ii) What is the diode current immediately after  $t = 0$ ,  $i_D(0^+)$ ?

$$i_D(0^+) = \underline{\hspace{2cm}}$$

Problem 2 continues on the next page.

## Problem 2 continued

iii) What, approximately, is the diode voltage,  $v_{AB}$ , in the limit  $t \gg 0$ ?

$v_{AB}(t \gg 0)$  \_\_\_\_\_

iv) Use your approximate value for  $v_{AB}(t \gg 0)$  above to estimate the diode current,  $i_D$ , in the limit  $t \gg 0$ .

$i_D(t \gg 0)$  \_\_\_\_\_

v) Use your answer for  $i_D(t \gg 0)$  to refine your value of  $v_{AB}(t \gg 0)$ . If you could not solve Part (e) (iv), give your answer in terms  $I_2$ , where  $I_2 \equiv i_D(t \gg 0)$ .

$v_{AB}(t \gg 0)$  \_\_\_\_\_

vi) At some time,  $t_1$ , between  $t = 0+$  and  $t \gg 0$ ,  $v_{AB}$  is zero [i.e.,  $v_{AB}(t_1) = 0$ ]. Use your answers in Part (e) (ii) and Part (e) (iv) to estimate  $t_1$  (within a factor of two).

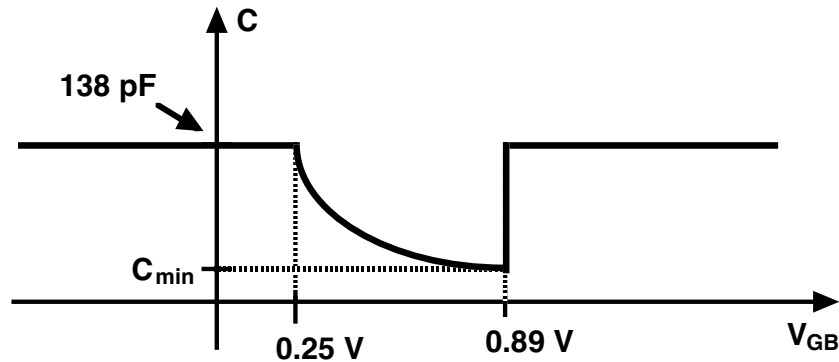
$t_1$  \_\_\_\_\_

vii) Explain, in 25 words or less, what happens during the transient for  $t > t_1$ , where  $t_1$  is as defined in Part (e) (vi).

End of Problem 2

**Problem 3** (20 points)

You are given the following MOS capacitor C-V curve measured on a chip you designed and processed. The dimensions of the MOS capacitor are  $W = 200 \text{ } \mu\text{m}$  and  $L = 200 \text{ } \mu\text{m}$ . The gate "metal" is p<sup>+</sup>-polycrystalline silicon (polysilicon) with  $\phi_{m,p^+} = -0.55 \text{ V}$ . Assume that  $\epsilon_{Si} = 10^{-12} \text{ F/cm}$ ,  $\epsilon_{ox} = 3.5 \times 10^{-13} \text{ F/cm}$ ,  $n_i = 10^{10} \text{ cm}^{-3}$ , and  $(kT/q)\ln 10 = 60 \text{ mV}$ .



- a) Determine the threshold voltage and flatband voltage of this device.

$$V_T = \underline{\hspace{2cm}}$$

$$V_{FB} = \underline{\hspace{2cm}}$$

- b) Determine the doping type and net doping concentration in the semiconductor upon which this capacitor is fabricated. Hint: Consider the flatband voltage.

$$\text{Type: } \underline{\hspace{0.5cm}} \text{ n-type } \underline{\hspace{0.5cm}} \text{ p-type}$$

$$N_A \text{ or } N_D = \underline{\hspace{2cm}}$$

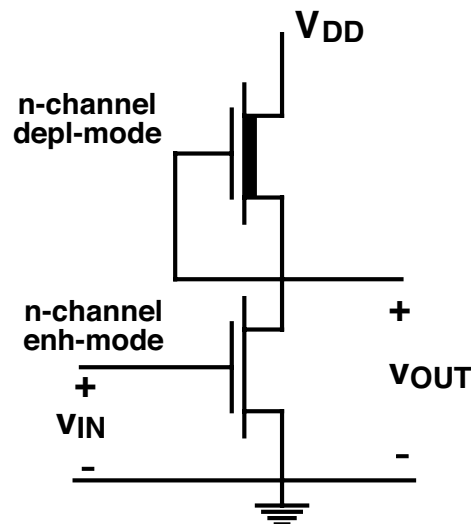
- c) What is the oxide thickness,  $t_{ox}$ ?

$$t_{ox} = \underline{\hspace{2cm}}$$

**Problem 3 continues on the next page**

## Problem 3 continued

- d) If the gate material is changed from p<sup>+</sup>-polysilicon to n<sup>+</sup>-polysilicon, how will the measured curve change? Assume  $\phi_{n+} = 0.55$  V. Keep your answer to 25 words or less.
- e) The same chip with the capacitor measured above (with p -poly) also has MOSFET circuits on it. Unfortunately, those circuits were designed to operate with a threshold voltage,  $V_T$ , 0.2 V higher than the C-V measurement (and other device measurements) showed  $V_T$  actually is. Can you recommend a course of action (other than processing another batch) to get the circuits functioning? Give your recommendation in 25 words or less, being fairly specific.
- f) One of the circuits on the chip is the NMOS inverter illustrated below



- i) Add the substrate terminal to each of the devices in the above circuit and indicate how they would be connected if  $V_{BS}$  on the enhancement-mode device is zero.

Problem 3 continues on the next page

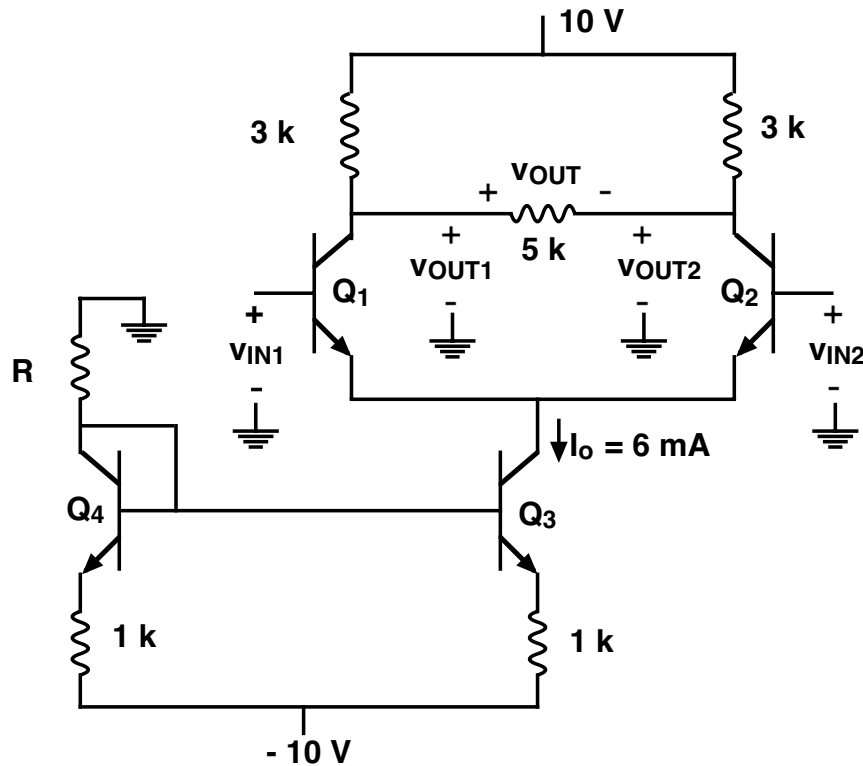
**Problem 3 continued**

- ii) In the space provided below, draw the incremental equivalent circuit for this circuit, valid for small signal operation about a bias point at which both transistors are in saturation.

**End of Problem 3**

**Problem 4** (20 points)

Consider the differential amplifier circuit illustrated below. All of the transistors in the circuit are identical with  $\beta = 75$ ,  $|V_{A1}| = 50\text{V}$ ,  $V_{BE,on} = 0.6\text{V}$ , and  $V_{CE,sat} = 0.2\text{V}$ .



- a) Find the value of  $R$ . Notice that  $I_o = 6\text{ mA}$ .

$$R = \underline{\hspace{2cm}}$$

- b) Find the quiescent value of  $V_{CE}$  for each transistor in this circuit (i.e. assuming  $V_{IN1} = V_{IN2} = 0$ ).

$$Q_1: V_{CE1} = \underline{\hspace{2cm}}$$

$$Q_2: V_{CE2} = \underline{\hspace{2cm}}$$

$$Q_3: V_{CE3} = \underline{\hspace{2cm}}$$

$$Q_4: V_{CE4} = \underline{\hspace{2cm}}$$

Problem 4 continues on the next page

### Problem 4 continued

- c) In the space below sketch the incremental half-circuit model you would use to calculate the difference-mode voltage gain of this circuit. Indicate the values of all of the elements in your circuit.

- d) Calculate the mid-band difference-mode voltage gain,  $A_{vd}$ , of this circuit.  $A_{vd} \equiv V_{od}/V_{id}$ , where  $V_{id} \equiv V_{in1} - V_{in2}$  and  $V_{od} \equiv V_{out1} - V_{out2}$ .

$$A_{vd} = \underline{\hspace{10em}}$$

- e) What is  $v_{OUT}$  if  $v_{IN1} = 5 \sin \omega t$  mV and  $v_{IN2} = 10 \sin \omega t$  mV? Assume that  $\omega$  is in the mid-band frequency range. If you could not solve Part d, write your answer in terms of  $A_{vd}$ .

$$v_{OUT} = \underline{\hspace{10em}}$$

Problem 4 continues on the next page

**Problem 4 continued**

- f) Determine the common-mode input voltage range of this circuit. That is, determine the range of values  $v_{IC}$  can have without moving any of the transistors out of their forward active operating region when there is no difference-mode input (i.e. when  $v_{IN1} = v_{IN2}$ ).

\_\_\_\_\_  $v_{IC}$  \_\_\_\_\_

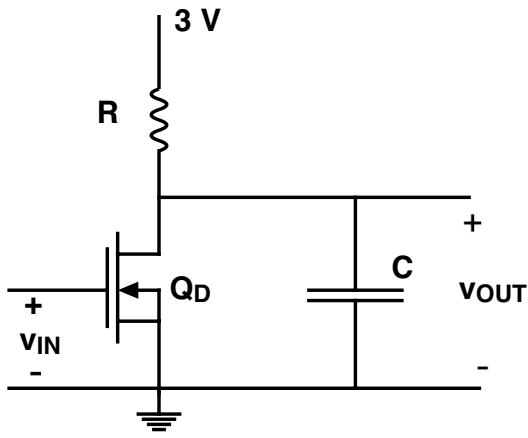
- g) Calculate the quiescent power,  $P_{ave}$ , dissipated in this circuit.

$P_{ave} =$  \_\_\_\_\_

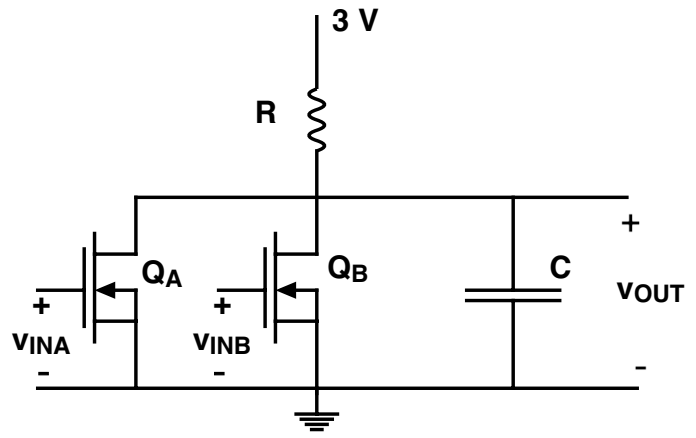
**End of Problem 4**

**Problem 5 (20 points)**

Consider the MOSFET circuits illustrated below; Circuit I is an inverter, Circuit II is a two-input logic gate. All of the MOSFETs are identical n-channel enhancement-mode devices with  $V_T = 0.75$  V.



Circuit I



Circuit II

- a) In Circuit I, what is  $V_{OUT}$  when  $V_{IN} = 0$  V?

$$V_{OUT} = \underline{\hspace{2cm}}$$

- b) With  $V_{IN} = 3$  V in Circuit I, we find  $V_{OUT} = 0.5$  V and  $I_D = 50$   $\mu$ A.

- i) What is the value of R?

$$R = \underline{\hspace{2cm}}$$

- ii) What is value of K for the transistor?

$$K = \underline{\hspace{2cm}}$$

Problem 5 continues on the next page.

## Problem 5 continued

- c) Complete the table below for Circuit II. (If you could not answer Part b you may leave your answers in terms of R and K).

$V_{INA}$	$V_{INB}$	$V_{OUT}$ (in Volts)
0 V	0 V	
3 V	0 V	
0 V	3 V	
3 V	3 V	

- d) The switching times for Circuit I are  $t_{LH}$  and  $t_{HL}$ , defined as follows:

$t_{LH} \equiv$  the time for  $v_{OUT}$  to change for LO to HI when  $v_{IN}$  is suddenly switched from HI to LO.

$t_{HL} \equiv$  the time for  $v_{OUT}$  to change for HI to LO when  $v_{IN}$  is suddenly switched from LO to HI.

Use this information to answer the following questions concerning the switching times for Circuit II:

- i) Define  $t_1$  as the time for  $v_{OUT}$  to change for LO to HI when  $v_{IN1}$  and  $v_{IN2}$  are suddenly switched from HI to LO. Is  $t_1$  greater than, equal to, or less than  $t_{LH}$ , and why?

$t_1$  greater than  $t_{LH}$

$t_1$  equal to  $t_{LH}$

$t_1$  less than  $t_{LH}$

because:

**Problem 5 continued**

- ii) Define  $t_2$  as the time for  $v_{OUT}$  to change for HI to LO when  $v_{IN1}$  is LO and  $v_{IN2}$  is suddenly switched from LO to HI. Is  $t_2$  greater than, equal to, or less than  $t_{HL}$ , and why?

$t_2$  greater than  $t_{HL}$

$t_2$  equal to  $t_{HL}$

$t_2$  less than  $t_{HL}$

because:

- iii) Define  $t_3$  as the time for  $v_{OUT}$  to change for HI to LO when  $v_{IN1}$  and  $v_{IN2}$  are both suddenly switched from LO to HI. Is  $t_3$  greater than, equal to, or less than  $t_{HL}$ , and why?

$t_3$  greater than  $t_{HL}$

$t_3$  equal to  $t_{HL}$

$t_3$  less than  $t_{HL}$

because:

**End of Problem 5**

**End of the exam**