

YOUR NAME _____

*Department of Electrical Engineering and Computer Science
Massachusetts Institute of Technology*

6.012 Electronic Devices and Circuits

FINAL EXAMINATION

Open book.

Notes:

1. Unless otherwise indicated, assume room temperature and that kT/q is 0.025 V.
2. This test is designed so that most parts can be worked independently of the others.
3. All of your answers and any relevant work must appear on these pages. Any additional paper you hand in will not be graded.
4. Make reasonable approximations and assumptions. State and justify any such assumptions and approximations.
5. Be certain that you have all twelve (12) pages of this exam booklet and make certain that you write your name at the top of this page in the space provided.
6. Your final grade can be obtained after 9 am Thursday, December 22. You may see your final exam beginning January 3, 1995.

For staff use only

Problem 1	_____
Problem 2	_____
Problem 3	_____
Problem 4	_____
Problem 5	_____

TOTAL

Problem 1 (15 points)

Warm-up questions, 3 points each:

a) A sample of silicon is known to contain 10^{17} cm^{-3} arsenic atoms (column V) and $5 \times 10^{16} \text{ cm}^{-3}$ boron atoms (column III). What are the equilibrium hole and electron concentrations in this sample at room temperature where $n_i = 10^{10} \text{ cm}^{-3}$?

$$n_o = \text{_____} \text{ cm}^{-3}$$

$$p_o = \text{_____} \text{ cm}^{-3}$$

b) A high quality long base silicon p-n diode is inadvertently irradiated in a nuclear reactor with the consequence that the minority carrier lifetimes on the n- and p-sides decrease from 10^{-4} s to 10^{-8} s (no other materials parameters change). How much, if at all, does the diode saturation current change?

$$\frac{I_{ES}(\text{after})}{I_{ES}(\text{before})} \text{ _____}$$

c) Rank order the following three bipolar linear amplifier configurations in order of increasing input resistance and indicate approximately the ratio of the highest to lowest input resistance, assuming comparable bias levels, I_C : common-emitter, common-base, emitter follower.

_____ _____ _____
 Lowest Middle Highest

$$\frac{R_{in}(\text{highest})}{R_{in}(\text{lowest})} \text{ _____}$$

Problem 1 continues on the next page.

Problem 1 continued

d) A certain common-emitter bipolar transistor amplifier is fabricated using resistors whose resistance is insensitive to temperature and with transistors whose forward current gain, β_F , Early voltage, V_A , and base-emitter knee voltage, $V_{BE,ON}$, are essentially unchanged between room temperature (25°C) and 100°C. None the less, when this amplifier is heated to 100°C its voltage gain, A_v , drops significantly. Give an explanation as to why the voltage gain might change and use your explanation to estimate $A_v(100^\circ\text{C})/A_v(25^\circ\text{C})$.

$$A_v(100^\circ\text{C})/A_v(25^\circ\text{C}) \quad \underline{\hspace{2cm}}$$

e) Answer in five words or less:

i) When operated at full speed, CMOS is as fast as any other MOSFET logic family and dissipates as much, or more, power. None the less, one of the most important applications for CMOS is in low speed circuitry. What is CMOS's advantage in these situations?

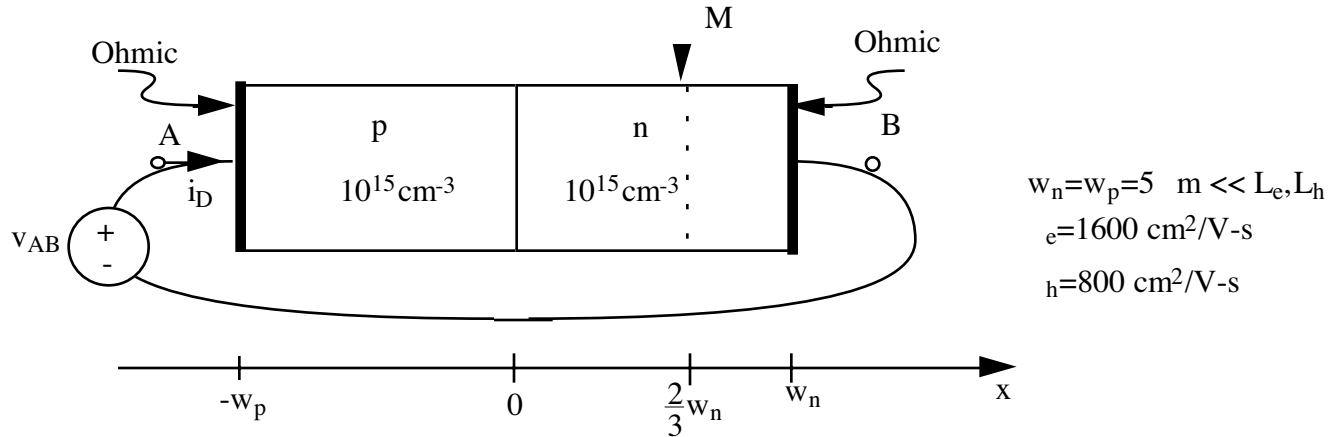
ii) What major structural change was made to enable the 486 to run faster than the 386 (and again to make the Pentium faster than the 486)?

iii) Why is CMOS attractive for linear amplifier applications? Give one reason (there are several).

End of Problem 1

Problem 2 (20 points)

The p-n diode shown below is illuminated by steady state light that generates M hole-electron pairs/cm²-s uniformly over the plane at $x = 2w_n/3$. The diode parameters are listed to the right of the drawing



(a) If we take as the criterion for low level injection that the excess minority carrier concentration must not exceed 10% of the equilibrium majority carrier concentration, what is the largest allowed value of M for the short circuited diode (i.e. with $v_{AB} = 0$)?

$M = \text{-----} \text{ cm}^{-2} \text{ s}^{-1}$

(b) For a particular level of illumination, M , it is known that the magnitude of the short-circuit diode current, $|i_D|$, is 1 mA.

i) What is the sign of this current, and why?

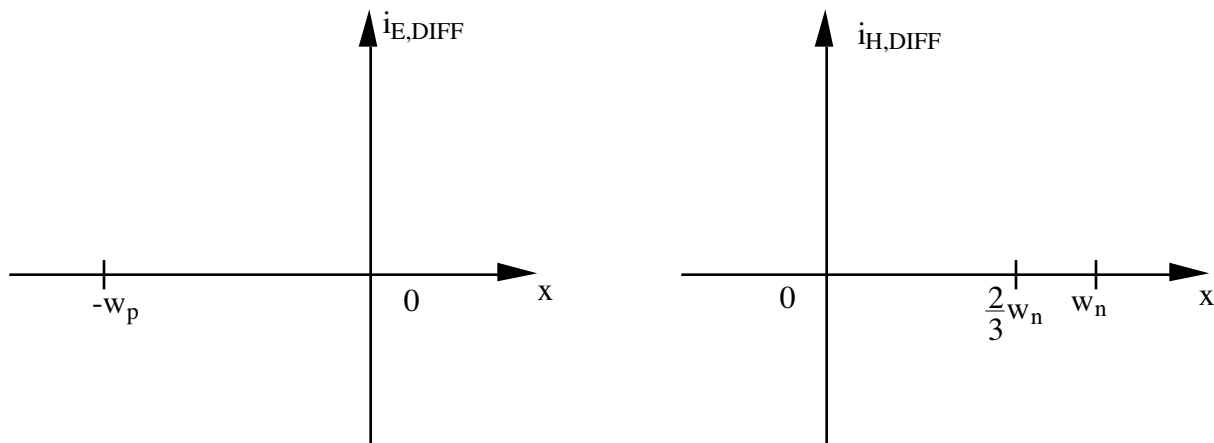
- Positive Negative

because

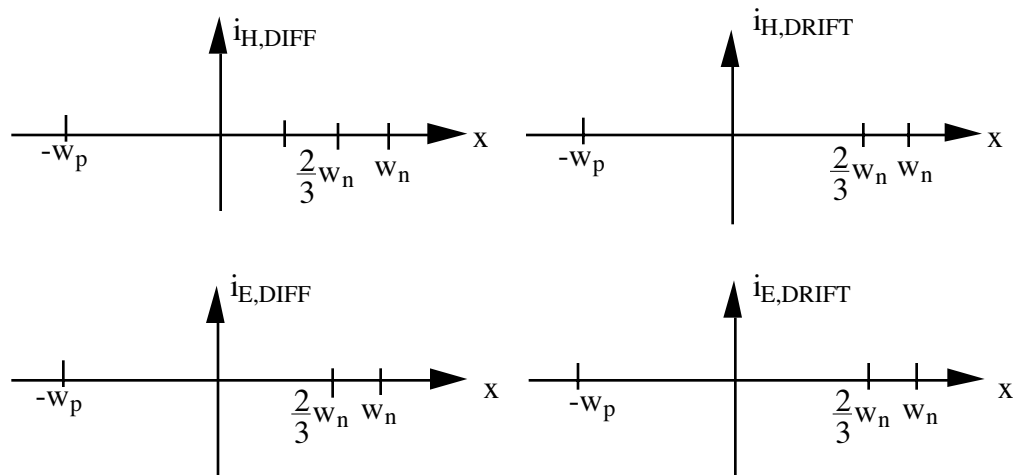
Problem 2 continues on the next page.

Problem 2 continued

ii) Make labeled plots on the axes provided below of the minority carrier diffusion currents in the p- and n-regions

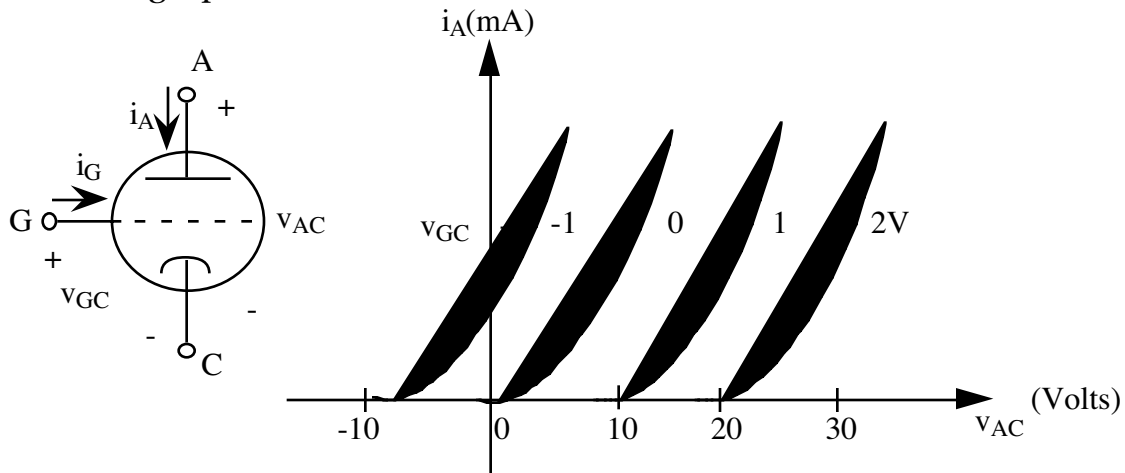


iii) On the axes provided below make labeled plots of the hole and electron drift and diffusion currents throughout the device.



c) In the space below draw a large signal equivalent circuit for the illuminated diode, using as one component the ideal exponential diode large-signal model for the p-n junction diode.

A certain three terminal transistor (different than any of the transistors we have studied thus far in 6.012) has the characteristics illustrated below, which can be described analytically by the formulas beneath the graph:



Analytical expressions:

$$i_G = I_G(e^{qV_{GC}/kT} - 1) \quad i_A = \begin{cases} 0 & \text{for } Kv_{AC} < v_{GC} \\ G(Kv_{AC} + v_{GC})^{3/2} & \text{for } Kv_{AC} \geq v_{GC} \end{cases}$$

where $I_G = 10^{-12}$ A, $K = 0.1$, and $G = 0.25$ mA/V^{2/3}

a) Consider a bias point $V_{AC} = + 50$ V, $V_{GC} = - 1$ V. What are I_G and I_A at this bias point?

$$I_G = \text{_____ mA}$$

$$I_A = \text{_____ mA}$$

b) For each of the following elements of a linear small signal equivalent circuit for this transistor provide (1) a general definition, (2) an algebraic expression(s) specific to this device, and (3) a numerical value valid for operation about the bias point in Part a:

i) Input conductance, g_{in} :

Definition:

Expression(s):

Value:

Problem 3 continued

ii) Transconductance, g_m :

Definition:

Expression(s):

Value:

iii) Output conductance, g_o :

Definition:

Expression(s):

Value:

c) In the space provided below draw a common-cathode low frequency, small signal linear equivalent circuit model for this transistor and use your model to derive an expression for the common-cathode open-circuit voltage gain, $A_{v,oc}$.

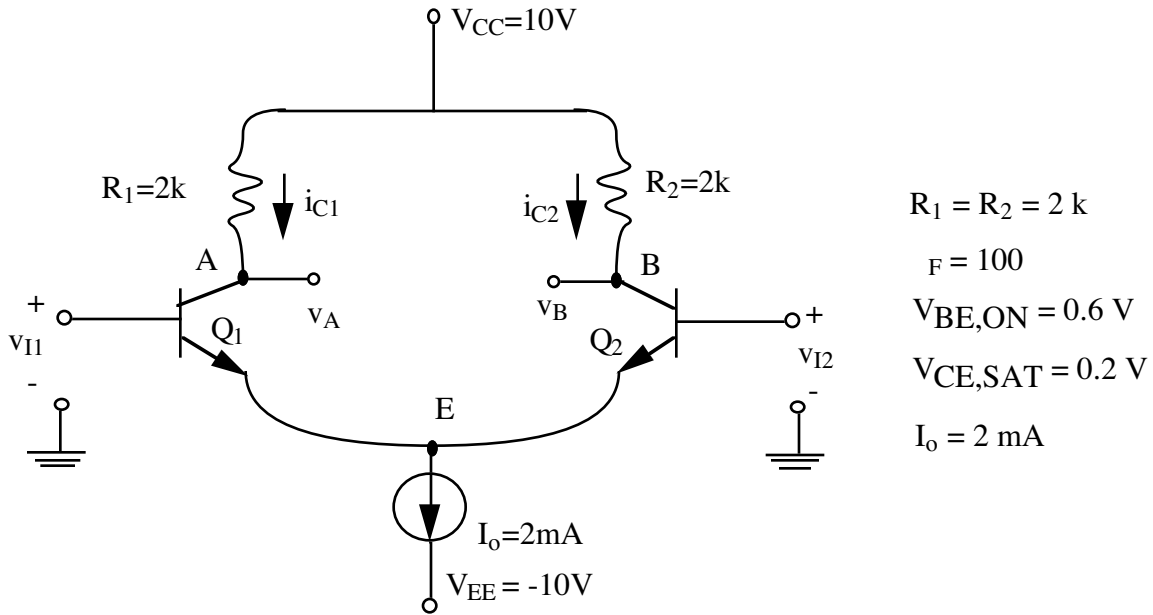
$$A_{v,oc} = \underline{\hspace{10cm}}$$

d) Describe, in 25 words or less, one shortcoming of this device that limits its use in a voltage amplifier.

End of Problem 3

Problem 4 (30 points)

The emitter-coupled pair amplifier shown below is biased by an ideal current source. All voltages in this schematic are referenced to ground.



a) With v_{I1} and $v_{I2} = 0$, find the voltage relative to ground at nodes A, B, and E.

$v_A = \text{-----} \text{ V}$

$v_B = \text{-----} \text{ V}$

$v_E = \text{-----} \text{ V}$

(b) With v_{I1} and $v_{I2} = 0$, is the current source delivering or receiving power, and what is the magnitude of this power?

Delivering Receiving $|P| = \text{-----} \text{ mW}$

Problem 4 continued

(c) A constant (dc) voltage V_C is applied to the input terminals so $v_{I1} = v_{I2} = V_C$. Find the voltage relative to ground at nodes A, B, and E, and find the base and collector currents of Q_1 and Q_2 when V_C has the values indicated in the table below:

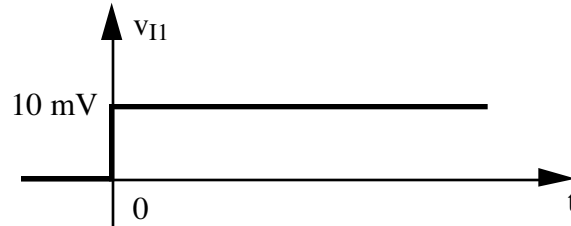
	$V_C = 3V$	$V_C = 6V$	$V_C = 9V$
v_A	-----	-----	-----
v_B	-----	-----	-----
v_C	-----	-----	-----
i_{C1}	-----	-----	-----
i_{C2}	-----	-----	-----
i_{B1}	-----	-----	-----
i_{B2}	-----	-----	-----

(d) In the space provided below draw the small signal linear equivalent circuit for the entire amplifier. Give numerical values for all of the circuit elements.

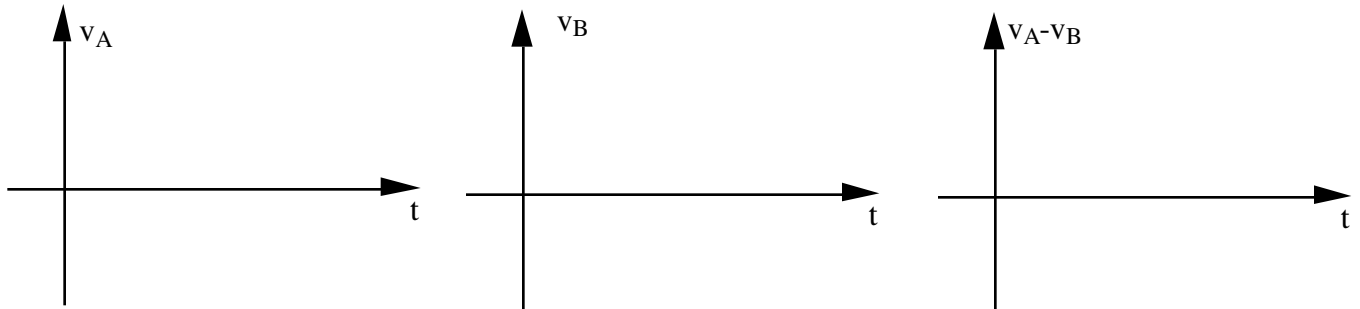
Problem 4 continues on the next page

Problem 4 continued

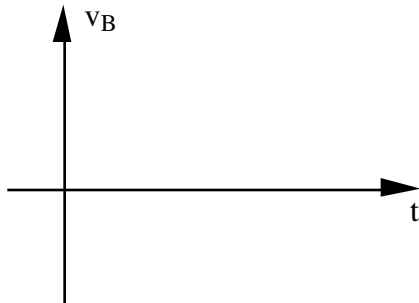
(e) Consider that the circuit has had v_{I1} and $v_{I2} = 0$ for a long time and that a small voltage step as illustrated below is applied to the left hand input.



i) On the axes provided below make labeled sketches of v_A , v_B , and $v_A - v_B$ for $t > 0$. Assume any turn-on transient is negligible.

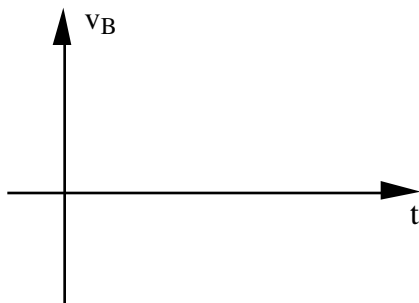


ii) A capacitor, $C = 3 \text{ F}$, is connected between output terminals A and B, and the same voltage step as applied to the input of the circuit. On the axes provided below make a labeled sketch of v_B for $t > 0$. What is the time constant of the transient in milliseconds (ms)?



= _____ ms

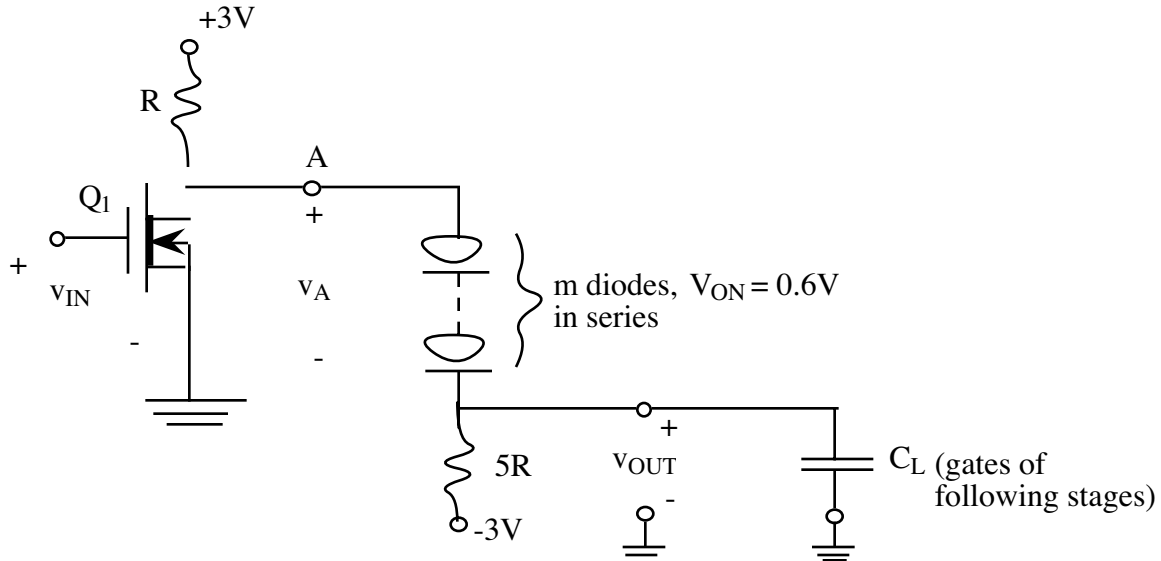
iii) Repeat Part e-ii with the 3 F capacitor removed from its initial position and now connected from terminal B to ground.



= _____ ms

End of Problem 4

This question concerns some of the issues that arise when one tries to make an inverter using a depletion-mode n-channel MOSFET. (You should recall that a depletion-mode n-channel FET is "on" with zero gate-to-source voltage, and that a negative voltage must be applied to its gate to turn it off.) Consider the circuit illustrated below. Note that it contains m diodes in series to adjust the output voltage level; you may model these diodes with a break-point model for which V_{ON} is 0.6 V.



$Q_1: V_T = -1V, K = 0.2 \text{ mA/V}^2$

a) i) What is v_A when Q_1 is off? (Your answer should include m , the number of diodes in series.)

v_A (with Q_1 off) = _____ V

ii) What is v_{OUT} when v_A is as in (i) (i.e. when Q_1 is off)?

v_{OUT} (with Q_1 off) = _____ V

b) Assume that when v_{IN} is "high" (i.e. $v_{IN} = V_{HI}$), Q_1 is on and effectively shunts node A to ground, yielding $v_A = 0$ V.

i) Explain why this is not an acceptable value for V_{LO} in this circuit and thus why v_A can not be taken directly as the output of this inverter stage.

ii) What is v_{OUT} (your answer should include m , the number of diodes)?

$v_{OUT} =$ _____

Problem 5 continues on the next page.

iii) What is the minimum value of m that will make this inverter operate with an acceptable V_{LO} . Explain your answer.

$$m \geq \underline{\hspace{2cm}}$$

because

c) Consider now the transients seen at the output of this inverter assuming that Q_1 turns on and off instantaneously.

i) What is the time constant associated with the output transient when the input goes from HI to LO (and the output then goes from LO to HI)?

$$(v_{OUT \text{ LO to HI}}) = \underline{\hspace{2cm}} \text{ s}$$

ii) What is the time constant associated with the output transient when the input goes from LO to HI (and the output then goes from HI to LO)?

$$(v_{OUT \text{ HI to LO}}) = \underline{\hspace{2cm}} \text{ s}$$

d) The magnitude of the resistance, R , effects many aspects of this circuit. Consider the impact of making R smaller on each of the following performance characteristics:

i) Static power dissipation, P_{static} : Making R smaller increases P_{static} , decreases P_{static} , has no effect on P_{static} , because

i1) Switching delay, t_d : Making R smaller, increases t_d , decreases t_d , has no effect on t_d , because

iii) Low logic level, V_{LO} : Making R smaller, increases V_{LO} , decreases V_{LO} , has no effect on V_{LO} , because