*YOUR NAME*________________________

Department of Electrical Engineering and Computer Science
Massachusetts Institute of Technology

6.012 Electronic Devices and Circuits

FINAL EXAMINATION

Open book.

Notes:

1. Unless otherwise indicated, assume room temperature and that kT/q is 0.025 V, kT/q ln 10 = 60 mV, and $n_i = 10^{10}$ cm^{-3} for Si.

2. This test is designed to that most parts can be worked independently of the others.

3. All of your answers and any relevant work must appear on these pages. Any additional paper you hand in will not be graded.

4. Make reasonable approximations and assumptions. State and justify any such assumptions and approximations.

5. Be certain that you have all thirteen (13) lucky pages of this exam booklet and make certain that you write your name at the top of this page in the space provided.

6. You may see your final exam beginning January 4, 1999.

For staff use only

Problem 1	______________
Problem 2	______________
Problem 3	______________
Problem 4	______________
Problem 5	______________
TOTAL	

Problem 1 (20 pts total)

Parts (a) thru (f) of this problem concern two npn silicon bipolar junction transistors, A and B. All of the dimensions of these two devices, and the magnitudes of all of the doping levels in these two devices are identical, <u>except that the base width</u>, w_B, of Transistor A is twice that of Transistor B.

(a) Which transistor, if either, has the larger dc current gain, β_F? Explain your answer and estimate the ratio of the two β_F's.

❑ Transistor A ❑ Transistor B ❑ neither, because

Ratio, $\beta_{F,A} / \beta_{F,B}$ = ____________

(b) Which transistor, if either, has the larger emitter-base junction saturation current, I_{ES}? Explain your answer and estimate the ratio of the two I_{ES}'s.

❑ Transistor A ❑ Transistor B ❑ neither, because

Ratio, $I_{ES,A} / I_{ES,B}$ = ________________

(c) With the base-collector junctions of both transistors reverse biased with the same values of base-collector junction voltage, V_{BC}, which transistor, if either, has the largest small-signal base-collector junction capacitance, C_μ? Explain your answer and estimate the ratio of the two C_μ's.

❑ Transistor A ❑ Transistor B ❑ neither, because

Ratio, $C_{\mu,A} / C_{\mu,B}$ = ________________

(d) With both transistors biased at the same quiescent current level, I_C, which transistor, if either, has the largest small-signal transconductance, g_m? Explain your answer and estimate the ratio of the two g_m's.

❑ Transistor A ❑ Transistor B ❑ neither, because

Ratio, $g_{m,A} / g_{m,B}$ = ________________

Problem 1 continues on the next page

Problem 1 continued

(e) Which transistor, if either, has a larger unity short-circuit current gain frequency, ω_T, at large collector current bias levels? Explain you answer and estimate the ratio of the two ω_T's.

❑ Transistor A ❑ Transistor B ❑ neither, because

Ratio, $\omega_{T,A}/\omega_{T,B}$ = ________________

(f) Which transistor, if either, has a larger Early voltage, V_A? Explain your answer.

❑ Transistor A ❑ Transistor B ❑ neither, because

Parts (g) thru (j) deal with an n-channel silicon MOSFET and a p-channel silicon MOSFET which are identical in all dimensions and doping level magnitudes except that the gate length, L, of one of the devices is twice that of the other. The K-factors in the large signal characteristics are also identical [where the K-factor is defined as $(W/L)\mu(e_{ox}/t_{ox})$].

(g) Which transistor, if either, would you expect to be the one with the longer gate length, and why?

❑ n-channel ❑ p-channel ❑ neither, because

(h) What is the ratio of the electron to hole mobility in these transistors (i.e., what is the ratio of the mobility of the electrons in the channel of the n-channel MOSFET to that of the holes in the channel of the p-channel MOSFET)? Explain your answer.

Ratio = ______ because

Problem 1 concludes on the next page

Problem 1 continued

(i) i) Which transistor, if either, has the larger small-signal gate-to-source capacitance in saturation, Cgs? Explain your answer.

❑ n-channel ❑ p-channel ❑ neither, because

ii) Which transistor, if either, has the larger small-signal gate-to-drain capacitance in saturation, C_{gd}? Explain your answer.

❑ n-channel ❑ p-channel ❑ neither, because

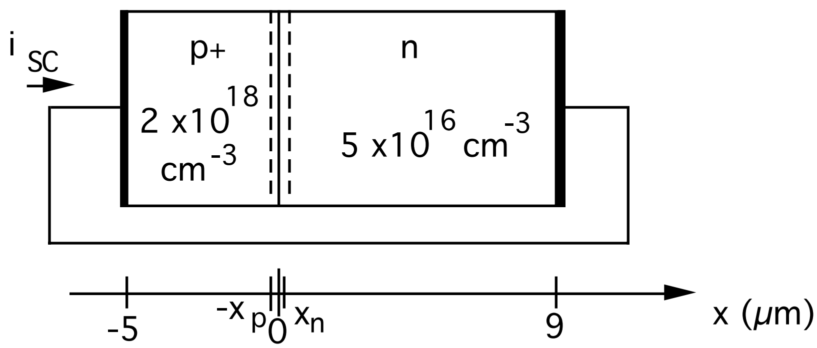
(j) Which transistor, if either, has the smallest drain-to-source transit time, τ_{tr}? Explain your answer.

❑ n-channel ❑ p-channel ❑ neither, because

End of Problem 1

Problem 2 (20 points)

Consider the p^+-n diode illustrated below. This diode has a cross-sectional area of 10^{-2} cm^2, a net acceptor concentration on the p-side, N_{Ap}, of 2 x 10^{18} cm^{-3}, and a net donor concentration on the n-side, N_{Dn}, of 5 x 10^{16} cm^{-3}. The electron mobility, μ_e, is 1600 cm^2/V-s, the hole mobility, μ_h, is 640 cm^2/V-s, the intrinsic carrier concentration, n_i, is 10^{10} cm^{-3}, and the minority carrier lifetime, τ_{min}, is 10^{-4} s.



(a) What is the built-in potential at the junction, ϕ_b?

ϕ_b = ____________________

(b) What is the minority carrier diffusion length, L_{min}, on the n-side?

L_{min} = ____________________

For the rest of this problem assume that the minority carrier diffusion lengths on the the n- and p-sides are much larger than the widths of the respective sides and that the depletion regions are negligibly thin, i.e. $L_{min} >> w_n, w_p >> x_n, x_p$.

(c) The diode is illuminated across the plane at x = 6 μm with light generating M hole-electron pairs/cm^2-s. The intensity of the light is such that the excess hole population at x = 6 μm, p'(6μm), is 10^{15} cm^{-3}.

(i) What is the short circuit current, i_{SC}, with this illumination?

i_{SC} = ____________________

Problem 2 continues on the next page.

Problem 2 continued

(ii) What fraction of the optically generated excess minority carriers recombine at the ohmic contact at x = 9 µm?

Fraction recombining at the ohmic contact: ________________

(iii) What is M?

M = ____________________

(d) Now consider moving the illumination from x = 6 µm to a position closer to the junction.

(i) Does the short-circuit current, i_{SC}, increase or decrease, and why?

❑ Increase ❑ Decrease ❑ No change, because

(ii) At what position of the illumination is the short-circuit current, i_{SC}, maximum, and what is its maximum value? You may leave your answer in terms of M if you prefer.

Position of illumination for maximum i_{SC}: x = ________

Maximum value of i_{SC}: ____________________

End of Problem 2

Problem 3 (20 points)

Consider an n-channel MOSFET with a channel length, L, of 1 μm and a channel width, W, of 10 μm, and for which V_{FB} = - 0.2 V and V_T = + 0.5 V, C^*_{ox} = 5 x 10^{-8} F/cm^2. The mobility of the electrons in the channel, μ_e, is 1000 cm^2/V-s

(a) This MOSFET is biased for t < 0 with $V_{BS} = V_{DS}$ = 0 V, and $v_{GS} = V_{FB}$ = - 0.2 V. At t = 0 the gate bias is changed to - 1.2 V.

(i) When t >> 0 and all transients have settled down, what is the total amount of any additional mobile charge at the oxide-semiconductor interface, and does it take the form of holes or electrons?

❑ Holes ❑ Electrons Total amount of charge:___________________________

(ii) Where does the mobile charge referred to in Part (a-i) come from?

(b) Now consider that this MOSFET is initially biased at threshold and the bias is suddenly increased. Assume the MOSFET is biased for t < 0 with $V_{BS} = V_{DS}$ = 0 V, and $v_{GS} = V_T$ = 0.5 V. At t = 0 the gate bias is changed to 1.5 V.

(i) When t >> 0 and all transients have settled down, what is the total amount of any additional mobile charge at the oxide-semiconductor interface, and does it take the form of holes or electrons?

❑ Holes ❑ Electrons Total amount of charge:___________________________

(ii) Where does the mobile charge referred to in Part (b-i) come from?

(c) What would your answer in Part (b-i) be if the drain-to-source bias was 10 V rather than 0 V, i.e., if V_{DS} = 10 V? All other voltages remain the same. HINT: Recall that C_{gs} of a MOSFET in saturation is 2/3 the total gate capacitance.

Total amount of charge:___________________________

Problem 3 continues on the next page.

Problem 3 continued

(d) This part of this problem concerns the transients associated with the gate voltage charging in Part (b), i.e. when the gate voltage is changed from V_T to V_T + 1 V. As in Part (b), assume $V_{BS} = V_{DS}$ = 0 V, unless otherwise instructed.

(i) If the charging was done through a 10 kOhm (i.e. 10^4 Ohms) resistor, how long would it take for the charging to be 90% complete?

Time to reach 90% of full charge:_____________

(ii) If the charging was done with a 100 μA (i.e. 10^{-4} A) current source, how long would it take for the charging to be 90% complete?

Time to reach 90% of full charge:_____________

(iii) If the charging was done by connecting the gate to an ideal voltage source with zero output resistance, and if all the lead and contact resistances are negligible, why wouldn't the gate charge up instantaneously, and what would you estimate the charging time to be?

Rate limiting process:_______________________

Approximate time to charge:______________________

(e) If the drain-to-source voltage was 10 V, rather than 0 V, in Part (d), your answers would be different. Indicate whether the charging would be faster or slower, and why and by how much, for Parts (d-i) and (d-ii), and for Part (d-iii), as indicated below.

(i) Parts (d-i) and (d-ii):

❑ Faster ❑ Slower by a factor of approximately ______ because:

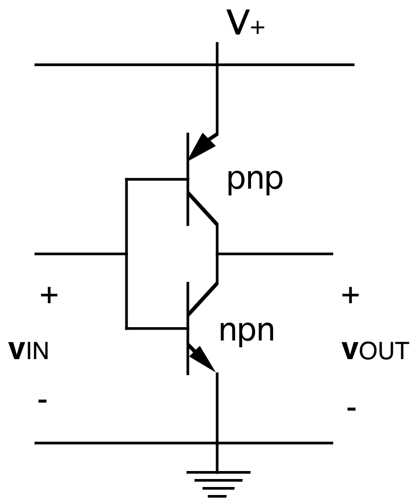
(i) Part (d-iii):

❑ Faster ❑ Slower by a factor of approximately ______ because::

End of Problem 3

Problem 4 (20 points)

A bipolar transistor manufacturer who is both impressed by CMOS inverters and fearful of the threat they pose to his business, has developed an complimentary bipolar logic family he calls CBL. The basic CBL inverter stage is illustrated below. The upper-most transistor is a pnp BJT and the lower transistor is an npn BJT. The transistors are designed to be symmetrical and to have the same saturation currents and alphas; thus for both $I_{ES} = I_{CS} = 10^{-14}$ A and $\alpha_F = \alpha_R = 0.9$.



(a) Check to see if the stage illustrated above actually functions as an inverter. Determine the state of each transistor with low and high inputs as directed below and indicate whether or not this stage is an inverter.

(i) What is the state of each transistor with v_{IN} = V+, where V+ = 1V, and is v_{OUT} low or high, and what is its approximate value?

pnp: ❑ Cutoff ❑ Active ❑ Saturated, because

npn: ❑ Cutoff ❑ Active ❑ Saturated, because

v_{OUT}: ❑ High ❑ Low, with value _________ because

(ii) Repeat part (i) with v_{IN} = 0 V.

pnp: ❑ Cutoff ❑ Active ❑ Saturated, because

npn: ❑ Cutoff ❑ Active ❑ Saturated, because

v_{OUT}: ❑ High ❑ Low, with value _________ because

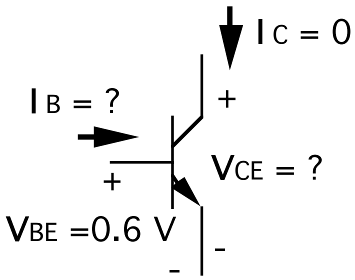
Problem 4 continues on the next page

Problem 4 continued

(iii) Does this stage function well as an inverter? Explain your answer

❑ Yes ❑ No, because

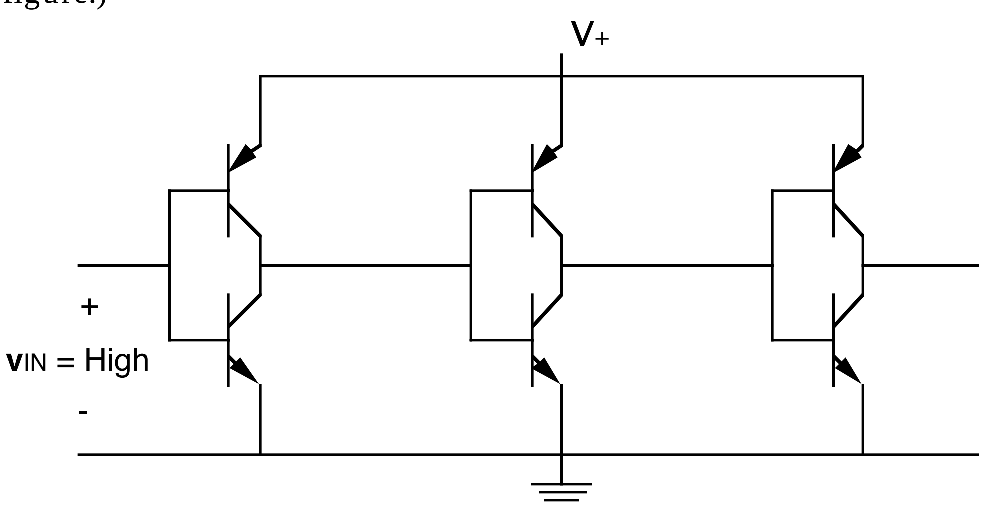
(b) Use the Ebers-Moll models given for the devices in this stage to determine the values of the collector-emitter voltage, V_{CE}, and the base current, I_B, of the npn transistor used in the circuit when a voltage of 0.6V is applied between its base and emitter and the collector terminal is open circuited, i.e., $i_C = 0$. The situation is illustrated below:



I_B = ____________________

V_{CE} = __________________

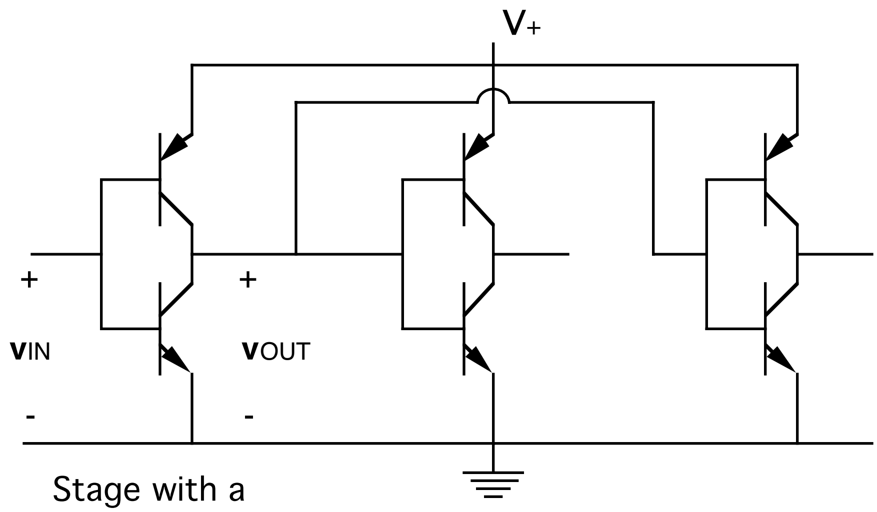
(c) The calculation you did in Part (b) can be used to estimate the low voltage level of this stage, but it is only an estimate because when such an inverter is used in an application it will be connected to other similar inverters, as illustrated below, and the collector current with v_{IN} high will not be zero. On the string of inverters below indicate with arrows all of the current paths by which current flows from the power supply to ground when the input on the left is high. (It may help you to label which transistors are on and which are off, and which outputs and inputs are high and low on the figure.)



Problem 4 continues on the next page.

Problem 4 continued

(d) Next we want to consider the impact of fan-out on the low and high output voltage levels of CJT inverter stages. Consider a CJT inverter whose output is taken to two stages, i.e. a stage with a fan-out of two (2), as illustrated below.



Stage with a fan-out of two (2)

With a fan-out of two (2) is the <u>low output value</u> (i.e., v_{OUT} with v_{IN} high) higher or lower than it is with a fan-out of one (1)?

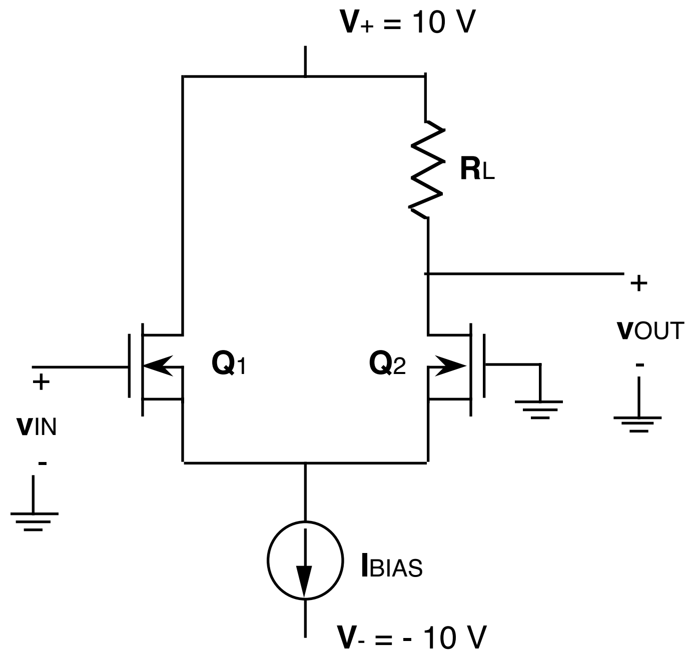
Low output value: ❑ Lower ❑ Higher ❑ No different, because

(e) Finally, in the space provided below, explain why we never worried about the impact of fan-out on the voltage levels of CMOS inverters.

End of Problem 4

Problem 5 (20 points)

You are asked to analyze the following circuit:



The two MOSFETs in this circuit are identical. Their relevant parameters are K = 5 mA / V^2, V_T = 0.5 V, and V_A = 20 V; it is also required that the MOSFETs be bisased (V_{GS} - V_T) be greater than 0.1 V for them to be properly on. The current source is ideal with I = 100 µA.

(a) Determine the value of R_L such that v_{OUT} = 2.5 V, when v_{IN} = 0 V.

R_L = ____________________

(b) Determine the gate-to-source voltages on each MOSFET, V_{GS1} and V_{GS2}, when v_{IN} = 0 V.

V_{GS1} = __________________

V_{GS2} = __________________

Problem 5 continues on the next page.

Problem 5 continued

(c) Derive an expression for the voltage gain, $A_v = v_{out}/v_{in}$, when both transistors are operating in their forward active regions, i.e. when they are in saturation, and calculate its value.

A_v (expression) = ____________________

A_v (value) = ___________________

(d) Determine the range of values of v_{OUT} for which the expression for A_v you derived in Part (c) is valid. Explain your assumptions.

_____________ $< v_{OUT} <$ _______

because

End of Problem 5

End of the exam

HAPPY HOLIDAYS