

MASSACHUSETTS INSTITUTE OF TECHNOLOGY
Department of Electrical Engineering and Computer Science
6.012 Electronic Devices and Circuits - Fall 2003

SPECIAL PROBLEM ON CIRCUIT DESIGN

Issued: Friday, November 7, 2003

Due: Wednesday, November 26, 2003 by 5 pm (be sure that your name is checked off the master list as you hand in your solution). Late solutions will receive zero points; see I.5 below.

I. General Comments

Don't panic when you see the circuit. It looks overwhelming at first but it is made up of simple building-block pieces and it is understandable. In addition, you will be given help along the way, first by this write-up, and later in recitations, lectures, and additional handouts. At the same time, the design process you need to go through is a complex one and not one you will successfully negotiate in one sitting. Thus it is important that you get started, first developing an understanding of the circuit and the nature of the design challenge, and then at doing your design. You can do it, but not in one night.

II. The Ground Rules

1. Consider this design problem more like an open book exam, than a problem set. You are encouraged to consult references and to seek guidance from the 6.012 staff, and to discuss design issues with others, but you should not work on your specific design and write-up with any other students or any other individuals. Nor should you compare design values or performance results with other students. The design you submit must be your own; any collaborations (and they should be minor) should be noted.

2. Do not let the design slide until the last week. Make a first attempt at a solution early so you can obtain any clarification and guidance you may need from the 6.012 staff well before the last weekend (November 22/23).

3. You are required to submit both the completed colored answer sheet (which will be distributed separately) and a detailed discussion of your design and your approach to arriving at it. Your write-up should include circuit diagrams for your large signal and incremental analyses, and the equations you used and calculations you made. It should also include a discussion of the trade-offs you considered in your design. View the minimum performance objectives as a challenge and try to do even better.

4. Make reasonable approximations. Do not carry your calculations out to any more than three (3) significant figures. Your resistor values and scaling factors should also be stated to no more than three (3) significant figures. The following are examples of numbers with three significant figures: 1.23, 0.123, 123, 3450, 0.0345, 6.78×10^9 .

5. Anyone who does not submit a design problem solution which demonstrates a reasonable level of effort will automatically receive zero points and a grade of "I" for 6.012 (as long as their performance is otherwise passing). An "I" received for this reason can only be completed by submitting an acceptable solution to this term's design problem by Feb. 1, 2004. Late solutions will be checked to determine that they are acceptable, but will receive zero points for purposes of determining an overall course grade.

III. Design Objective

Your design objective is to specify component values for the integrated linear amplifier shown in Figure 1 so that it meets or, hopefully, exceeds the performance objectives itemized below.

The circuit, which is described in full detail in Section V, is a BiCMOS differential amplifier designed to have a large output voltage swing, large common-mode rejection ratio, and large common-mode input voltage range. It relies heavily on n-channel MOSFETs in the critical gain stages to maximize its bandwidth.

You are to specify the resistor values and certain device dimensions in the circuit in Figure 1, and to calculate the corresponding bias levels and performance characteristics. You are also expected to discuss the main aspects of your design in your solution write-up, and to also discuss there the factors you took into consideration in arriving at your design.

Performance Objectives:

- 1) Small-signal gains defined by writing $v_{out} = A_{vc}(v_{in1}+v_{in2})/2 + A_{vd}(v_{in1} - v_{in2})$:
 - i) Small-signal difference-mode voltage gain, $|A_{vd}|$: 5×10^3
 - ii) Small-signal common-mode voltage gain, $|A_{vc}|$: 5×10^{-4}
- 2) Common-mode rejection ratio, A_{vd}/A_{vc} : 10^7
- 3) Small-signal output resistance, r_{out} : 75Ω .
- 4) Maximum output voltage swing into a 100Ω load, $|v_{OUT}|_{max}$: 0.65 V .
- 5) Minimum common-mode input voltage range, $|v_{IC}|_{min}$: 0.5 V .
- 6) Total quiescent power dissipation not to exceed 5 mW .
- 7) Quiescent output voltage, V_{OUT} , with shunt feedback*: $|V_{OUT}|$ 0.1 mV

* In practice a high-gain amplifier like this will be used with external feed-back elements that will insure that the quiescent output voltage is very near zero in spite of unavoidable imbalances and mismatches between the devices in any "real" integrated circuit, and even if we can't insure zero output in the ideal case.

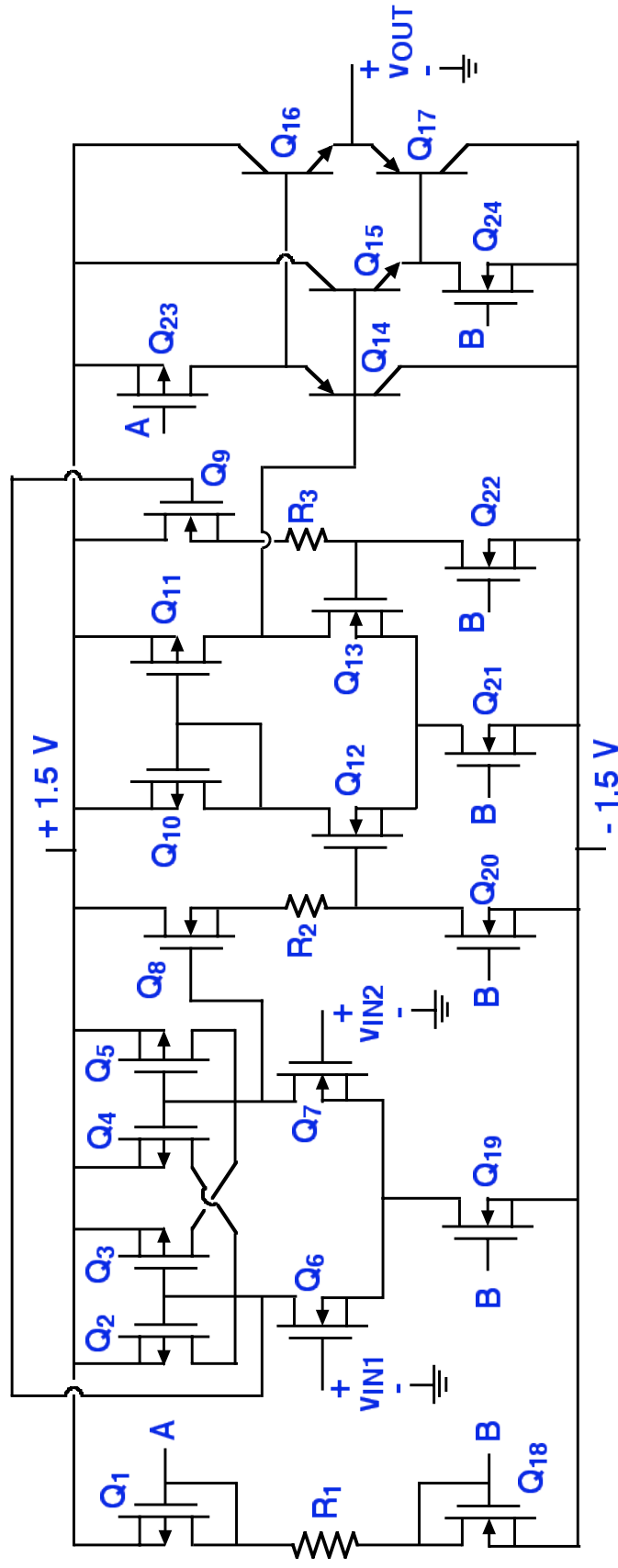


Figure 1 - The Fall 2003 Design Problem circuit, a high gain BICMOS differential amplifier with a large common-mode rejection ratio, common-mode input swing, and output voltage swing.

IV. Component Specifications

A. *Transistors*

Some of the transistors in the circuit can be chosen to be the smallest devices that can be made with the fabrication process used, but others will have to be designed to be larger; this might be done to adjust the value of a current source, for example, or to maximize the gain of a stage. In the listing below the properties of the minimum size devices are listed first and then the scaling rules for designing larger devices are given.

1. nnp Bipolar Transistors -- The npn transistors are vertical structures that have the following large-signal and small-signal (hybrid- π) parameters

- a) *Minimum size devices*
- i) $\beta_F = 100$
 - ii) $V_{BE,on} = 0.6 \text{ V @ } I_C = 100 \text{ } \mu\text{A}$ (i.e. $I_{ES} = 10^{-14} \text{ A}$)
 $V_{BC,sat} = 0.4 \text{ V}$
 - iii) $g_m = qI_C/kT$, $g_\pi = g_m/\beta_F$, $r_x = 0$
 $g_o = I_C/|V_A|$ with $|V_A| = 100\text{V}$
 - iv) Operating range: $0.5 \text{ } \mu\text{A} \leq I_C \leq 2 \text{ mA}$

b) *Scaled devices* -- You may increase the base-emitter junction area by up to a factor of 10 times. Increasing the base-emitter junction area, A_E , by a factor of γ , increases the current limits on the operating range by the same factor. The emitter-base diode saturation current in the Ebers-Moll model, I_{ES} , increases by the same factor, γ ; so too does I_{CS} . No other static model parameters change.

2. ppn Bipolar Transistors -- The pnp transistors are lateral structures that have the following large-signal and small-signal (hybrid- π) parameters

- a) *Minimum size devices*
- i) $\beta_F = 50$
 - ii) $V_{BE,on} = -0.6 \text{ V @ } I_C = -100 \text{ } \mu\text{A}$ (i.e. $I_{ES} = 10^{-14} \text{ A}$)
 $V_{BC,sat} = -0.4\text{V}$
 - iii) $g_m = q|I_C|/kT$, $g_\pi = g_m/\beta_F$, $r_x = 0$
 $g_o = |I_C|/|V_A|$ with $|V_A| = 50 \text{ V}$
 - iv) Operating range: $5 \text{ } \mu\text{A} \leq I_C \leq 1.0 \text{ mA}$

b) *Scaled devices* -- You may increase the base-emitter junction area by up to a factor of 10 times. Increasing the base-emitter junction area, A_E , by a factor of γ , increases the current limits on the operating range by the same factor. The emitter-base diode saturation current in the Ebers-Moll model, I_{ES} , increases by the same factor, γ ; so too does I_{CS} . No other static model parameters change.

3. n-channel MOSFET's -- The n-channel MOSFET's are enhancement-mode devices with the following large and small-signal parameters.

a) *Minimum size devices*

i) $K = 2.0 \text{ mA/V}^2$ $\alpha = 1$

ii) $V_T = +0.5 \text{ V}$

iii) $g_m = \sqrt{2K |I_D|}$
 $g_o = I_D / |V_A|$ with $|V_A| = 10 \text{ V}$

iv) Operating range: $(V_{GS} - V_T) \geq 0.2 \text{ V}$

b) *Scaled devices* -- The width of the gate (and channel), W , can be increased by up to a factor of 25 times, i.e., γ can be as large as 25. K varies linearly with W , so that $K_i = \gamma_i K_{\min}$. The length of the gate of the n-channel MOSFETs can not be increased.

4. p-channel MOSFET's -- The p-channel MOSFET's are enhancement-mode devices with the following large and small-signal parameters.

a) *Minimum size devices*

i) $K = 1.0 \text{ mA/V}^2$ $\alpha = 1$

ii) $V_T = -0.5 \text{ V}$

iii) $g_m = \sqrt{2K |I_D|}$
 $g_o = |I_D| / |V_A|$ with $|V_A| = 10 \text{ V}$

iv) Operating range: $(V_{GS} - V_T) \leq -0.2 \text{ V}$

b) *Scaled devices* -- The width of the gate (and channel), W , can be increased by up to a factor of 25 times, i.e., γ can be as large as 25. K varies linearly with W , so that $K_i = \gamma_i K_{\min}$. It is also possible to increase the length of the gate, L , by up to a factor of 5. Because K varies inversely with L , this decreases γ by as much as $1/5$. Also, increasing L increases $|V_A|$ by the same factor.

B. Resistors

The resistor values must be specified in increments of 100Ω . No resistor value is to exceed $50 \text{ k}\Omega$ or to be less than 100Ω , unless it is set equal to zero or infinity.

C. Power Supplies

The power supplies are ideal voltage sources with fixed values of 1.5 V and -1.5 V relative to ground.

V. Discussion of the Circuit

You should first look at the circuit carefully and identify its various pieces. Initially the circuit looks very complicated but if you break it into its component

parts and understand what each does and how they interact, you will find that the amplifier is actually much less formidable.

Begin by identifying the biasing circuitry and the current sources, in this case the n-channel MOSFETs Q_{18} , Q_{19} , Q_{20} , Q_{21} , Q_{22} , and Q_{24} ; the p-channel MOSFETs Q_1 and Q_{23} ; and the resistor R_1 . The chain formed by Q_1 , R_1 , and Q_{18} determines the reference voltages at points A and B. In this way, the transistor Q_{18} establishes the reference voltage on the gates of Q_{19} , Q_{20} , Q_{21} , Q_{22} , and Q_{24} ; and transistor Q_1 establishes the reference voltage on the gate of Q_{23} .

Once you see which transistors are involved in the biasing you can mentally replace them with current sources, as has been done in Figure 2, and ignore those devices until much later. Focus first on determining what bias currents you want from each current source, and the values of V_{GS} you want on Q_1 and Q_{18} . When these are known, then you will be able to complete the design of the devices in the current sources. The design of the Q_1 - R_1 - Q_{18} chain, for example, will be relatively easy after you have a target current level and target V_{GS} 's on Q_1 and Q_{18} .

Move on next to look at the amplifier stages themselves, starting with the input stage, Q_6 and Q_7 . This stage is an n-channel MOSFET differential common-source stage loaded with a Lee Load formed by the p-channel MOSFETs Q_2 , Q_3 , Q_4 , and Q_5 . The Lee Load was invented by Professor Tom Lee of Stanford (a former 6.012 student). It looks incrementally like a very large resistor for differential-mode inputs, and like a very much smaller resistor for common-

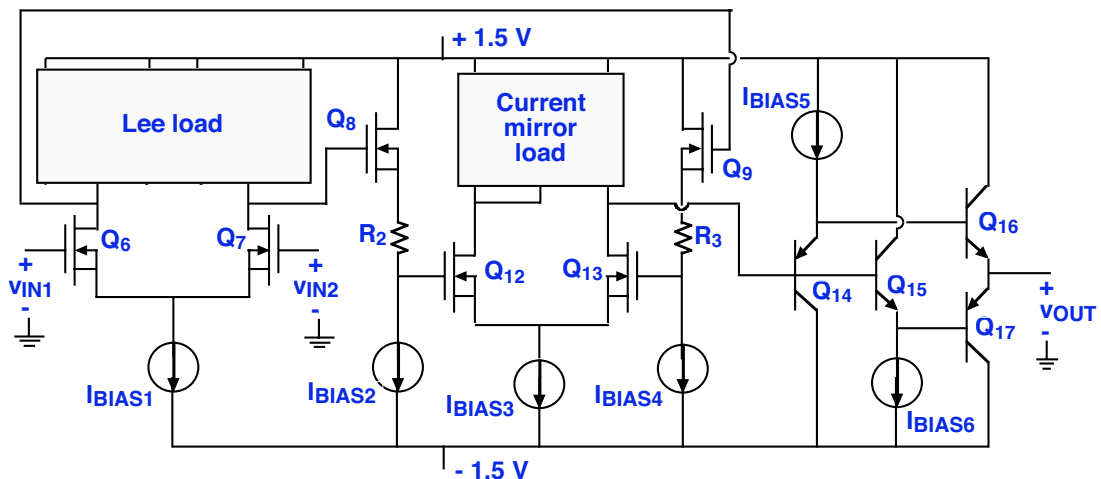


Figure 2 - A simplified schematic of the design problem circuit drawing attention to some of the functional units of the circuit. There are five stages in this amplifier: From left to right, we find that Stage 1 is an n-MOS common-source gain stage with a Lee load; Stage 2 is an n-MOS source-follower level-shift stage; Stage 3 is an n-MOS common-source stage with a p-MOS current mirror load; Stage 4 is a pair of BJT emitter-follower buffer stages; and Stage 5 is a BJT push-pull output stage (this is essentially another emitter-follower stage).

mode inputs. The difference-mode voltage gain is thus very large and the common-mode voltage gain is less than one (i.e., it is not a gain, but an attenuation). Consequently using the Lee Load results in a gain stage with a very large common-mode rejection ratio.

The second stage is an n-channel MOSFET differential source-follower level-shift stage, Q_8 and Q_9 . The quiescent voltage drop across resistors R_2 and R_3 shifts the bias level at the input of the next stage to a lower value so you will be able to bias its output near zero volts. The primary role of this stage is to provide this bias level shift. Notice, however, that it does introduce some attenuation of the signal because of the current divider effect of the resistors in series with the output resistance of the current sources biasing the stage.

The third stage is a second common-source gain stage, Q_{12} and Q_{13} , this time with a current-mirror load, Q_{10} and Q_{11} . The biasing of this stage is important to meeting the output voltage swing specification. The current mirror does several things: First, it provides an active load which effectively applies the output of Q_{10} to the gate of Q_{11} , so that the output due to the difference-mode signal input to Q_{10} is added to the output due to the difference-mode signal input to Q_{13} . Doing this converts the output from a double-ended (or differential) output to a single-ended output, and does so in such a manner that we obtain an additional factor of two in gain. (This is explained in Section 12.4, pages 392-395 in the Course Text.) Second, the output resistance of the current mirror looks different for common-mode and difference-mode signals, which helps reduce the common-mode voltage gain.

The output of the third stage is taken from the node joining the drains of Q_{11} and Q_{13} , and is what is termed a "high impedance" node. In practice the quiescent value of the voltage on this node this voltage is sensitive to differences in the transistors and process variations. This is a typical situation in high gain differential amplifiers and the issue is dealt with by using the amplifier with feedback that stabilizes the quiescent output voltage very near to zero volts. It is still important to design the circuit so that this output voltage would be as small as possible (within the other design constraints) if every transistor in the circuit met the design specifications exactly, but the actual quiescent value of zero Volts will be established by an external feedback circuit.

The fourth "stage" is a pair of emitter-follower stages, one that uses a pnp BJT and the other that uses an npn BJT. These followers are coupled to the fifth, and final stage, which is a complimentary output stage called a push-pull stage. This is basically an emitter-follower stage in which an npn transistor (Q_{16} in this circuit) drives the load (i.e., supplies current to the load resistor) when the output voltage goes above zero, and a pnp transistor (Q_{17}) turns on and drives the load when the voltage goes negative.

The quiescent current through Q_{16} and Q_{17} will be the quiescent current through Q_{14} and Q_{15} multiplied by the ratio of the areas of the two sets of devices. The sizes of these devices will be important design parameters.

Taken together the last two stages give the amplifier a low output resistance (see Section 11.3.4, and especially the discussion on page 345, in the Course Text). This is a different push-pull design than that in the text, but the basic idea is the same. When you do your design problem analysis of the last stage (the push-pull) both pairs of transistors (the pair Q_{14} and Q_{16} , and the pair Q_{15} and Q_{17}) are on and their incremental equivalents are in parallel. When the output goes positive, however, the lower pair (Q_{15} and Q_{17}) soon turns off and the upper pair (Q_{14} and Q_{16}) turns more strongly on and dominates the contribution of this part of the circuit to the output resistance and to the loading on the second gain stage. When the output goes negative, the lower pair dominates and the upper pair turns off. Also assume a $100\ \Omega$ load, and remember that the design spec is that the quiescent output voltage is $0\ \text{V}$.

VI. Starting your Analysis

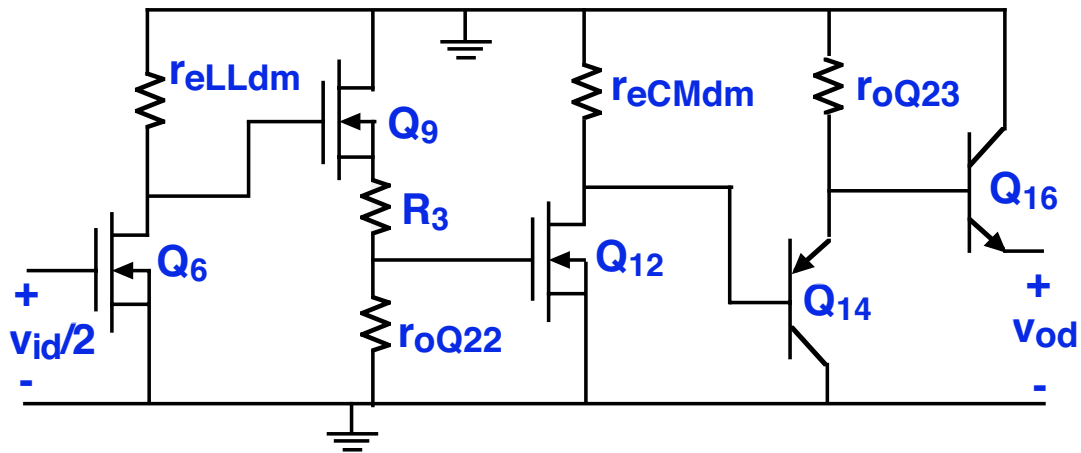
As pointed out earlier, one of the first things to do is to identify the various sub-circuits in the full circuit, i.e., the various gain stages, the biasing circuitry, etc. Then look at each piece individually and understand what it can do and what constraints are placed upon it. Look at each gain stage, for example, and write an expression for its gain. Try to get a relationship that depends on the bias level and device parameters, and then on any bounds on the dimensions of the devices, and on any limitations on the operating currents and/or voltages of the devices. We know in general, for example, that MOSFET gain stages loaded with non-linear loads formed from transistors biased in their constant current regions (FAR in the case of BJTs; saturation in the case of MOSFETs) tend to have higher gain when biased at low levels of drain current, that is, with small $|V_{GS} - V_T|$. Since there is a minimum value this quantity can have, it will be useful to try to express the gain of the current mirror gain stage in terms of $|V_{GS} - V_T|_{\min}$, and find what the maximum gain for the stage can be. Then you can begin to understand how you must size and bias the stage to achieve that gain (or as near to it as possible).

You should also spend some time understanding the output stages; in particular what the output resistance depends upon and whether that impacts any earlier stage(s), and what constraint the output voltage swing specification implies. To analyze the final stage you can assume that only one of the transistors is on at a time. (For your incremental modeling, assume the npn transistor is the one that is on, as was discussed at the end of Section V.)

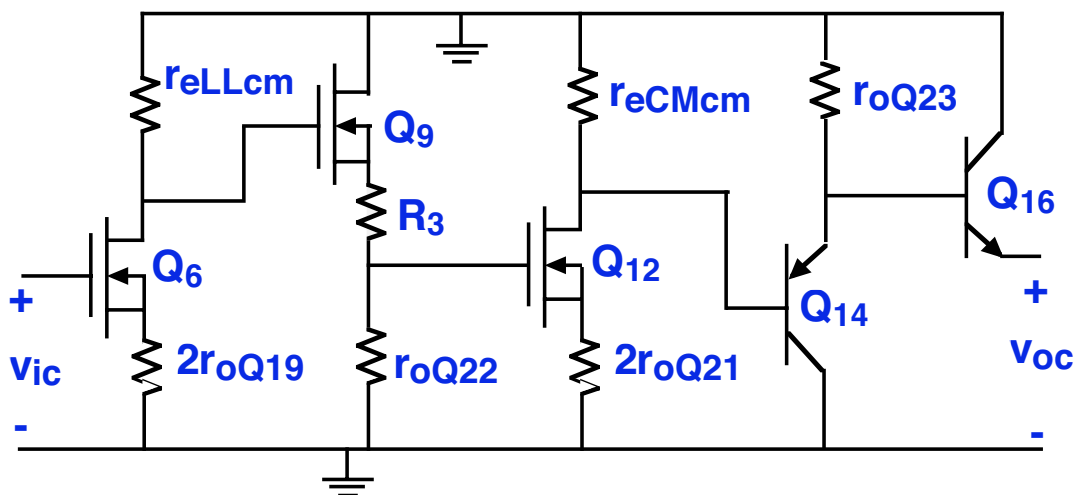
To help you get started understanding the incremental behavior of the amplifier, partial small signal linear equivalent circuits for the amplifier with difference- and common-mode inputs are shown in Figures 3a and 3b, respectively

The biasing circuitry can be viewed as a separate issue in terms of understanding how it operates. Once you do this you can understand how to size the various transistors and R_1 to achieve the bias levels you need based on your understanding and analysis of the amplifier proper. Of course, there may be limitations placed on the bias levels you can achieve that force you to adjust

your designs for the amplifier stages, but by this point your understanding of the circuits should be such that making any such adjustments is not a major calamity; a major pain maybe, but no cause for panic.



(a) Difference-mode input



(b) Common-mode input

Figure 3 - Partial linear equivalent circuits for the design problem circuit for difference-mode and common-mode inputs. The transistors need to be replaced by their linear equivalent circuits to get the complete linear equivalent circuit of the amplifier, and the factor of 2 enhancement from the current mirror has to be included, but these abstractions help one gain insight. " r_{eLLdm} ", " r_{eLLcm} ", " r_{eCMdm} ", and " r_{eLLcm} ", refer to the equivalent linear difference- and common-mode load resistances, respectively, of the Lee Load and Current Mirror load, and " r_{oQ_x} " refers to the equivalent linear output resistance of transistor Q_x . A document giving expressions for the effective load resistances of the Lee Load and the Current Mirror load has been posted on the course website in the "Design Problem" section.

A second set of things you should do early in your design process is to look through the design specifications and understand upon what each depends. As you develop an understanding of the circuit, you can write expressions for the various quantities specified (i.e., voltage gains, input and output resistances, etc.).

Once you begin to understand the pieces and specifications, make some initial design choices and see what you get. You may find that some parts work just fine, while others require major reworking. It may take several iterations to meet all of the specifications, but the more you understand the pieces and their interactions, and understand the implications for the circuit of the constraints placed on the sizes and operating ranges of the devices, the more quickly you can get to the answer and the less of a random walk your effort will seem.

VII. Enhancements to the Circuit

You are encouraged to think about (and discuss in your write up) ways that the circuit could be improved beyond the present design.