

Lecture 17 - Linear Amplifier Basics - Outline

- **Announcements**

 - Handouts - Lecture Outline and Summary

 - Web posting - Expanded Lecture 16 foil set

 - Exam 2 - Wednesday night, November 5, Room 10-250

- **Review - CMOS inverters**

 - Noise Margins: when $\{dv_{OUT}/dv_{IN}\} > 1$, disturbance grows

 - Gate delay: often defined as average, i.e. $(\tau_{LO-HI} + \tau_{HI-LO})/2$ (We leave the 2 out)

 - Power density: $PD = P_{ave} @ f_{max} / \text{Area}$ (Maximum power density is what matters)

 - Using $P_{ave} = f C_L V_{DD}^2$, and noting $f_{max} \propto 1/GD$, and Area $\propto W_n L_{min}$:

 - $PD \propto \mu_e \mu_{bx} V_{DD} (V_{DD} - V_T)^2 / t_{ox} L_{min}^2$ (Must reduce dimensions and voltage - Lec 25)

- **Biasing transistors**

 - Current source biasing

 - Transistors as current sources

 - Current mirror current sources and sinks

- **Linear amplifiers**

 - Performance metrics: gains (voltage, current, power)

 - input and output resistances

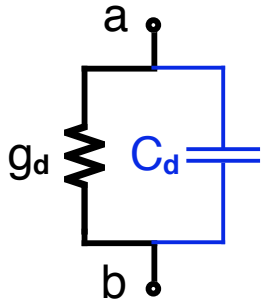
 - power dissipation

 - bandwidth (We'll save this for later - Lec. 22)

 - Possible amplifier connections of transistors

• **Linear equivalent circuits:**

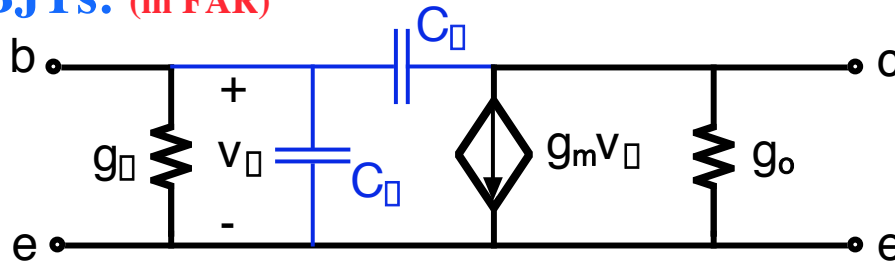
pn diodes:



$$g_d = q|I_D|/kT$$

$$C_d = g_d \tau_d + C_{dpl}(V_{AB})$$

BJTs: (in FAR)



$$g_m = q|I_C|/kT$$

$$g_\pi = g_m / \beta_F$$

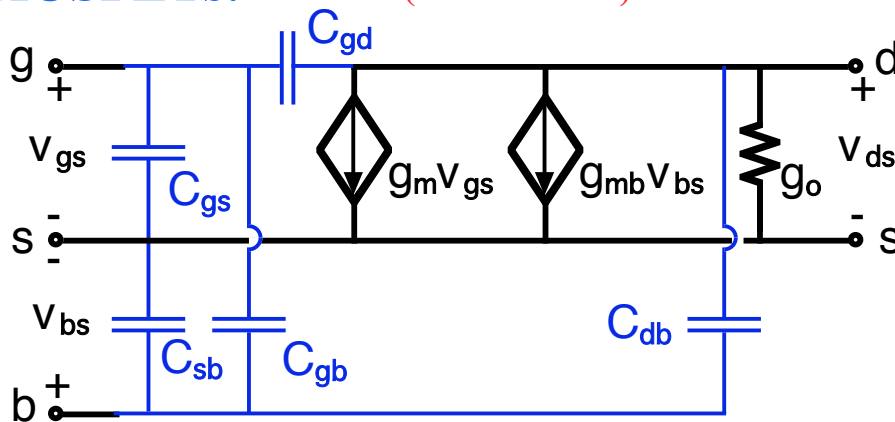
$$g_o = |I_C/V_A| \text{ [or } \beta |I_C|]$$

$$C_\pi = g_m \tau_b + C_{dpl,be}(V_{BE})$$

$$\tau_b = w_B^2 / 2D_e$$

$$C_\mu = C_{dpl,bc}(V_{BC})$$

MOSFETs: (in saturation)



$$g_m = K(V_{GS} - V_T) = (2K|I_D|)^{1/2}$$

$$g_{mb} = \beta g_m$$

$$\beta = \{ \epsilon_{Si} q N_A / 2(|I_D| - V_{BS}) \}^{1/2} / C_{ox}^*$$

$$g_o = |I_D/V_A| \text{ [or } \beta |I_D|]$$

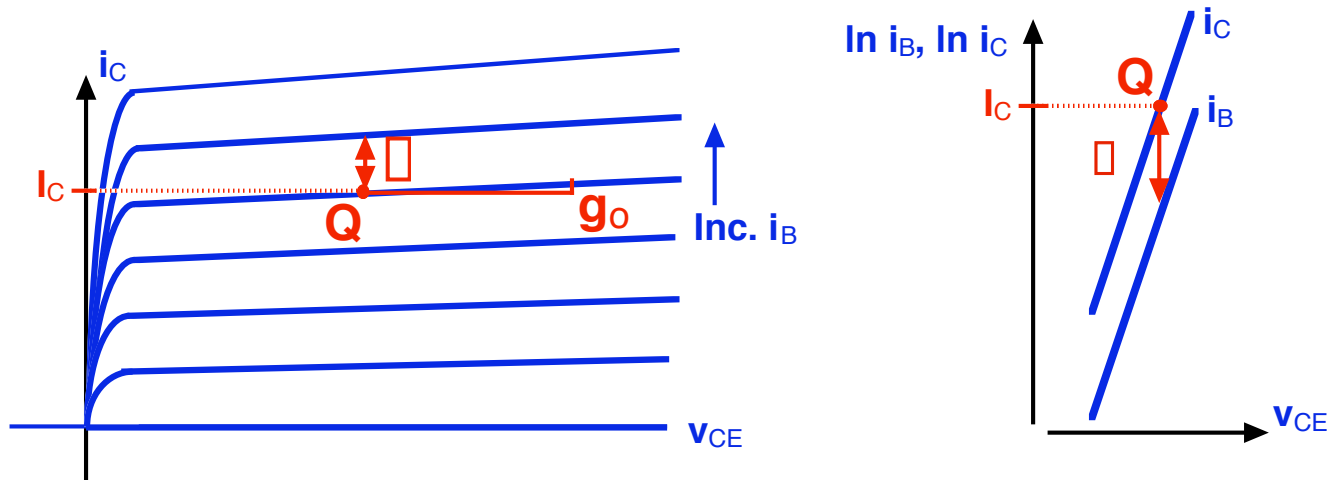
$$C_{gs} = (2/3) WL C_{ox}^*$$

$$C_{gd}: \text{ G-D fringing and overlap capacitance, all parasitic}$$

$$C_{sb}, C_{gb}, C_{db}: \text{ depletion capacitances}$$

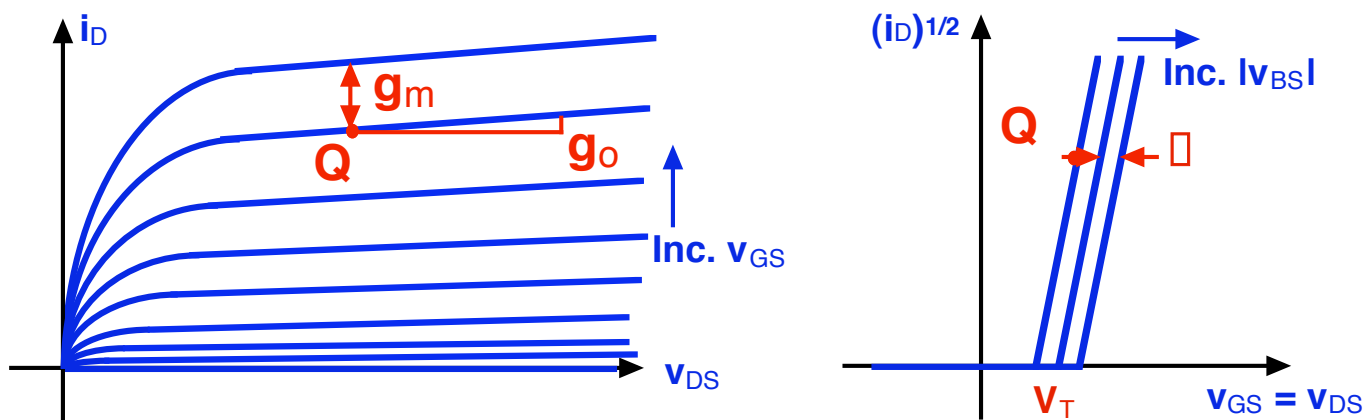
- Identifying the incremental parameters in the characteristics

BJT:



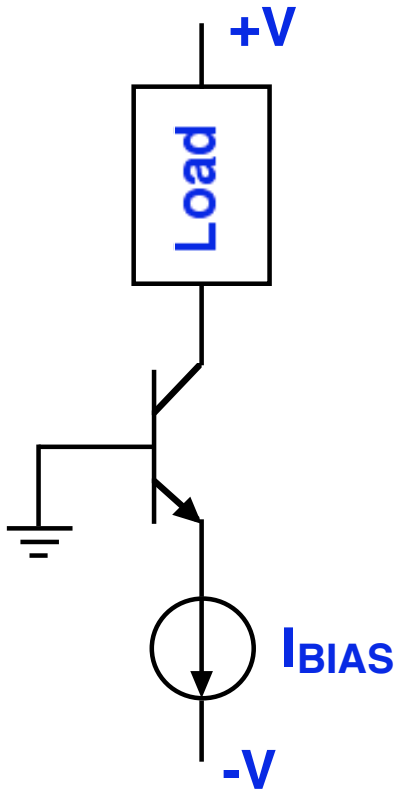
$$g_m = qI_C/kT; g_{\square} = \square g_m \text{ with } \square = di_C/di_B|_Q; g_o = di_C/dv_{CE}|_Q$$

MOSFET:

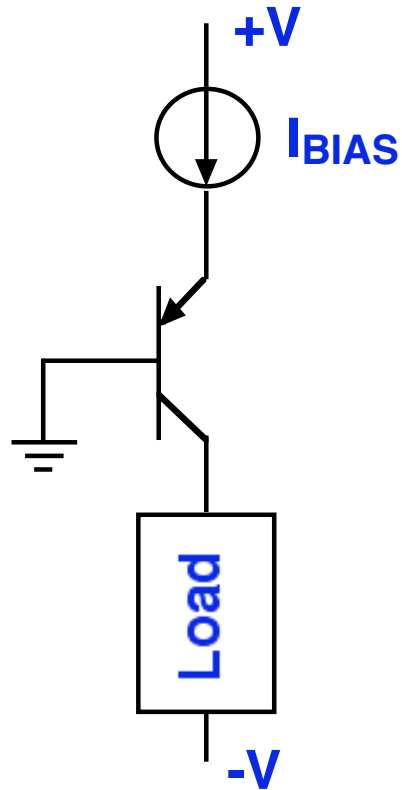


$$g_m = di_D/dv_{GS}|_Q; g_{mb} = \square g_m \text{ with } \square = -dV_T/dv_{BS}|_Q; g_o = di_D/dv_{DS}|_Q$$

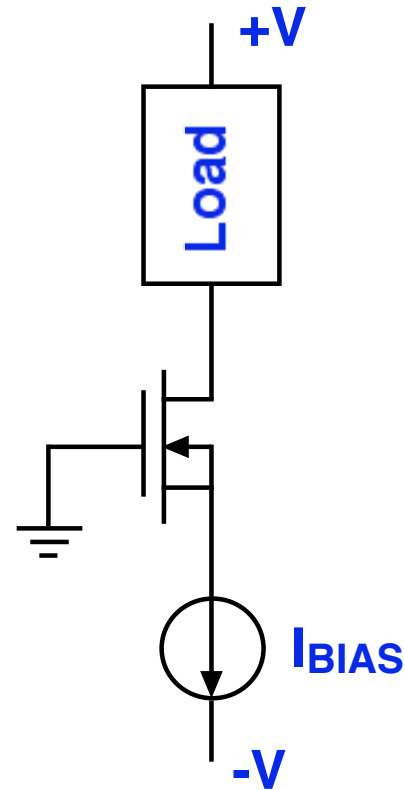
- **BJTs and MOSFETs biased for linear amplifier applications**



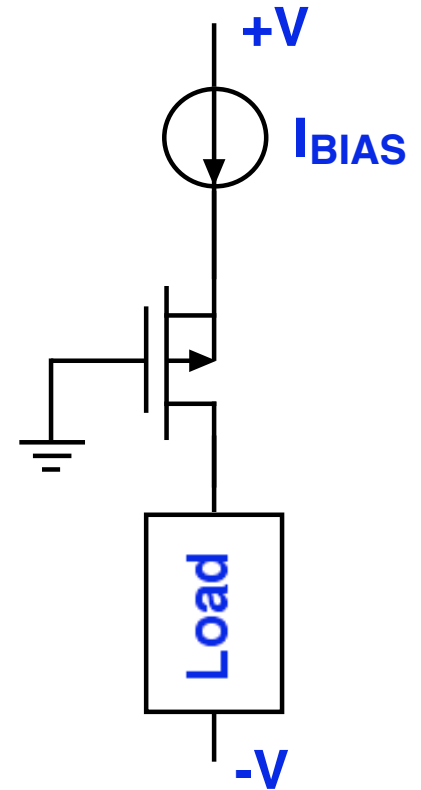
npn



pnp

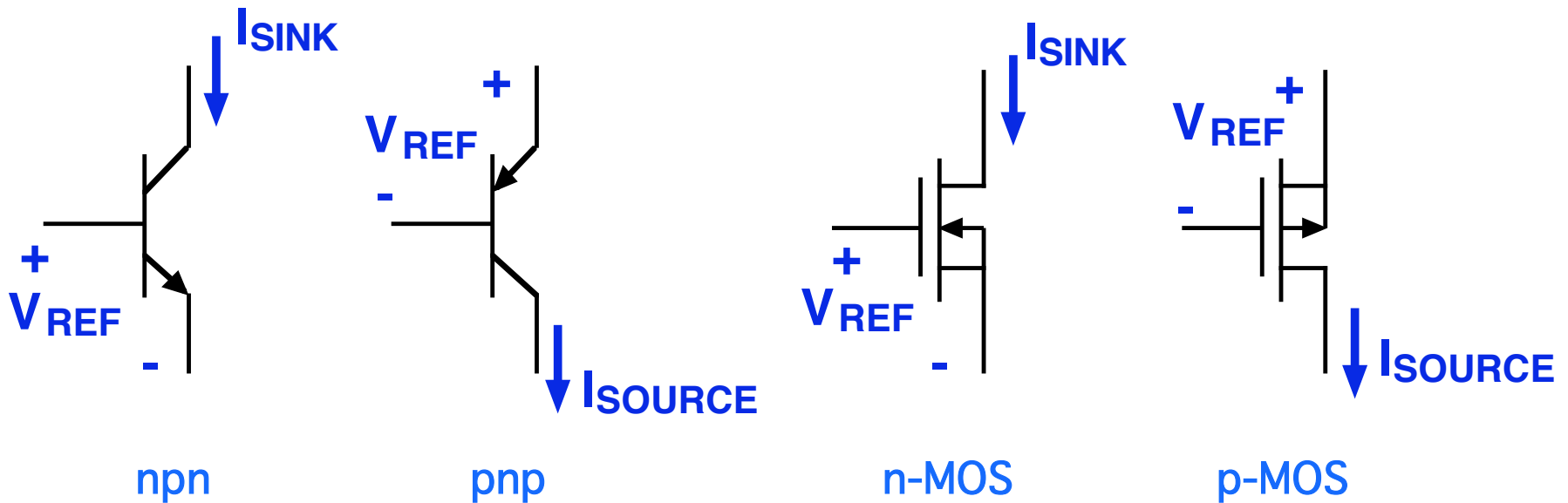


n-MOS



p-MOS

- Getting I_{BIAS} : Making a transistor into a current source/sink*



BJT current sources/sinks

Must maintain $V_{CE} > 0.2V$
 [V_{EC} in case of pnp]

$$I_{SOURCE/SINK} = \left[\frac{\beta_F}{\beta_F + 1} \right] I_{ES} (e^{qV_{REF}/kT} - 1)$$

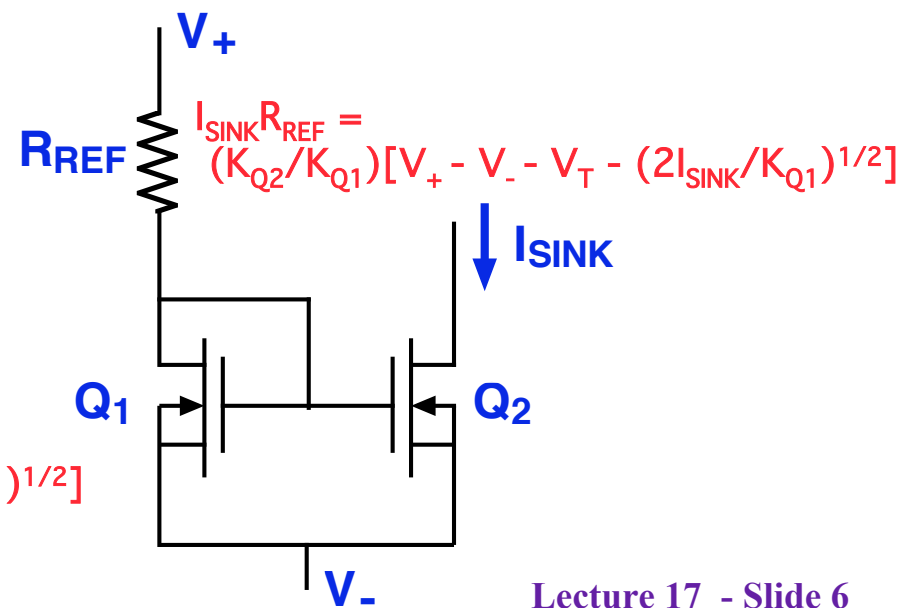
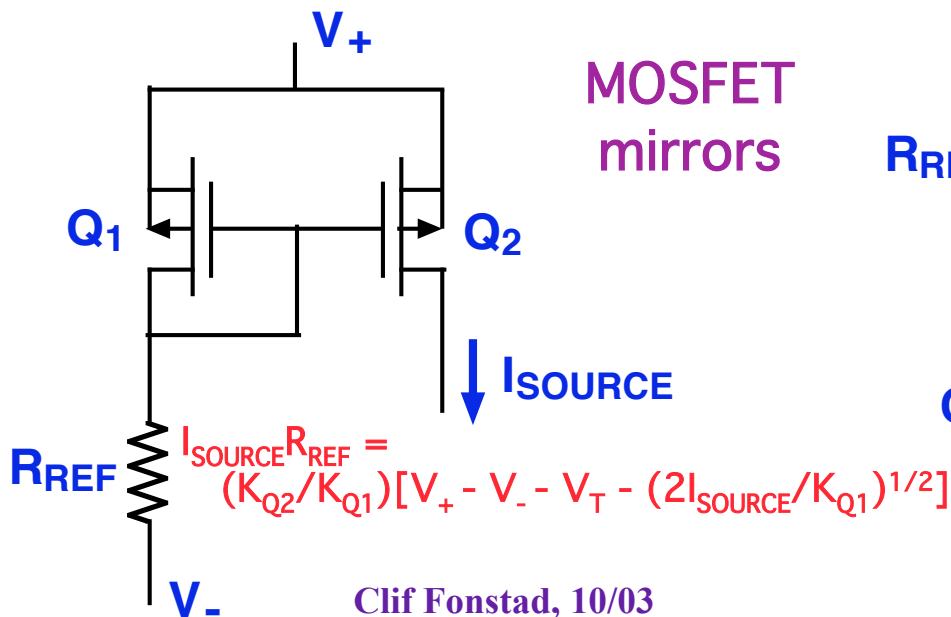
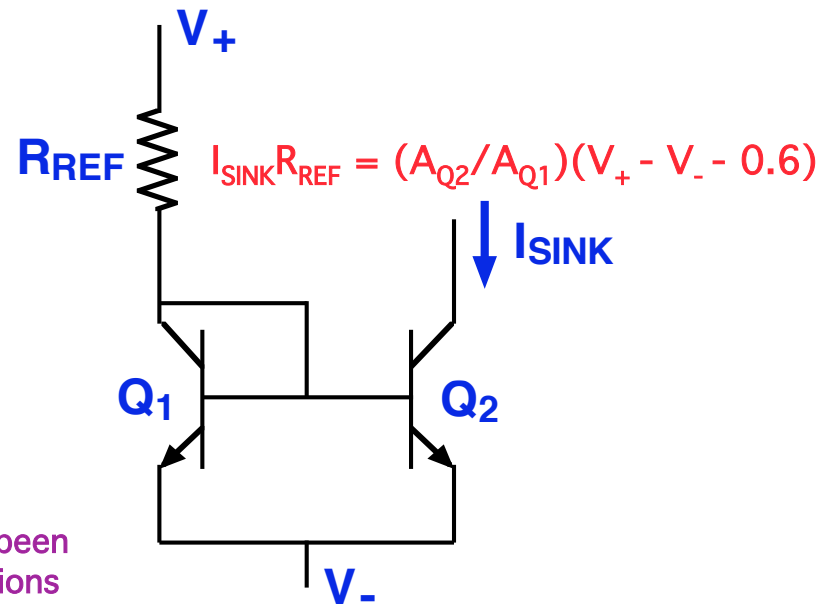
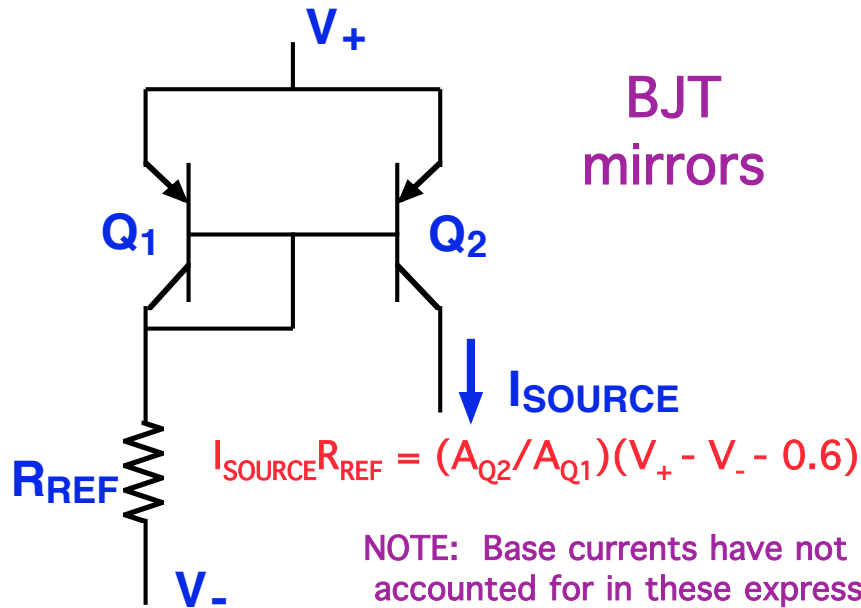
$$\approx I_{ES} e^{qV_{REF}/kT}$$

MOSFET current sources/sinks

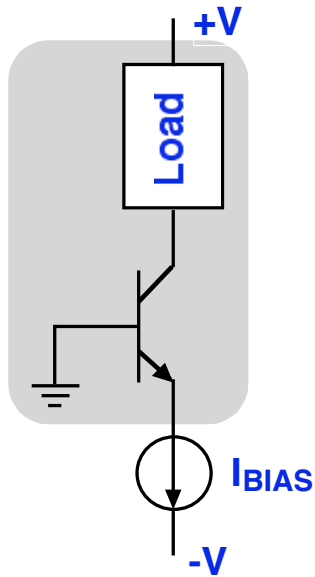
Must maintain $V_{DS} > (V_{REF} - V_T)$
 [$V_{SD} > (V_{REF} + V_T)$ in case of p-MOS]

$$I_{SOURCE/SINK} = K(V_{REF} - |V_T|)^2/2$$

- Current mirror sources and sinks

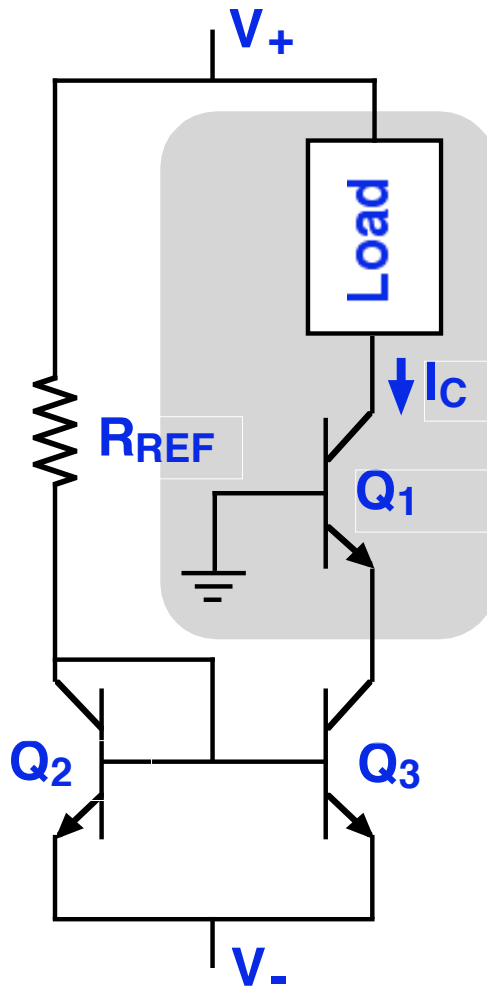


- Examples of current mirror biased BJT circuits:



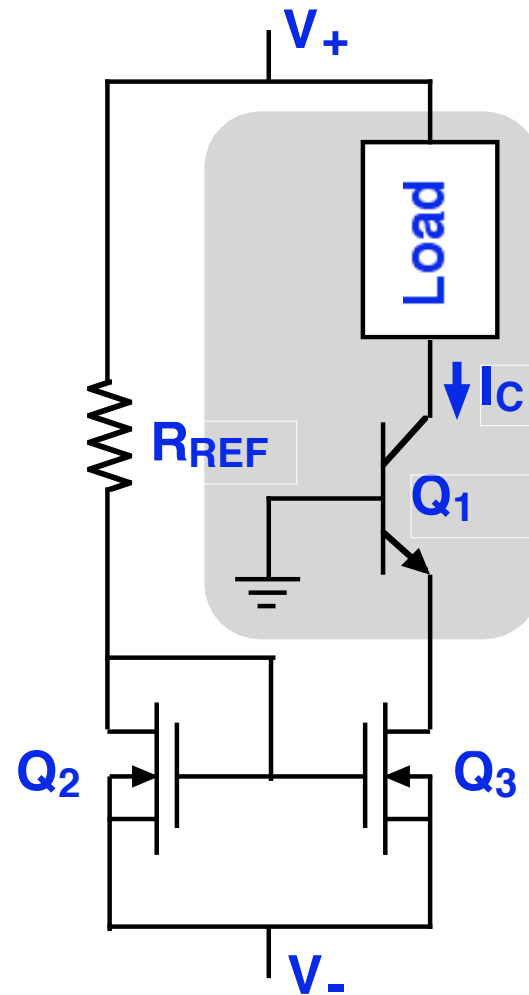
Above: Concept

Right: Implementations



BJT Mirror

$$I_C \approx (A_{Q3}/A_{Q2}) I_{REF}$$



MOSFET Mirror

$$I_C \approx (K_{Q3}/K_{Q2}) I_{REF}$$

- **Resistor biasing:** An older biasing techniques used in discrete circuits where transistors are expensive.

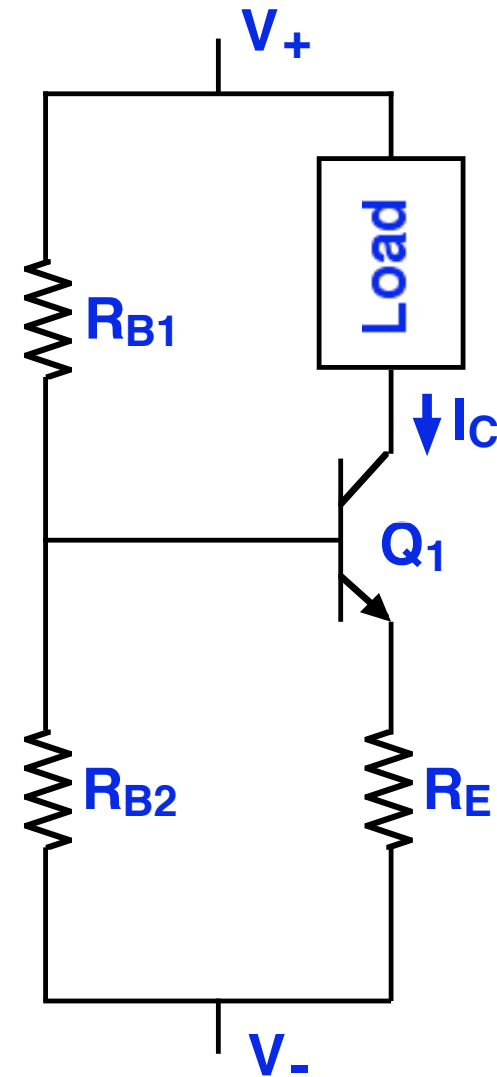
Resistor biasing

$$I_C \approx [(V_+ - V_-)R_{B2} / (R_{B1} + R_{B2}) - 0.6] / R_E$$

You might call this "poor man's current source biasing" because it uses three resistors and only one transistor. The resistor, R_E , with a constant voltage,

$(V_+ - V_-)R_{B2} / (R_{B1} + R_{B2}) - 0.6V$,
across it looks like a current source
of magnitude:

$$[(V_+ - V_-)R_{B2} / (R_{B1} + R_{B2}) - 0.6V] / R_E.$$

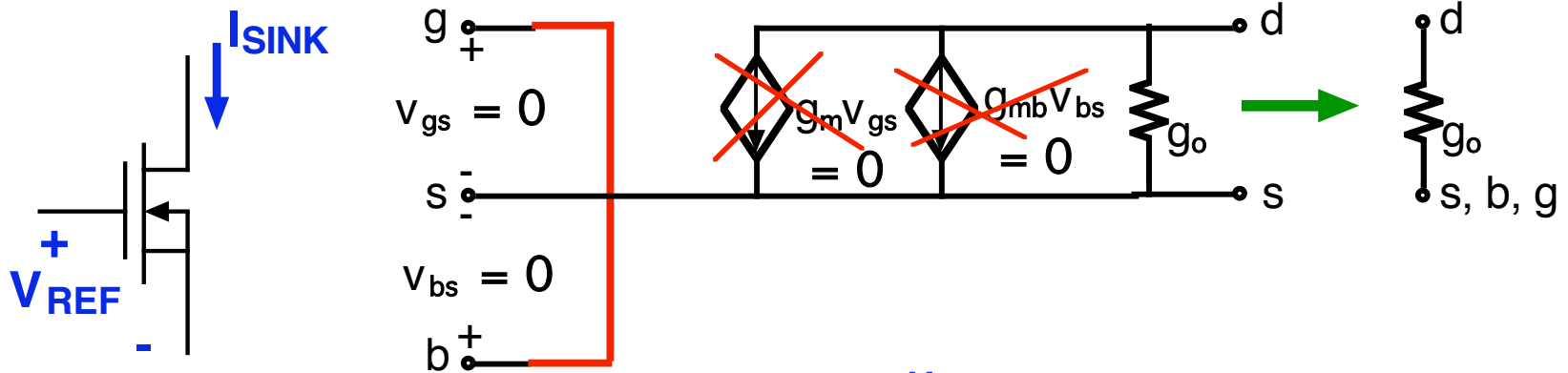


- Final comments on current sources:

What do they look like incrementally?

They look like a resistor with conductance g_o

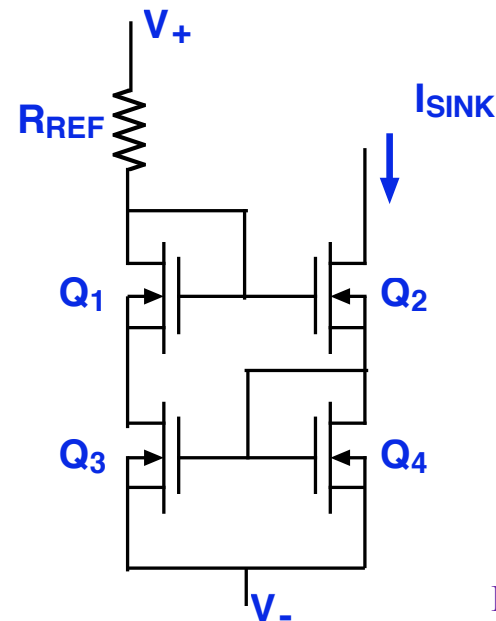
For example, consider an n-MOS sink:



How do you do better?

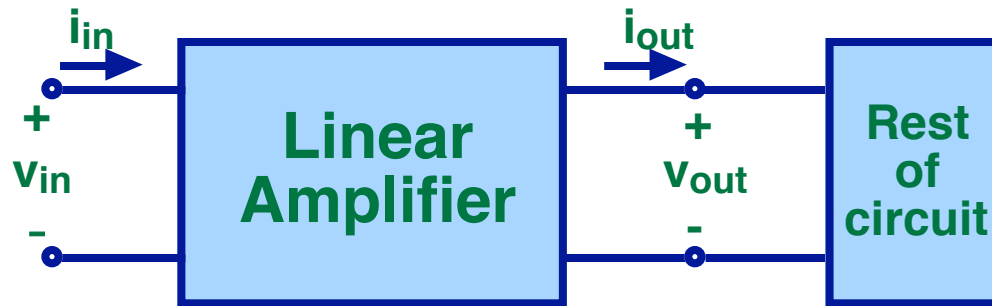
The Wilson connection:

check it out for yourself



- Linear amplifier performance metrics:

The characteristics of linear amplifiers that we use to compare different amplifier designs, and to judge their performance and suitability for a given application are given below:

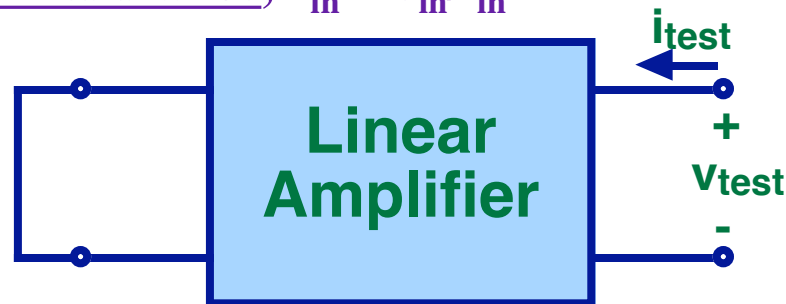


Voltage gain, $A_v = v_{out}/v_{in}$

Current gain, $A_i = i_{out}/i_{in}$

Power gain, $A_{power} = P_{out}/P_{in} = v_{out}i_{out}/v_{in}i_{in} = A_vA_i$

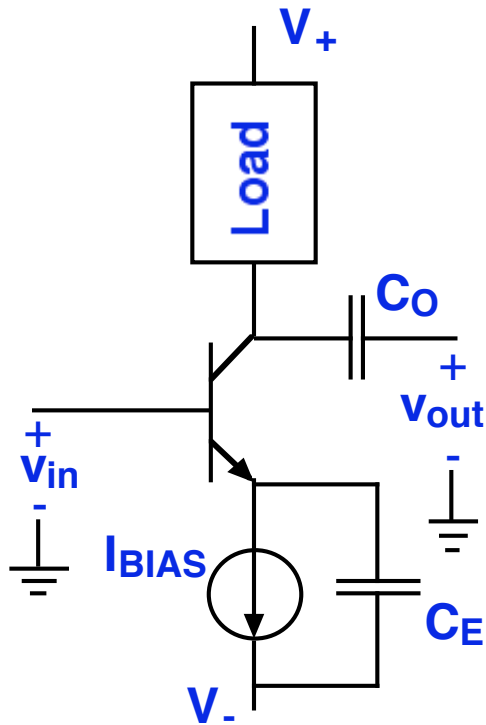
Input resistance, $r_{in} = v_{in}/i_{in}$



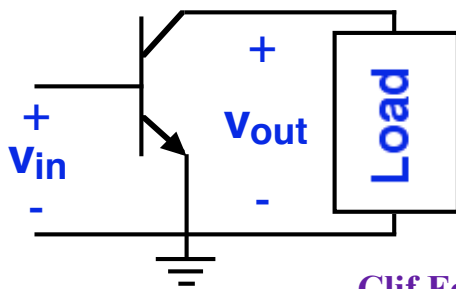
Output resistance, $r_{out} = v_{test}/i_{test}$ with $v_{in} = 0$

DC Power dissipation, $P_{DC} = (V_+ - V_-)(\sum I_{BIAS}'s)$

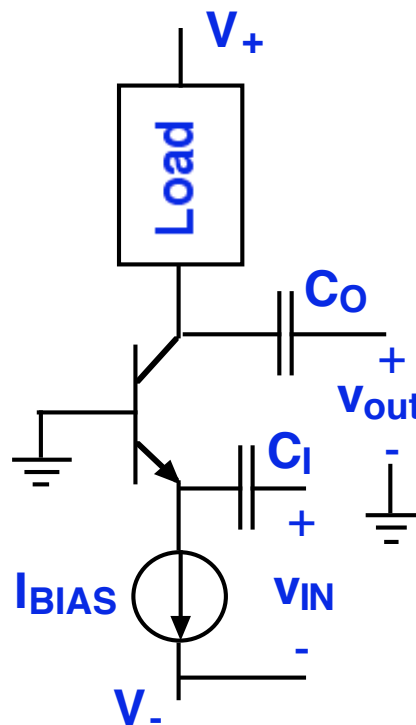
- **Three BJT single-transistor amplifiers**



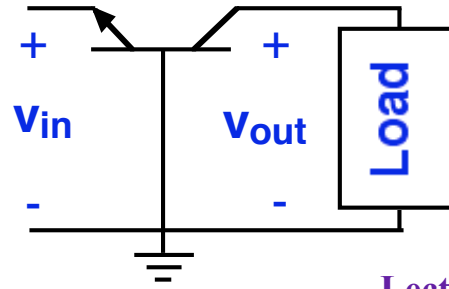
COMMON EMITTER
 Input: base
 Output: collector
 Common: emitter



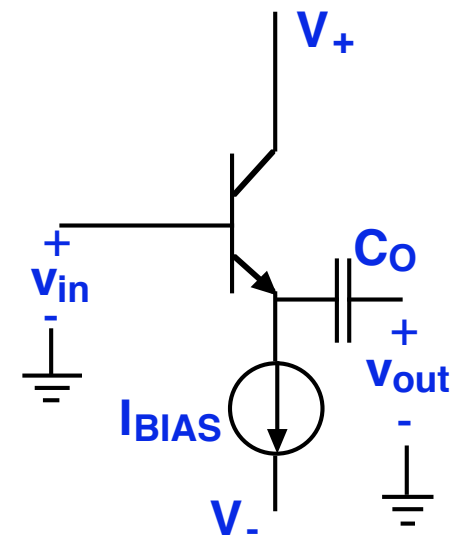
Clif Fonstad, 10/03



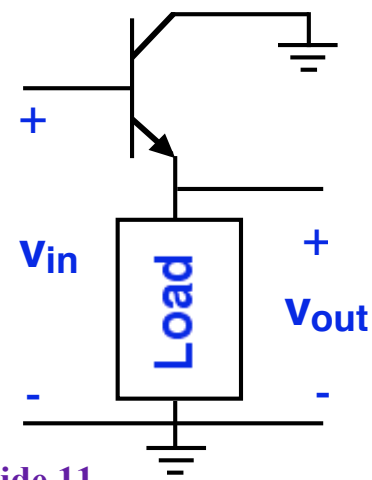
COMMON BASE
 Input: emitter
 Output: collector
 Common: base



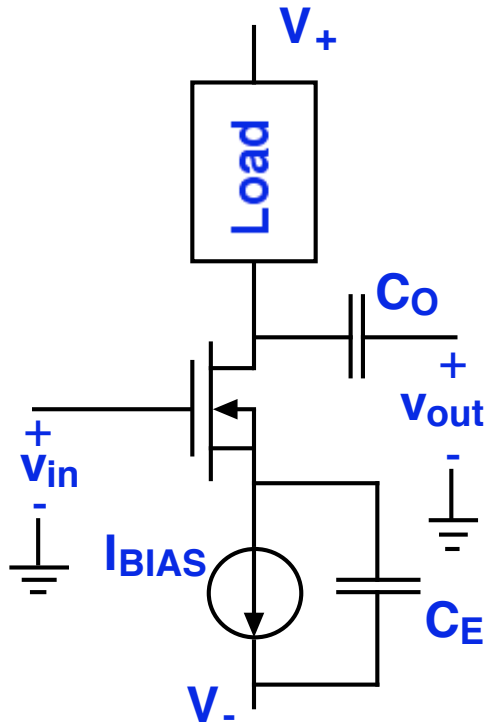
Lecture 17 - Slide 11



EMITTER FOLLOWER
 Input: base
 Output: emitter
 Common: collector

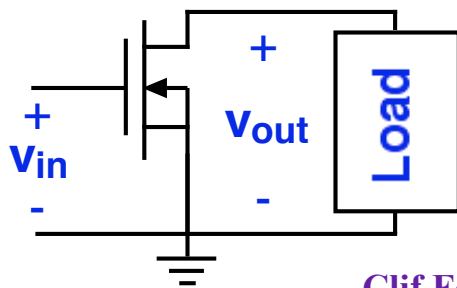


- **Three MOSFET single-transistor amplifiers**

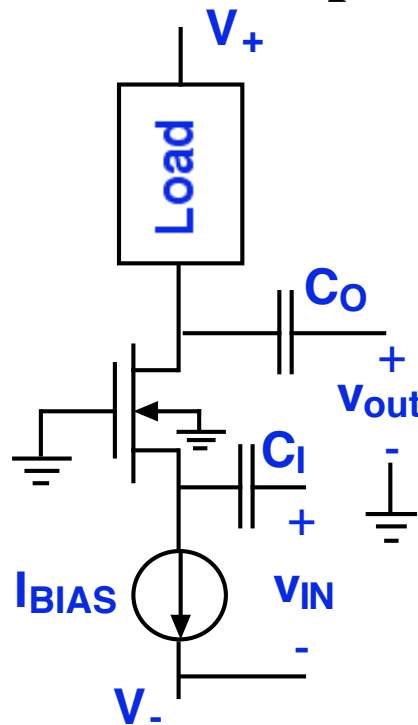


COMMON SOURCE

Input: gate
Output: drain
Common: source
Substrate: to source

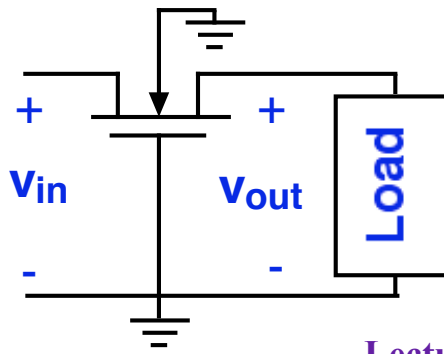


Clif Fonstad, 10/03

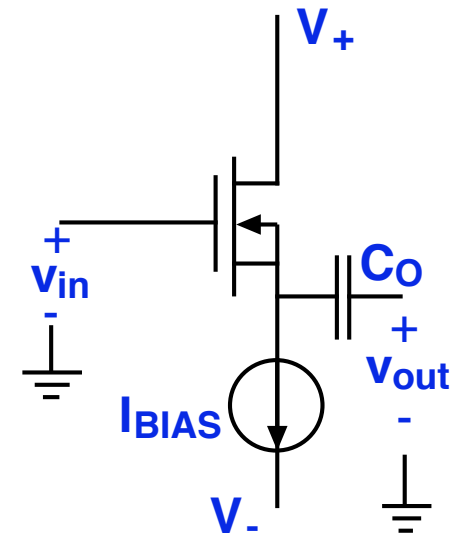


COMMON GATE

Input: source; Output: drain
Common: gate; Substrate: to ground

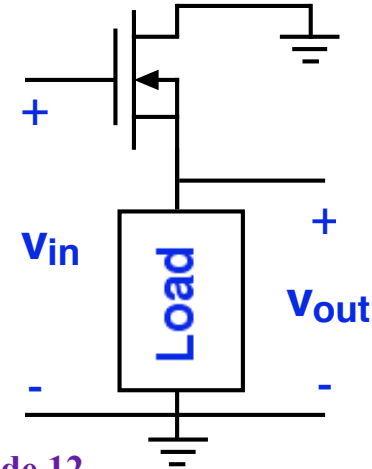


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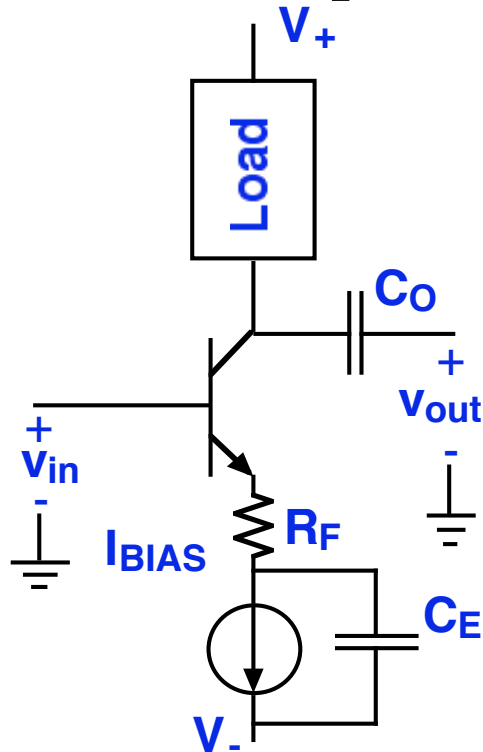


SOURCE FOLLOWER

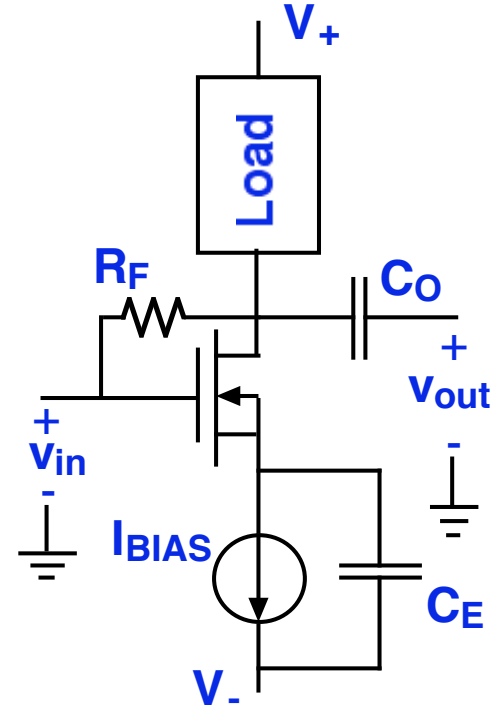
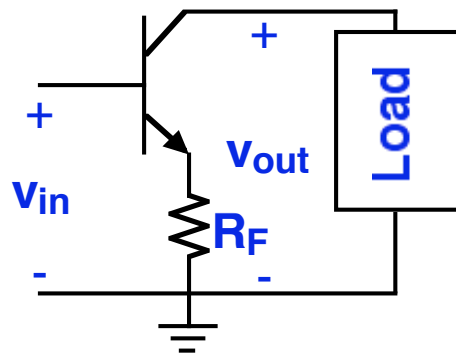
Input: gate
Output: source
Common: drain
Substrate: to source



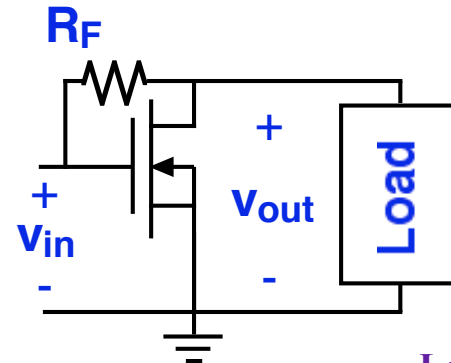
- Single-transistor amplifiers with feedback



Parallel feedback
also termed "emitter degeneration"



Series feedback



Lecture 17 - Linear Amplifier Basics - Summary

- **Biassing transistors**

Current source biasing: a current source is used to establish a stable bias pt.
large signals models are used in this analysis

Transistors as current sources: great as long as in saturation or FAR

Current mirror current sources and sinks: it takes one to know one

- **Linear amplifiers**

Performance metrics: gains (voltage, current, power)

$A_v = v_{out}/v_{in}$, $A_i = i_{out}/i_{in}$, $A_{power} = v_{out}i_{out}/v_{in}i_{in}$
input and output resistances

$r_{in} = v_{in}/i_{in}$, $r_{out} = v_{test}/i_{test}$ with $v_{in} = 0$
dc power dissipation: $(V_+ - V_-)(\sum I_{BIAS}'s)$

bandwidth (We'll save this for later - Lec. 22)

Possible amplifier connections of transistors:

Simple stages: Common emitter, common source
Common base, common gate
Emitter follower, Source follower

Stages with feedback: Parallel (Degeneracy in emitter/source)
Series