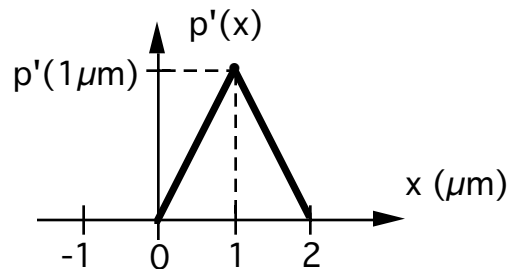


6.012 Fall 1998 - Answers to Exam #2

Problem 1

- a) Neglecting the depletion region, which we assumed you would do (and most of you did), the plot is as shown:



- b) Half of the injected minority carrier flux of MA flows to and across the junction and the other flows to the ohmic contact. The current I is minus the former multiplied by the charge per carrier; thus $I = -qMA/2$.
- c) Since many fewer minority carriers flow to the right, much more of the total injected minority carrier flux of MA must flow to the left and across the junction, meaning that the magnitude of I is now increased. In fact I is nearly $-qMA$. This "trick" is used in many photodiodes to increase the photocurrent and reduce undesirable recombination at ohmic contacts and device surfaces (which can look a bit like ohmic contacts in that they act as places of increased recombination).
- d) The charge on the gate varies nearly linearly with the gate voltage in accumulation, which occurs for $v_{GB} < V_{FB}$ in a MOS capacitor fabricated on a p-type substrate, and in inversion, which occurs for $v_{GB} > V_T$. In both cases the proportionality factor is the oxide capacitance, $\epsilon_{ox}A/t_{ox}$, which in this case is 3.5×10^{-11} Coul/V, or 35 pF.
- e) With the switch closed, v_{GB} is greater than V_T so the interface is inverted and the inversion layer charge is $-C_{ox}(v_{GB} - V_T)$, or -8.75×10^{-11} Coul.
- f) The diode is reverse biased for v_{GB} greater than zero, and for v_{GB} greater than a few kT the current through the reverse biased diode is a constant I_S . Thus it will look like a current source of this value for the v_{GB} range of interest, i.e. for $0.5 \text{ V} < v_{GB} < 3.0 \text{ V}$. Since we have a charge, Q , of 8.75 Coul to discharge and there is a current, I , discharging it at a rate of 10^{-12} Coul/s (the value of I_S), it will take Q/I , or 87.5 s to discharge the inversion layer charge and reach 0.5 V.

Problem 2

- a) If we short the collector-base junction in the Ebers-Moll model, the current i_R is zero so the emitter current, which is in general $-i_F + \alpha_R i_R$, is just $-i_F$. The emitter current is also the negative of the diode current, i_D , we are looking for so we have $i_D = i_F$. Since i_F is $I_{ES}[\exp(-qV_{BE}/kT) - 1]$, and v_{BE} is v_{AB} for the diode, we have

$$i_D = I_{ES}[\exp(-qV_{AB}/kT) - 1],$$

Thus $I_S = I_{ES} = 2 \times 10^{-13} \text{ A}$

- b) V_{REF} is the diode voltage at which i_D is 0.2 mA. Since this current is much larger than I_S we know that v_{AB} will be much greater than kT/q and we will be able to neglect the "1" in the $[\exp(-qV_{AB}/kT) - 1]$ term. V_{REF} thus satisfies

$$2 \times 10^{-4} = 2 \times 10^{-13} \exp(-qV_{REF}/kT)$$

which is to say

$$V_{REF} = \frac{kT}{q} \ln 10^9$$

Using our approximation that $(kT/q) \ln 10 = 60 \text{ mV}$, we have $V_{REF} = 0.54 \text{ V}$. (Not making this approximation you find $V_{REF} = 5.18 \text{ V}$.)

We can now calculate what R_R must be because we know the current through it, 0.2 mA, and the voltage drop across it, $(3.0 - 0.54)\text{V} = 2.46 \text{ V}$, leading to $R_R = V/I = 12,300 \text{ Ohms}$.

- c) i) In the forward active region the reverse current, i_R , in Q_2 can be neglected and its collector current (which is the I_2 you are asked to find) is $\alpha_F i_F$, where i_F is $I_{ES} [\exp(qV_{BE}/kT) - 1]$. But this is just the current through Q_1 since v_{BE} for Q_2 is V_{REF} , or 0.2 mA. Since α_F is 0.995, I_2 is 0.199 mA, or approximately 0.2 mA. Note: This circuit is called a "current mirror" since the current in Q_2 mirrors the current in Q_1 . We will use this idea to make current sources for biasing differential amplifier stages.
- ii) We must keep v_{CE} on Q_2 larger than 0.2V so that it doesn't become saturated, so the voltage drop across R_2 must be less than 2.8 V (i.e., $3\text{V} - 0.2\text{V}$). Since it has 0.2 mA flowing through it, its value must be less than $2.8\text{V}/0.2\text{mA}$, or 14,000 Ohms. There is no minimum value for R_2 , i.e., it can be zero.
- iii) If the area of Q_2 is twice that of Q_1 , its I_{ES} will be twice that of Q_1 's, all else being equal, and thus the current through it will be twice that through Q_1 , with v_{BE} the same in both devices. Thus I_2 will be very nearly 0.4 mA. This is how we can use one V_{REF} to set several different size current sources.

d) i) The same reasoning applies in this case as earlier, and thus I_2 is 0.2mA. (In fact, since there is no base current, it is as if we had α_F exactly equal to 1, and I_2 is now exactly 0.2 mA, not 0.995×0.2 mA, as in the bipolar parts of the question.)

ii) Q_1 is clearly in saturation since $v_{DS} > v_{GS} - V_T$ always when $v_{DS} = v_{GS}$ as it does for Q_1 . Thus V_{REF} is v_{GS} such that i_D is 0.2 mA, where i_D is given by

$$i_D = K(v_{GS} - V_T)^2/2$$

Thus we have

$$0.2 = 0.1 (V_{REF} - 0.5)^2/2$$

giving us

$$V_{REF} = 2.5 \text{ V}$$

As before, we find R_R by dividing the voltage drop across it, $3.0\text{V} - 2.5\text{V} = 0.5\text{V}$, by the current through it, 0.2 mA, giving us 2,500 Ohms.

iii) With K for Q_2 now three times larger, the current will be three times larger, or 0.6 mA.

Problem 3

a) i) The pull-down FET is off so i_{pD} is zero.

ii) v_{OUT} will increase to its maximum, which will be 0.6V because the diode at the input of the loading stage FET will limit it to V_{ON} (= 0.6V).

iii) The pull-up current, i_{pU} , will be determined by the voltage drop across the 400 Ohm pull-up resistor, which in this case is $1\text{V} - 0.6\text{V}$, or 0.4V. The pull-up current is clearly 1 mA.

iv) All of the pull-up current flows into the load FET gate, so $i_{sL} = i_{pU} = 1\text{mA}$.

b) i) If v_{OUT} is 0.2V the diode in the gate circuit of the load FET will not be conducting and i_{sL} will be zero.

ii) The pull-down current, i_{pD} , will now be equal the pull-up current, i_{pU} , since i_{sL} is zero, and i_{pU} is the current through a 400 Ohm resistor with a voltage drop across it of $1\text{V} - 0.2\text{V}$, or 0.8V. Thus i_{pD} is now 2 mA.

iii) The MOSFET is just in saturation because $v_{GS} - V_T = v_{IN} - V_T = 0.2 \text{ V}$, and $v_{DS} = v_{OUT} = 0.2 \text{ V}$. Thus we can write

$$i_{pD} = 0.2 \text{ mA} = K(0.2)^2/2$$

and solve to find

$$K = 100 \text{ mA/V}^2$$

- c) i) When $v_{IN} < V_T$, the pull-up current, which is the total current per stage coming from the power supply, is 1 mA, and thus the power being dissipated is $1\text{mA} \times 1\text{V} = 1\text{mW}$.
- ii) When $v_{IN} = 0.6\text{V}$ and $v_{OUT} = 0.2\text{V}$, i_{PU} is 2 mA, so the power being dissipated is 2 mW.
- iii) The average power is the average of the two values just calculated, or 1.5 mW.

Exam 1 Statistics:

Average:	77.3
Standard Deviation:	17.9
Number taking exam:	55

Distribution:

