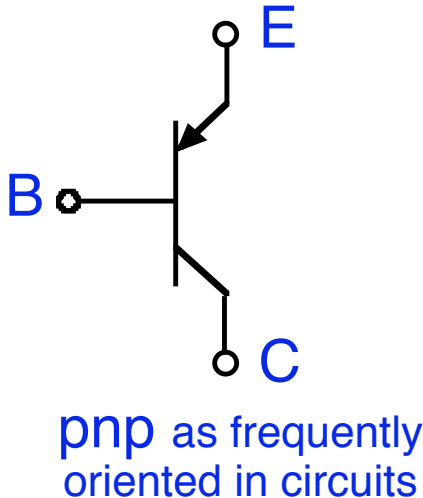
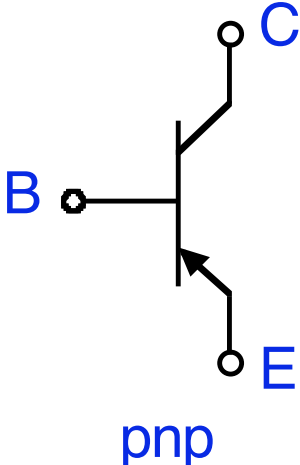
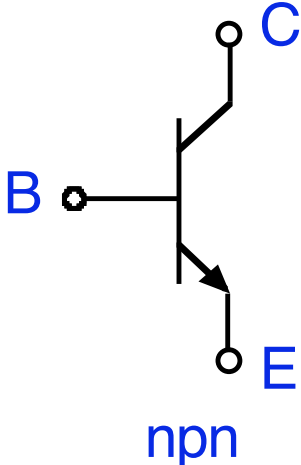


## Lecture 14 - Linear Equivalent Circuits - Outline

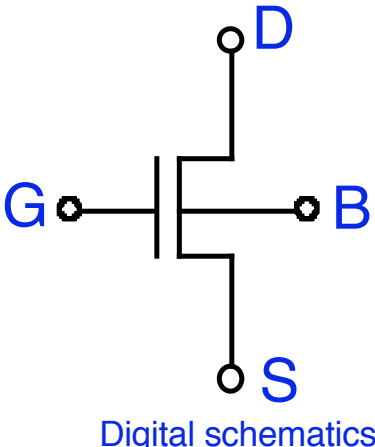
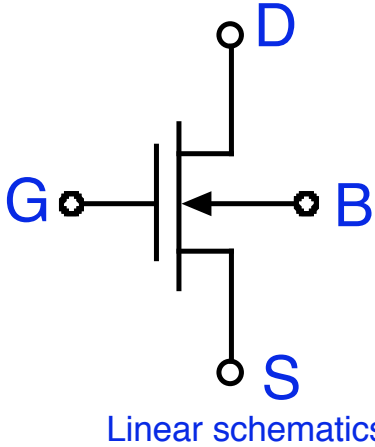
- **Announcements**
  - Handout - Lecture Outline and Summary**
- **Review - Adding refinements to large signal models**
  - Charge stores: depletion regions, excess carriers, gate charge**
  - Active-length modulation: the Early effect**
  - Extrinsic parasitics: Lead resistances, capacitances, and inductances**
- **Small signal models**
  - What are they good for?**
- **Linear equivalent circuits**
  - pn diodes: linearizing the exponential diode**  
**incorporating the charge stores**
  - BJTs: linearizing the Ebers-Moll model**  
**incorporating the charge stores**  
**adding the Early effect and possible parasitics**
  - MOSFETs: linearizing the Gradual-Channel model**  
**incorporating the charge stores**  
**adding the Early effect and possible parasitics**

# Circuit symbols:

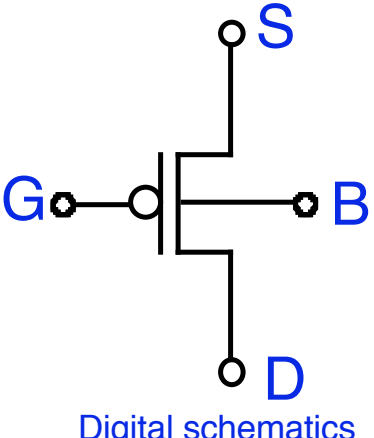
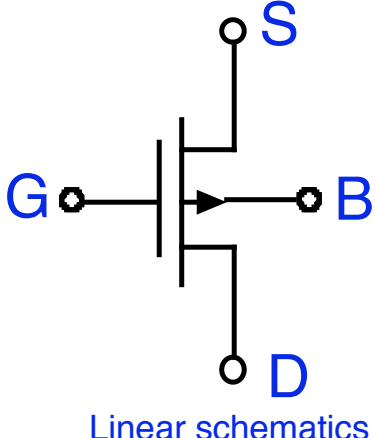
BJT:



MOSFET:



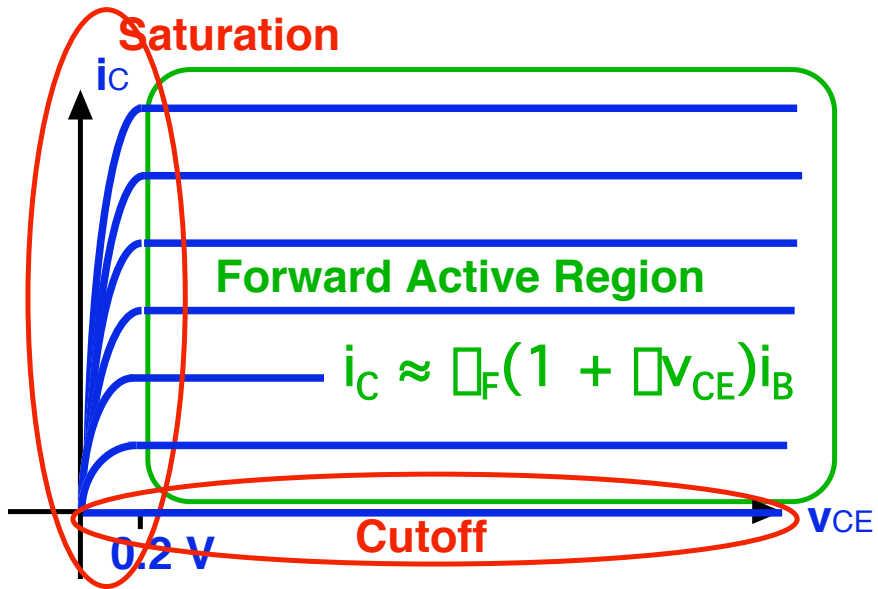
n-channel



p-channel (usual circuit orientation)

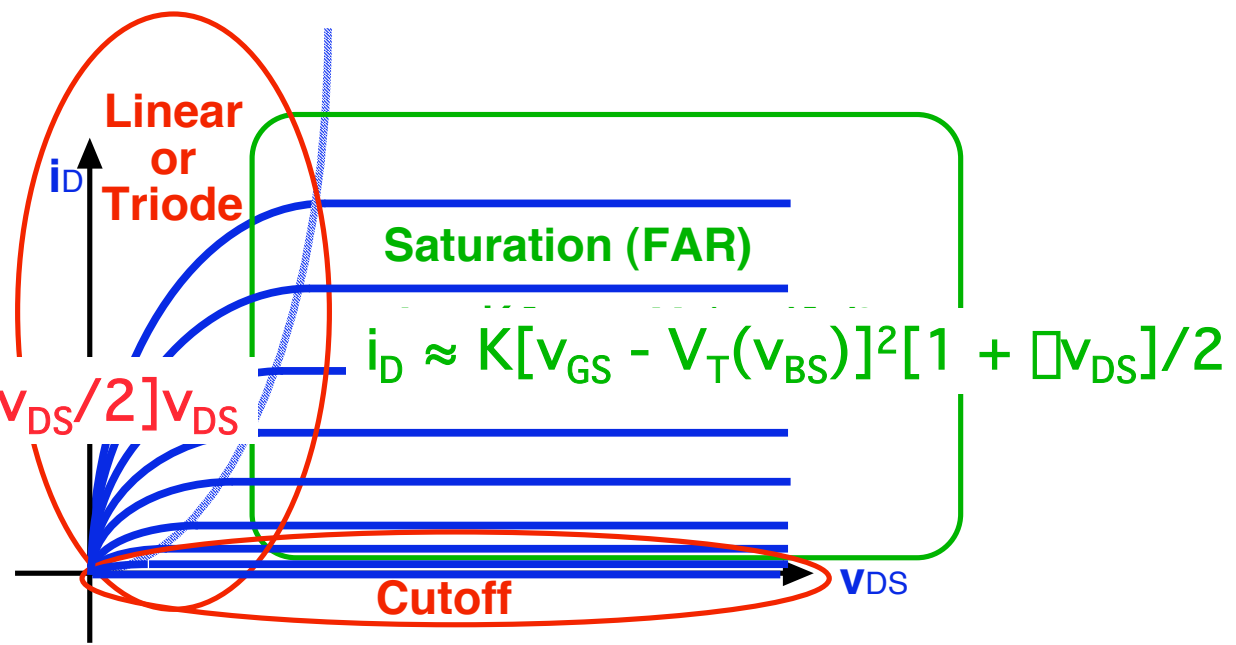
# Output Characteristics

BJT: npn



MOSFET:  
n-channel

$$i_D \approx K[v_{GS} - V_T(v_{BS}) - v_{DS}/2]v_{DS}$$



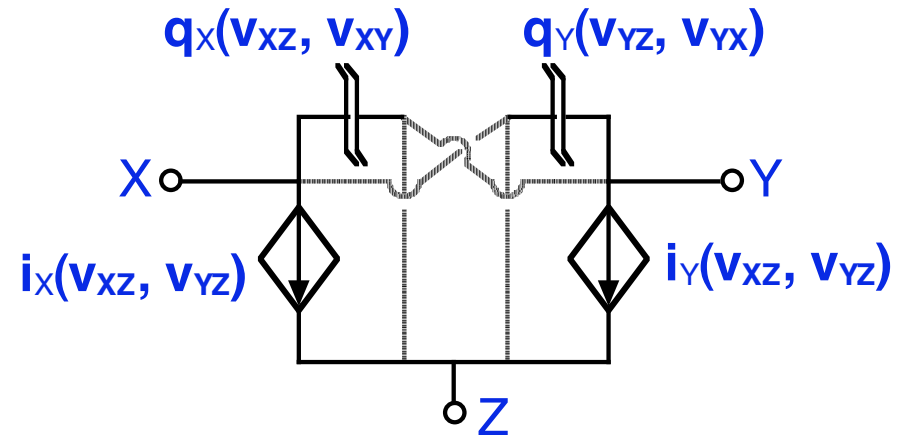
- **Creating a linear equivalent circuit, LEC:**

Suppose we have a device with three terminals, X, Y, and Z, and that we have expressions for the currents into terminals X and Y in terms of the voltages  $v_{XZ}$  and  $v_{YZ}$ :

$$i_X(v_{XZ}, v_{YZ}) \quad \text{and} \quad i_Y(v_{XZ}, v_{YZ})$$

Suppose we also have expressions for the charge stores associated with terminals X and Y:

$$q_X(v_{XZ}, v_{YZ}) \quad \text{and} \quad q_Y(v_{XZ}, v_{YZ})$$



We begin with the static model for the terminal characteristics, and linearize them about an bias point,  $Q$ , defined as a specific set of  $v_{XZ}$  and  $v_{YZ}$  that we write, using our notation, as  $V_{XZ}$  and  $V_{YZ}$

For example, for the current into terminal X we have:

$$i_X(v_{XZ}, v_{YZ}) = i_X(V_{XZ}, V_{YZ}) + \left. \frac{\partial i_X}{\partial v_{XZ}} \right|_Q (v_{XZ} - V_{XZ}) + \left. \frac{\partial i_X}{\partial v_{YZ}} \right|_Q (v_{YZ} - V_{YZ}) + \text{higher order terms}$$

For sufficiently small  $(v_{XZ} - V_{XZ})$  and  $(v_{YZ} - V_{YZ})$ , we have:

$$i_X(v_{XZ}, v_{YZ}) \approx i_X(V_{XZ}, V_{YZ}) + \left. \frac{\partial i_X}{\partial v_{XZ}} \right|_Q (v_{XZ} - V_{XZ}) + \left. \frac{\partial i_X}{\partial v_{YZ}} \right|_Q (v_{YZ} - V_{YZ})$$

- **Creating a linear equivalent circuit, LEC, cont.:**

Using our notation, we recognize that:

$$I_X \equiv i_X(V_{XZ}, V_{YZ}), \quad i_x \equiv [i_X \square I_X], \quad v_{xz} \equiv [v_{XZ} \square V_{XZ}], \quad v_{yz} \equiv [v_{YZ} \square V_{YZ}]$$

We identify the partial derivatives as conductances, and name them as:

$$\left. \frac{\partial i_X}{\partial v_{XZ}} \right|_Q \equiv g_i \quad \left. \frac{\partial i_X}{\partial v_{YZ}} \right|_Q \equiv g_r$$

Applying these to our earlier result we have, first:

$$i_X(v_{XZ}, v_{YZ}) \square I_X + \left. \frac{\partial i_X}{\partial v_{XZ}} \right|_Q v_{xz} + \left. \frac{\partial i_X}{\partial v_{YZ}} \right|_Q v_{yz}$$

and finally:

$$i_x(v_{xz}, v_{yz}) \square g_i v_{xz} + g_r v_{yz}$$

Doing the same for  $i_Y$ , we arrive at

$$i_y(v_{xz}, v_{yz}) \square g_f v_{xz} + g_o v_{yz}$$

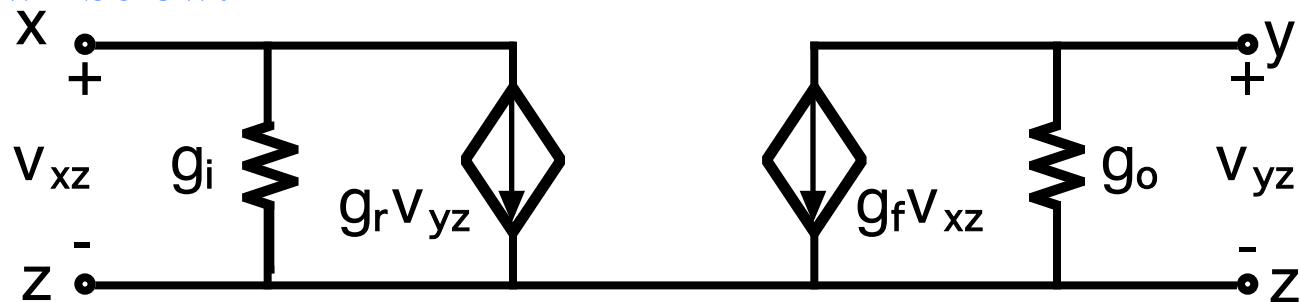
where:

$$g_f \equiv \left. \frac{\partial i_Y}{\partial v_{XZ}} \right|_Q \quad g_o \equiv \left. \frac{\partial i_Y}{\partial v_{YZ}} \right|_Q$$

continued on the next page

- **Creating a linear equivalent circuit, LEC, cont.:**

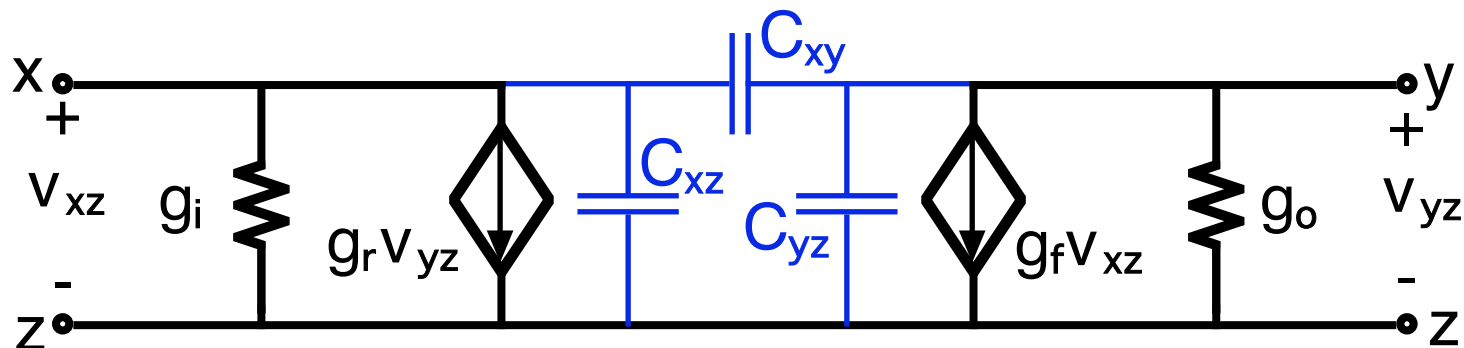
A circuit showing relating the incremental currents and voltages is shown below:



Next, to handle high frequency signals, we linearize the charge stores' dependencies on voltage. Their LECs, which are linear capacitors:

$$\left. \frac{\partial q_X}{\partial v_{XZ}} \right|_Q \equiv C_{xz} \quad \left. \frac{\partial q_Y}{\partial v_{YZ}} \right|_Q \equiv C_{yz} \quad \left. \frac{\partial q_X}{\partial v_{XY}} \right|_Q \equiv C_{xy} = \left. \frac{\partial q_Y}{\partial v_{YX}} \right|_Q$$

Adding these to the model gives us:



- **Linear equivalent circuit (LEC) for the p-n junction diode:**

We begin with the static model for the terminal characteristics:

$$i_D(v_{AB}) = I_{BS} \left[ e^{qv_{AB}/kT} - 1 \right]$$

Linearizing  $i_D$  about  $V_{AB}$ , which we will denote by  $Q$  (for quiescent bias point):

$$i_D(v_{AB}) \approx i_D(V_{AB}) + \left. \frac{\partial i_D}{\partial v_{AB}} \right|_Q [v_{AB} - V_{AB}]$$

We define the equivalent incremental conductance of the diode,  $g_d$ , as:

$$g_d \equiv \left. \frac{\partial i_D}{\partial v_{AB}} \right|_Q = \frac{q}{kT} I_{BS} e^{qV_{AB}/kT} \approx \frac{qI_D}{kT}$$

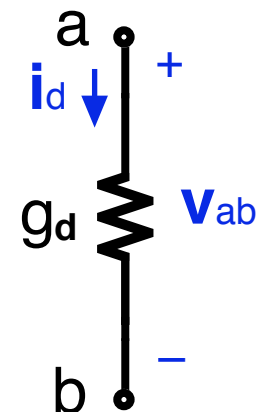
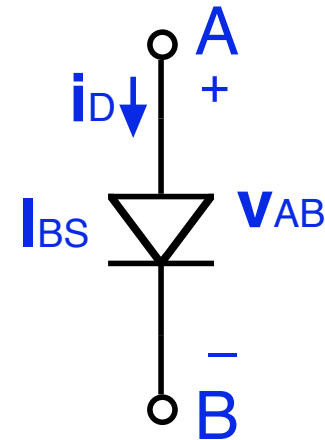
and we use our notation to write:

$$I_D = i_D(V_{AB}), \quad i_d = [i_D - I_D], \quad v_{ab} = [v_{AB} - V_{AB}]$$

ending up with

$$i_d = g_d v_{ab}$$

The corresponding LEC is shown at right:  $g_d \approx \frac{qI_D}{kT}$



- **LEC for the p-n junction diode, cont.:**

At high frequencies we must include the charge store,  $q_{AB}$ , and linearize its two components:

$$q_{AB} = q_{DP} + q_{QNR,p\text{-side}} \quad C_d = C_{dp} + C_{df}$$

Depletion layer charge store,  $q_{DP}$ , and its linear equivalent capacitance,  $C_{dp}$ :

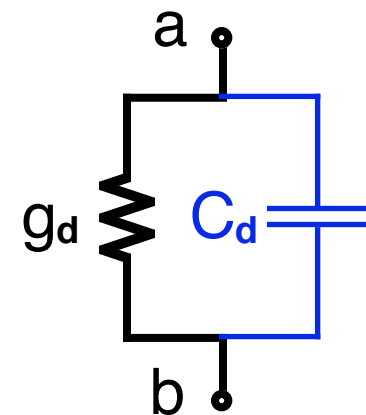
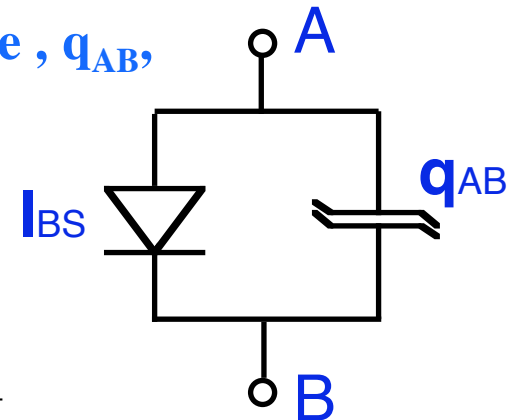
$$q_{DP}(v_{AB}) = AqN_{Ap}x_p(v_{AB}) = A\sqrt{2q\epsilon_{Si}N_{Ap}(\phi_b - v_{AB})}$$

$$C_{dp}(V_{AB}) \equiv \left. \frac{\partial q_{DP}}{\partial v_{AB}} \right|_Q = A\sqrt{\frac{q\epsilon_{Si}N_{Ap}}{2(\phi_b - V_{AB})}}$$

Diffusion charge store,  $q_{QNR,p\text{-side}}$ , and its linear equivalent capacitance,  $C_{df}$ :

$$q_{QNR,p\text{-side}}(v_{AB}) = \frac{i_D [w_p - x_p]^2}{2D_e}$$

$$C_{df}(V_{AB}) \equiv \left. \frac{\partial q_{QNR,p\text{-side}}}{\partial v_{AB}} \right|_Q = \frac{qI_D}{kT} \frac{[w_p - x_p]^2}{2D_e} = g_d \tau_d \quad \text{with} \quad \tau_d \equiv \frac{[w_p - x_p]^2}{2D_e}$$



- **Linear equivalent circuit for the BJT (static):**

In the forward active region, our static model says:

$$i_B(v_{BE}, v_{CE}) = I_{BS} \left[ e^{qv_{BE}/kT} - 1 \right]$$

$$i_C(v_{BE}, v_{CE}) = \beta_o [1 + \beta_o v_{CE}] i_B(v_{BE}, v_{CE}) = \beta_o I_{BS} \left[ e^{qv_{BE}/kT} - 1 \right] [1 + \beta_o v_{CE}]$$

We begin by linearizing  $i_C$  about Q:

$$i_c(v_{be}, v_{ce}) = \left. \frac{\partial i_C}{\partial v_{BE}} \right|_Q v_{be} + \left. \frac{\partial i_C}{\partial v_{CE}} \right|_Q v_{ce} = g_m v_{be} + g_o v_{ce}$$

We introduced the transconductance,  $g_m$ , and the output conductance,  $g_o$ , defined as:

$$\underline{g_m} \equiv \left. \frac{\partial i_C}{\partial v_{BE}} \right|_Q \quad \underline{g_o} \equiv \left. \frac{\partial i_C}{\partial v_{CE}} \right|_Q$$

Evaluating these partial derivatives using our expression for  $i_C$ , we find:

$$g_m = \frac{q}{kT} \beta_o I_{BS} e^{qv_{BE}/kT} [1 + \beta_o v_{CE}] \left[ \frac{qI_C}{kT} \right]$$

$$g_o = \beta_o I_{BS} \left[ e^{qv_{BE}/kT} + 1 \right] \left[ \beta_o I_C \right] \quad \text{or} \quad \frac{I_C}{V_A}$$

- **LEC for the BJT (static), cont.:**

Turning next to  $i_B$ , we note it only depends on  $v_{BE}$  so we have:

$$i_b(v_{be}) = \left. \frac{\partial i_B}{\partial v_{BE}} \right|_Q v_{be} = g_{\pi} v_{be}$$

The input conductance,  $g_{\pi}$ , is defined as:

$$g_{\pi} \equiv \left. \frac{\partial i_B}{\partial v_{BE}} \right|_Q$$

To evaluate  $g_{\pi}$  we do not use our expression for  $i_B$ , but instead use

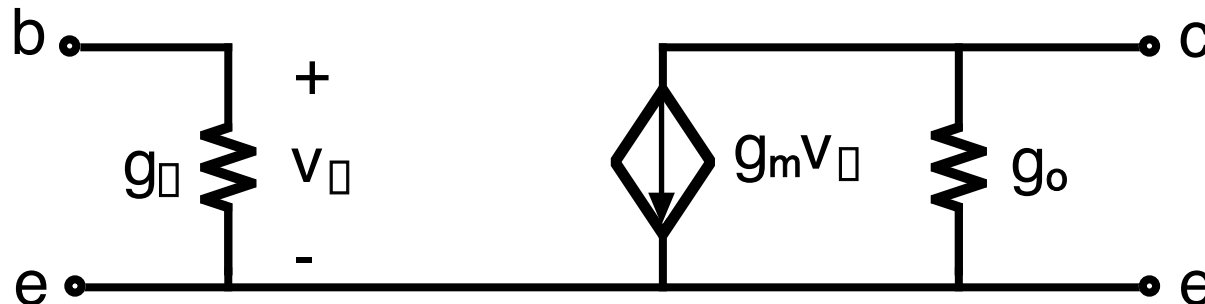
$$i_B = i_C / \beta_o$$

$$g_{\pi} \equiv \left. \frac{\partial i_B}{\partial v_{BE}} \right|_Q = \frac{1}{\beta_o} \left. \frac{\partial i_B}{\partial v_{BE}} \right|_Q = \frac{g_m}{\beta_o} = \frac{q I_C}{\beta_o k T}$$

(Notice that we do not define  $g_{\pi}$  as  $qI_B/kT$ )

Representing this as a circuit we have:

(Notice that  $v_{be}$  has been renamed  $v_{\pi}$ )

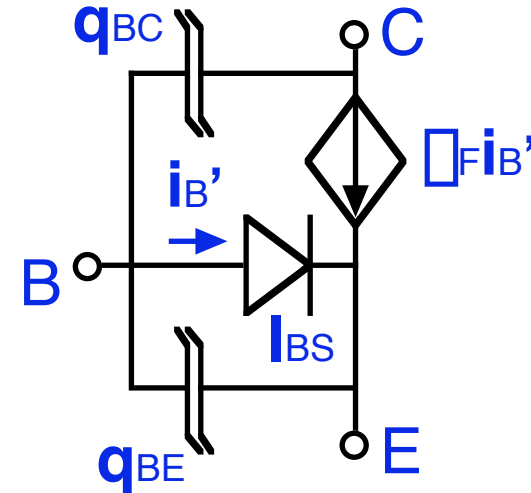


- **Linear equivalent circuit for the BJT (dynamic):**

To complete the model we next linearize and add the charge stores associated with the two junctions.

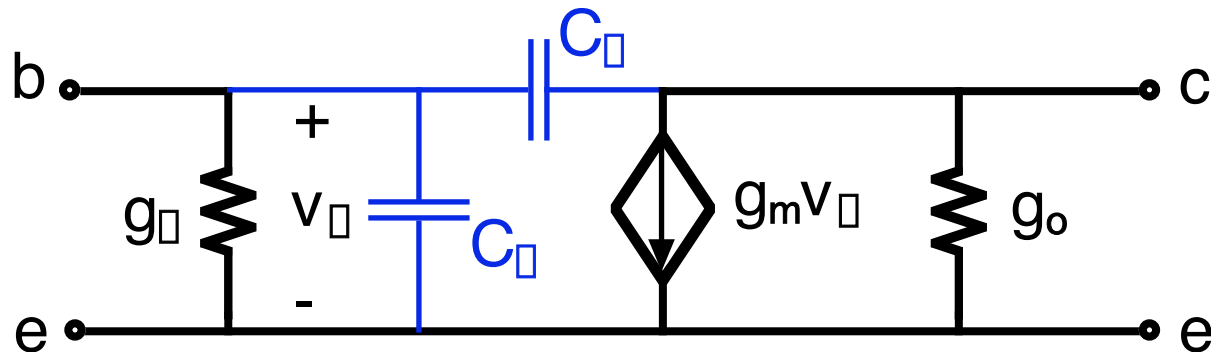
The base-collector junction is reverse biased so the charge associated with it,  $q_{BC}$ , is the depletion region charge. The corresponding capacitance is labeled  $C_{\square}$ .

The base-emitter junction is forward biased as has the excess charge injected into the base as well as the base-emitter depletion charge store associated with it. The linear equivalent capacitance is labeled  $C_{\square}$ . The part of  $C_{\square}$  due to the excess charge turns out to be  $qI_C/w_B^2/2D_e kT$ , which can also be written  $g_m \tau_b$  with  $\tau_b = w_B^2/2D_e$



**Summarizing:**  $C_{\square} = g_m \tau_b + \text{B-E depletion cap.}$ ,  $C_{\square}$ : B-C depletion cap.

Adding these C's to our model:



- **Linear equivalent circuit for the MOSFET (static):**

**In saturation, our static model is:**

(We've said  $\lambda = 1$ )

$$i_G(v_{GS}, v_{DS}, v_{BS}) = 0 \quad i_B(v_{GS}, v_{DS}, v_{BS}) = 0$$

$$i_D(v_{GS}, v_{DS}, v_{BS}) = \frac{K}{2} [v_{GS} - V_T(v_{BS})]^2 [1 + \lambda v_{DS}]$$

$$\text{with } K \equiv \frac{W}{L} \mu_e C_{ox}^* \text{ and } V_T(v_{BS}) \equiv V_{FB} - 2\phi_{p-Si} + \frac{1}{C_{ox}^*} \left\{ 2\phi_{Si} q N_A \left[ 2\phi_{p-Si} | \phi_{BS} \right] \right\}^{1/2}$$

**Note that because  $i_G$  and  $i_B$  are zero they are already linear, and we can focus on  $i_D$ . Linearizing  $i_D$  about Q we have:**

$$\begin{aligned} i_d(v_{gs}, v_{ds}, v_{bs}) &= \left. \frac{\partial i_D}{\partial v_{GS}} \right|_Q v_{gs} + \left. \frac{\partial i_D}{\partial v_{DS}} \right|_Q v_{ds} + \left. \frac{\partial i_D}{\partial v_{BS}} \right|_Q v_{bs} \\ &= g_m v_{gs} + g_o v_{ds} + g_{mb} v_{bs} \end{aligned}$$

**We have introduced the transconductance,  $g_m$ , output conductance,  $g_o$ , and substrate transconductance,  $g_{mb}$ :**

$$g_m \equiv \left. \frac{\partial i_D}{\partial v_{GS}} \right|_Q \quad g_o \equiv \left. \frac{\partial i_D}{\partial v_{DS}} \right|_Q \quad g_{mb} \equiv \left. \frac{\partial i_D}{\partial v_{BS}} \right|_Q$$

(Continued on next foil.)

- **LEC for the MOSFET (static), cont.:**

Evaluating the conductances using our expression for  $i_D$ , we find:

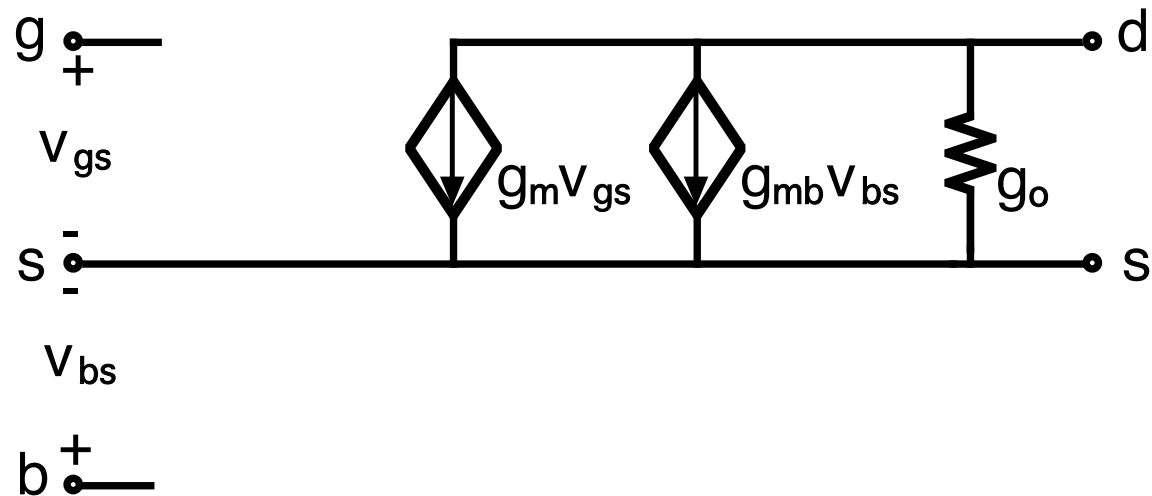
$$\underline{g_m} \equiv \left. \frac{\partial i_D}{\partial v_{GS}} \right|_Q = K[V_{GS} - V_T(V_{BS})][1 + \lambda V_{DS}] \sqrt{2KI_D}$$

$$\underline{g_o} \equiv \left. \frac{\partial i_D}{\partial v_{DS}} \right|_Q = \frac{K}{2}[V_{GS} - V_T(V_{BS})]^2 \lambda \quad \text{or} \quad \frac{I_D}{V_A}$$

$$\underline{g_{mb}} \equiv \left. \frac{\partial i_D}{\partial v_{BS}} \right|_Q = \lambda K[V_{GS} - V_T(V_{BS})][1 + \lambda V_{DS}] \left. \frac{\partial V_T}{\partial v_{BS}} \right|_Q = \lambda g_m = \lambda \sqrt{2KI_D}$$

$$\text{with } \lambda \equiv \left. \frac{\partial V_T}{\partial v_{BS}} \right|_Q = \frac{1}{C_{ox}^*} \sqrt{\frac{\epsilon_{Si} q N_A}{q \epsilon_p |V_{BS}}}$$

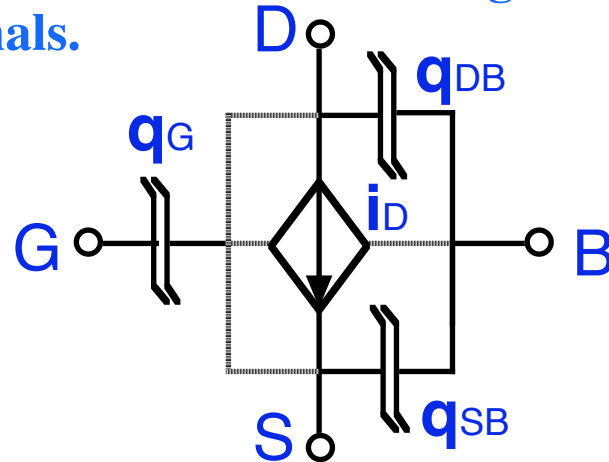
Representing this as a circuit we have:



- **Linear equivalent circuit for the MOSFET (dynamic):**

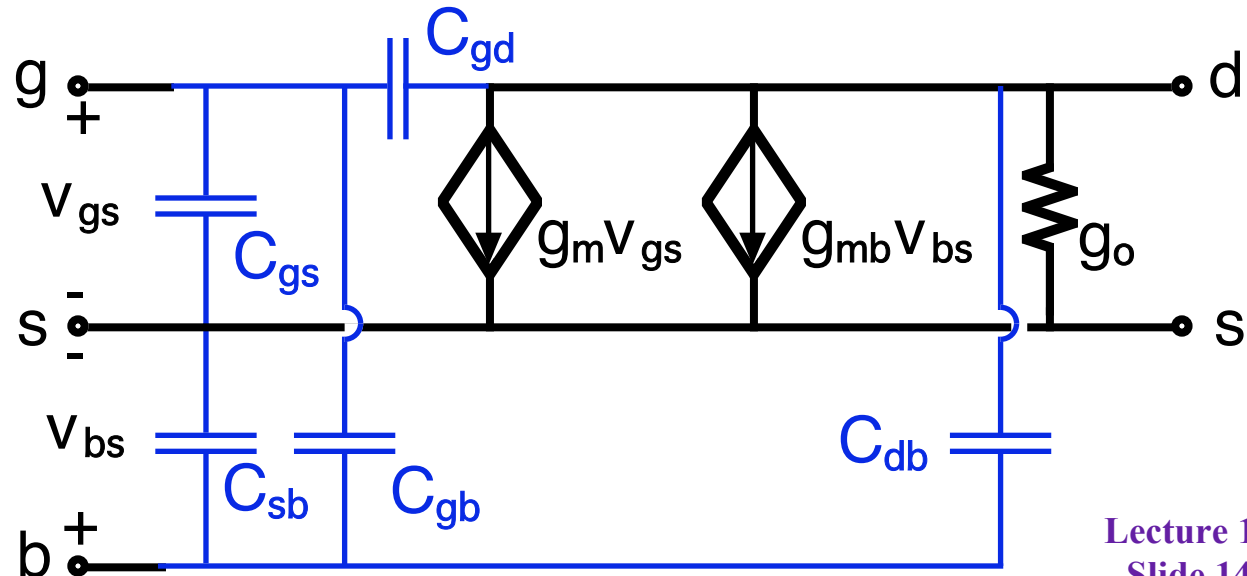
To complete the model we next linearize and add the charge stores associated with each pair of terminals.

In saturation  $q_G$  is a function only of  $v_{GS}$  and  $v_{GB}$ , so our model only accounts for  $C_{gs}$  and  $C_{gb}$ .  $C_{gd}$  is a parasitic element.



**We have:**  $C_{gs} = (2/3) WL C_{ox}^*$   
 $C_{gd}$ : sum of G-D fringing and overlap capacitances (all parasitics)  
 $C_{sb}, C_{gb}, C_{db}$ : depletion capacitances

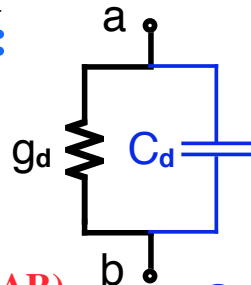
Adding these C's to our model:



# Lecture 14 - Linear Equivalent Circuits - Summary

- **Analog circuit design; small signal models**  
 Linear amplification and processing of signals  
 Digital circuits are ultimately analog
- **Linear equivalent circuits: it all depends on the bias point**

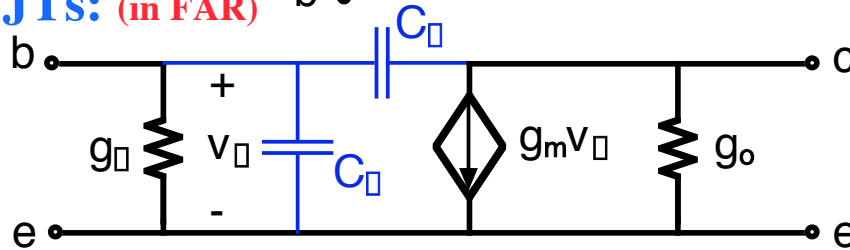
pn diodes:



$$g_d = qI_D/kT$$

$$C_d = g_d\tau_d + C_{dp}(V_{AB})$$

BJTs: (in FAR)



$$g_m = qI_C/kT$$

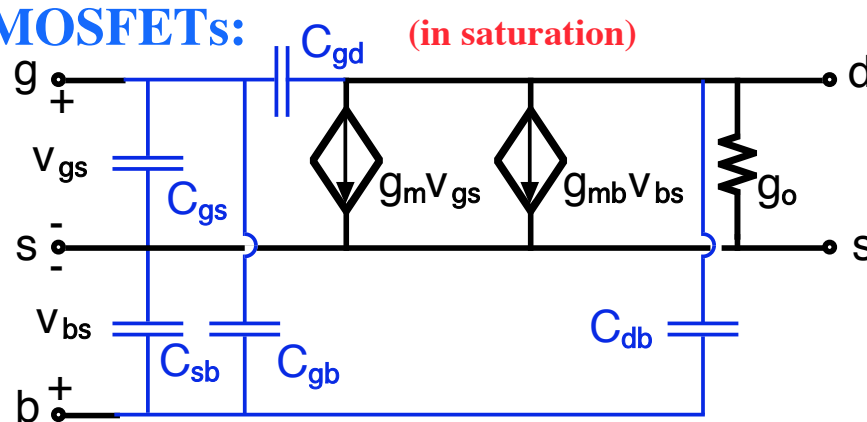
$$g_{\pi} = g_m/\beta_F$$

$$g_o = I_C/V_A \text{ [or } \beta I_C]$$

$$C_{\pi} = g_m\tau_b + C_{dp,be}(V_{BE})$$

$$C_{\mu} = C_{dp,bc}(V_{BC})$$

MOSFETs:



$$g_m = K(V_{GS} - V_T) = (2KI_D)^{1/2}$$

$$g_{mb} = \beta g_m$$

$$\beta = \{qN_A/2(12\epsilon_p - V_{BS})\}^{1/2}/C_{ox}^*$$

$$g_o = I_D/V_A \text{ [or } \beta I_D]$$

$$C_{gs} = (2/3) WL C_{ox}^*$$

$C_{gd}$ : G-D fringing and overlap capacitance, all parasitic

$C_{sb}, C_{gb}, C_{db}$ : depletion capacitances