

YOUR NAME _____

*Department of Electrical Engineering and Computer Science
Massachusetts Institute of Technology*

6.012 Electronic Devices and Circuits

Exam No. 2

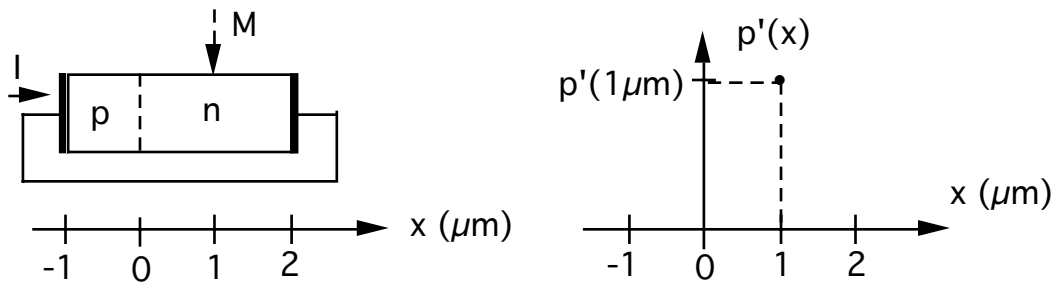
Notes:

1. Unless otherwise indicated, assume room temperature and that kT/q is 0.025 V. You may also approximate $[(kT/q) \ln 10]$ as 0.06 V.
2. Open book; 6.012 text and any other notes permitted.
3. All of your answers and any relevant work must appear on these pages. Any additional paper you hand in will not be graded.
4. Make reasonable approximations and assumptions. State and justify any such assumptions and approximations you do make.
5. Be careful to include the correct units with your answers when appropriate.
6. Be certain that you have all eight (8) pages of this exam booklet and make certain that you write your name at the top of this page in the space provided.

6.012 Staff Use Only	PROBLEM 1 _____ (of 28 possible)
	PROBLEM 2 _____ (of 36 possible)
	PROBLEM 3 _____ (of 36 possible)
	TOTAL

Problem 1 (28points; 4 points each for Parts a, b, c, e, f; 8 points for d)

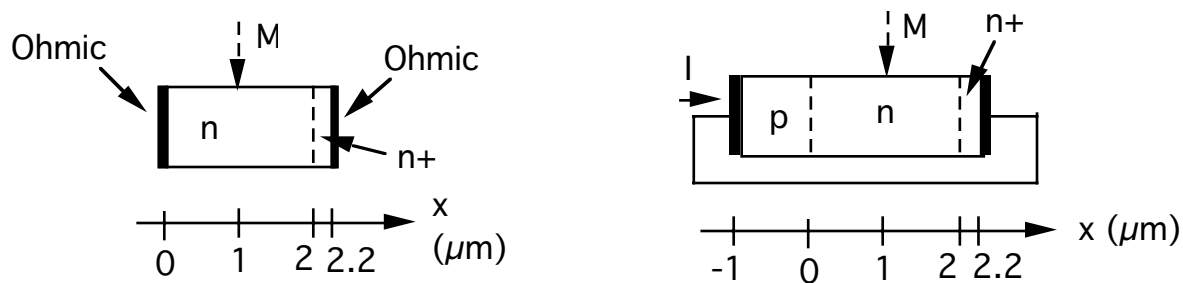
The first several parts of this problem concern the photodiode illustrated to the left below. It is illuminated with light which generates M hole-electron pairs/cm²-s across the plane at $x = 1 \mu\text{m}$, as indicated in the figure. There contacts are ohmic, and the n-type region between $x = 0$ and $2 \mu\text{m}$ is doped to a level of 10^{16} cm^{-3} . The p-region between $x = -1 \mu\text{m}$ and 0 is doped to a level of 10^{16} cm^{-3} . Throughout the device the minority carrier diffusion length is much greater than $2 \mu\text{m}$, μ_e is $1600 \text{ cm}^2/\text{V-s}$, and μ_h is $600 \text{ cm}^2/\text{V-s}$; the cross-sectional area is A . The terminals are shorted, as shown.



- a) Plot the excess minority carrier profile in the diode on the axes provided above on the right.
- b) What is the current, I , measured in the external short circuit?

$I =$ _____

- c) In Exam #1 we looked at adding a $0.2 \mu\text{m}$ thick n^+ region ($N_D = 10^{18} \text{ cm}^{-3}$) before the ohmic contact on one end of an n-type bar, as shown below to the left. Doing this greatly reduces the minority carrier flux to the right-hand ohmic contact.

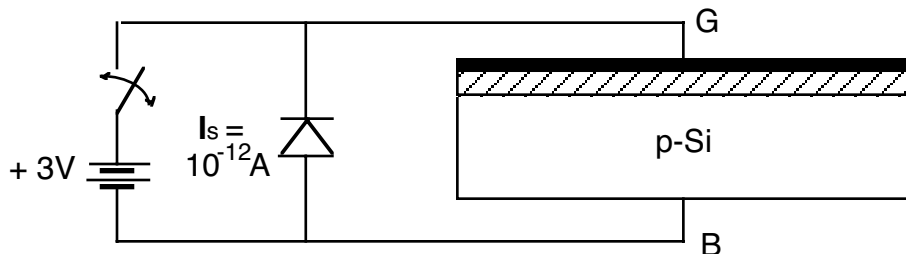


What impact will adding a similiar n^+ layer to our photodiode have on the magnitude of the short circuit current, I ? The "new" diode is shown above to the right. Explain your answer.

- Increase because
- Decrease
- Essentially no impact (i.e., no change),

Problem 1 continued

The last parts of this problem concern the MOS capacitor illustrated below. For this structure the oxide thickness, t_{ox} , is 10 nm ($= 10^{-6}$ cm), the oxide dielectric constant, ϵ_{ox} , is 3.5×10^{-13} coul/V-cm, and the gate area, A , is 10^{-4} cm²; the flatband voltage, V_{FB} , is - 0.3 V, and the threshold voltage, V_T , is + 0.5 V.



d) There are two ranges of values for v_{GB} over which the charge on the gate metal, q_G , varies approximately linearly with v_{GB} , i.e., for which dq_G/dv_{GB} constant. Find these two ranges and for each evaluate the constant and give the condition of the oxide-semiconductor interface (i.e., in accumulation, depletion, and/or inversion).

Range #1: _____ $< v_{GB} <$ _____

Range #2: _____ $< v_{GB} <$ _____

Constant = _____

Constant = _____

Interface condition: _____

Interface condition: _____

e) The switch is closed and the system comes to equilibrium. What is the condition of the oxide-semiconductor interface? If the interface is in either inversion or accumulation, calculate the electron or hole charge, respectively, at the interface in the corresponding inversion or accumulation layer.

Interface condition: _____

Total charge: _____

f) After being closed for a long time, the switch is opened at $t = 0$, and the charge on the MOS capacitor discharges through the diode. Indicate whether this diode is best modeled as a current source (i.e., passing a constant current) or a resistor, and estimate the time it will take for the diode voltage to reach 0.5 V. Ignore any charge stored in the diode.

Resistor

Current source

because

Time to reach 0.5 V: _____

End of Problem 1

Problem 2 (36 points; 3 points for each answer)

An important “diode” connection of a bipolar junction transistor is that in which the base and collector terminals are shorted together as shown on the left below.



- a) Use the Ebers-Moll model to show that the terminal current, i_D , and voltage, v_{AB} , are related as $i_D = I_S[\exp(qv_{AB}/kT) - 1]$, and find an expression for I_S in terms of I_{CS} , I_{ES} , α_F , and α_R , and evaluate it. Assume that the Ebers-Moll parameters for the BJT are $I_{ES} = 2 \times 10^{-13}$ A, $I_{CS} = 4 \times 10^{-13}$ A, $\alpha_F = 0.995$, $\alpha_R = 0.5$.

$$I_S = \frac{\quad}{\text{(expression)}} = \frac{\quad}{\text{(value)}}$$

- b) Now consider putting this “diode” in the circuit shown on the left of the figure on the top of the next page. Calculate V_{REF} , the voltage on the transistor base terminal, when the current I_R through the resistor R_R is 0.2 mA. Then determine the value for the resistor R_R which results in I_R being 0.2 mA. [If you could not find I_S in Part (a), use the value 10^{-14} A, and check here . Do not assume $V_{BE,on} = 0.6$ V, unless you are unable to calculate a more accurate value for it; if this is the case, check here .

$$V_{REF} = \underline{\hspace{2cm}}$$

$$R_R = \underline{\hspace{2cm}}$$

Problem 2 continues on the next page

Problem 2 continued

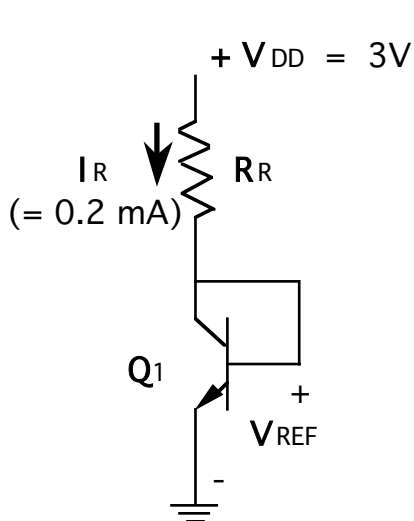


Figure for Part b.

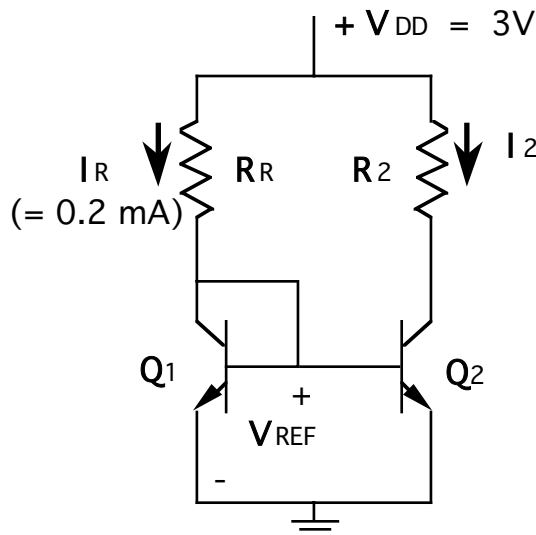


Figure for Part c.

c) Next connect another transmitter, Q_2 , which is identical to the original transistor, and a resistor, R_2 , to the circuit as shown in the right side of the figure above. Ignore the impact connecting Q_2 has on the value of V_{REF} (i.e., assume that the values of V_{REF} and I_R are unchanged inspite of the fact that there is now a small current flowing into the base of Q_2).

i) What is I_2 (assuming Q_2 is in its forward active region)?

$$I_2 = \underline{\hspace{2cm}}$$

ii) Over what range of values can R_2 be varied without changing the value of I_2 ? Assume an npn BJT is in saturarion if v_{CE} is less than 0.2 V. (If you could not answer Part c)i), give your answer in terms of I_2 .)

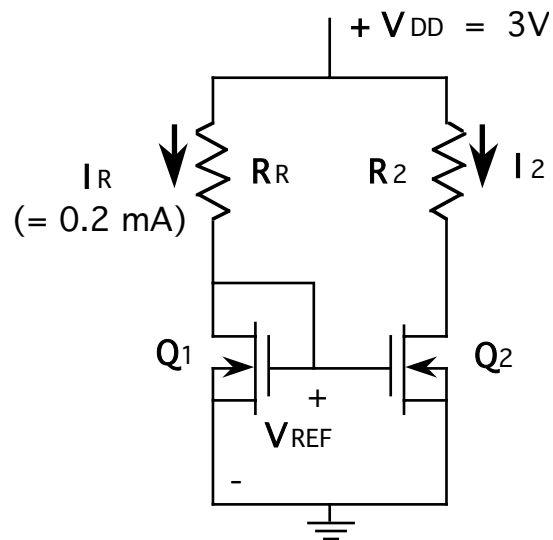
$$\underline{\hspace{2cm}} < R_2 < \underline{\hspace{2cm}}$$

iii) Suppose that Q_2 is identical to Q_1 all ways except that it has twice the cross-sectional area. What is I_2 now? (Assume Q_2 is in its forward active region.

$$I_2 = \underline{\hspace{2cm}}$$

Problem 2 continued

d) Imagine building this same circuit with n-channel, enhancement mode MOSFETs with $K = 0.1 \text{ mA/V}^2$, $V_T = 0.5 \text{ V}$, and $\alpha = 1$. I_R should still be 0.2 mA .



i) What is I_2 now? Assume that Q_2 is in saturation.

$$I_2 = \underline{\hspace{2cm}}$$

ii) What are V_{REF} and R_R ?

$$V_{REF} = \underline{\hspace{2cm}}$$

$$R_R = \underline{\hspace{2cm}}$$

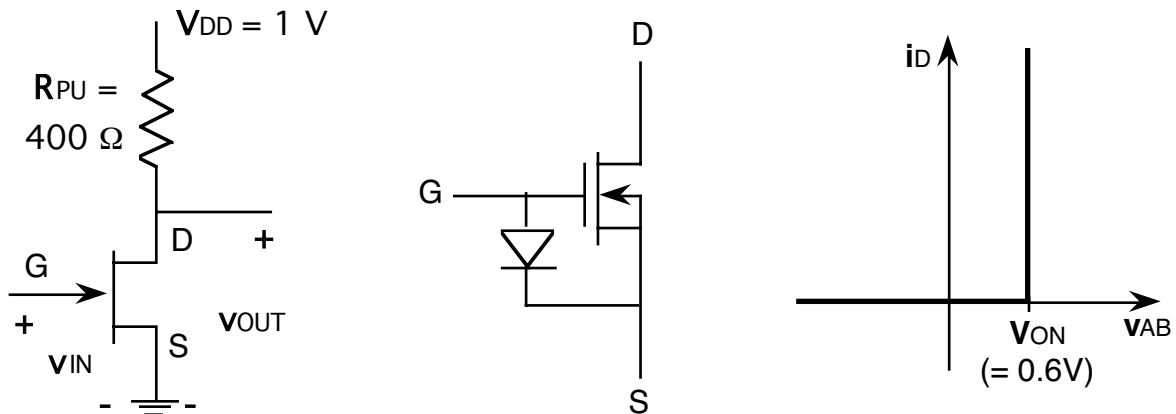
iii) What is I_2 if the K -value of Q_2 is 0.3 mA/V^2 (K for Q_1 is still 0.1 mA/V^2). Continue to assume Q_2 is in saturation.

$$I_2 = \underline{\hspace{2cm}}$$

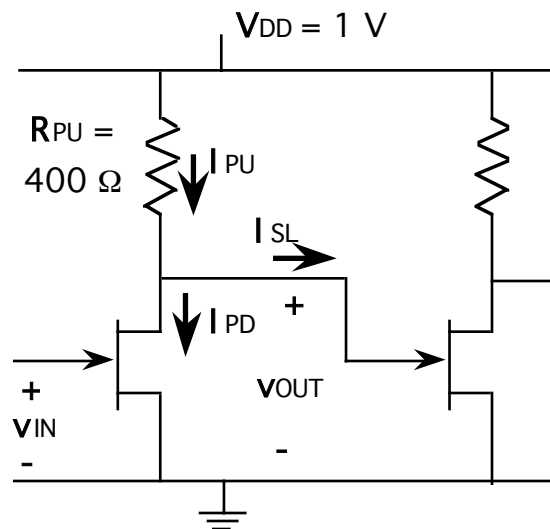
End of Problem 2

Problem 3 (36 points; 12 points each for Parts a, b, and c)

This problem concerns the inverter stage illustrated on the left below. The pull-up device in this stage is a 400 Ohm resistor, and the pull-down device is a junction field effect transistor, an FET which looks like a MOSFET with a p-n diode between its gate and source. This equivalence is shown in the middle figure below. The diode can be modeled as a break-point diode with the characteristic shown below on the right; $V_{ON} = 0.6\text{ V}$. The MOSFET has a threshold voltage, V_T , of 0.4 V .



Analyze this inverter in a string of identical stages as illustrated below.



a) When the input voltage, v_{IN} , is less than V_T , what are the following quantities?

i) The pull-down current, i_{pD} .

$i_{pD} = \underline{\hspace{2cm}}$

ii) The output voltage, v_{OUT} .

$v_{OUT} = \underline{\hspace{2cm}}$

Problem 3 continues on the next page

Problem 3 continued

iii) The pull-up current, i_{PU} .

$$i_{PU} = \underline{\hspace{2cm}}$$

iv) The source load current, i_{SL} .

$$i_{SL} = \underline{\hspace{2cm}}$$

b) When the input voltage, v_{IN} , is 0.6 V, which is above threshold, we want to design the inverter to have v_{OUT} equal to 0.2 V.

i) What is the stage load current, i_{SL} , in this case?

$$i_{SL} = \underline{\hspace{2cm}}$$

ii) What is the pull-down current, i_{PD} , in this case?

$$i_{PD} = \underline{\hspace{2cm}}$$

iii) What must the K-value of the pull-down MOSFET be?

$$K = \underline{\hspace{2cm}}$$

c) Next consider the static power dissipation per inverter stage in this design.

i) What is the static power dissipation when $v_{IN} < V_T$, $v_{OUT} = 0.6$ V?

$$P(v_{IN} < V_T, v_{OUT} = 0.6 \text{ V}) = \underline{\hspace{2cm}}$$

ii) What is the static power dissipation when $v_{IN} = 0.6$ V, $v_{OUT} = 0.1$ V?

$$P(v_{IN} = 0.6 \text{ V}, v_{OUT} = 0.1 \text{ V}) = \underline{\hspace{2cm}}$$

iii) If each inverter is on average in each of the above states half of the time, what is the average power dissipation in an inverter stage?

$$P_{AVE} = \underline{\hspace{2cm}}$$

End of Problem 3; End of Exam