

YOUR NAME \_\_\_\_\_

*Department of Electrical Engineering and Computer Science  
Massachusetts Institute of Technology*

## **6.012 Electronic Devices and Circuits**

### **FINAL EXAMINATION**

**Open book.**

Notes:

1. Unless otherwise indicated, assume room temperature and that  $kT/q$  is 0.025 V.
2. This test is designed so that most parts can be worked independently of the others.
3. All of your answers and any relevant work must appear on these pages. Any additional paper you hand in will not be graded.
4. Make reasonable approximations and assumptions. State and justify any such assumptions and approximations.
5. Be certain that you have all thirteen (13) pages of this exam booklet and make certain that you write your name at the top of this page in the space provided.
6. Your final grade can be obtained after Thursday, December 19. You may see your final exam beginning January 6, 1997.

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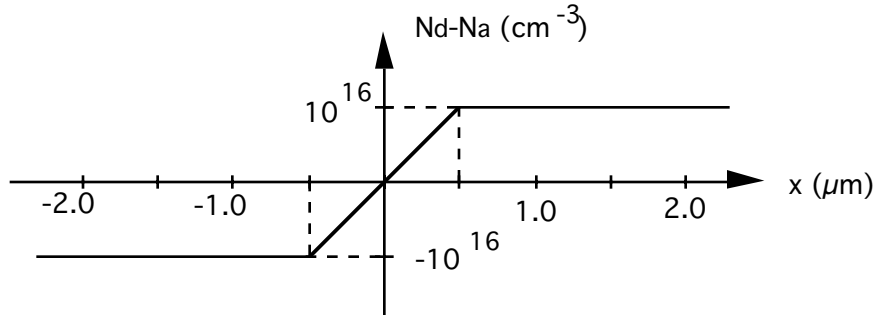
Problem 1	_____
Problem 2	_____
Problem 3	_____
Problem 4	_____
Problem 5	_____

**TOTAL**

**Problem 1** (20 points)

Short questions; answers worth 2 points each.

- (a) Consider a p-n junction with the doping profile illustrated below



- (i) When a bias voltage of -3 V is applied to this junction, the total depletion region width is  $2 \mu\text{m}$ . What is  $x_p$ ?

$$x_p = \text{-----}$$

- (ii) What is the small signal depletion capacitance per unit area of this junction when the bias voltage is -3 V? [ $\epsilon_{\text{Si}} = 10^{-12} \text{ F/cm}^2$ ]

$$C_{\text{pd}} (V_{\text{AB}} = -3\text{V}) = \text{-----}$$

- (b) A sample of germanium ( $n_i = 10^{13} \text{ cm}^{-3}$  at room temperature) with a minority carrier lifetime of  $10^{-6} \text{ s}$  is doped with  $10^{16} \text{ cm}^{-3}$  boron atoms.

- (i) What are the thermal equilibrium electron and hole concentrations,  $n_0$  and  $p_0$ , respectively, in this sample?

$$n_0 = \text{-----}$$

$$p_0 = \text{-----}$$

Problem 1 continues on the next page.

## Problem 1 continued

- (ii) The temperature of the sample is increased to 100°C. Will the electron concentration,  $n_0$ , increase, decrease, or remain essentially unchanged? What about the hole concentration,  $p_0$ ?

$n_0$ :      Increase      Decrease                      No change, because

$p_0$ :      Increase                      Decrease                      No change, because

- (iii) The sample is illuminated with light generating  $10^{18}$  hole-electron pairs/cm<sup>3</sup>-s throughout its bulk. Will the electron concentration,  $n$ , increase, decrease, or remain essentially unchanged? What about the hole concentration,  $p$ ?

$n$ :      Increase                      Decrease                      No change, because

$p$ :      Increase                      Decrease                      No change, because

- (c) A local company has succeeded in making gallium nitride (GaN) p-n diodes with n-type GaN in which the excess hole-electron recombination is very effective in producing blue light. They want your help in designing blue light emitting diodes.

- (i) What type of diodes do you recommend they make, p<sup>+</sup>-n, p-n, or p-n<sup>+</sup>, and why?

p<sup>+</sup>-n ( $N_{Ap} \gg N_{Dn}$ )      p-n ( $N_{Ap} \approx N_{Dn}$ )      p-n<sup>+</sup> ( $N_{Ap} \ll N_{Dn}$ ),  
because

- (ii) How thick do you recommend they make the n-regions (compared to the minority carrier diffusion length,  $L_h$ ), and why?

$w_n$  much greater than  $L_h$        $w_n$  much less than  $L_h$ , because

End of Problem 1

**Problem 2** (20 points)

The questions of this problem require that you to give your answers as written statements (i.e., they are "essay" questions). Keep your answers brief and to the point. Twenty-five (25) words or less should suffice.

- (a) Explain why two discrete p-n diodes with their p-terminals connected together cannot function as an npn bipolar junction transistor, that is, cannot provide current gain.
- (b) (i) Explain physically how a bipolar junction transistor, BJT, can have current gain, that is,  $\beta_F = I_C/I_B > 1$ .
- (ii) Write an expression for the current gain,  $\beta_F$ , of a BJT in terms of the doping concentrations, mobilities, and widths of the different regions of the transistor (use a short-base model).
- (c) (i) What is the physical origin of the Early voltage in a BJT?
- (ii) Why is the collector usually more lightly doped than the emitter in a BJT?
- (iii) Can the collector and emitter be exchanged for current amplification and why or why not?

**Problem 2 continues on the next page.**

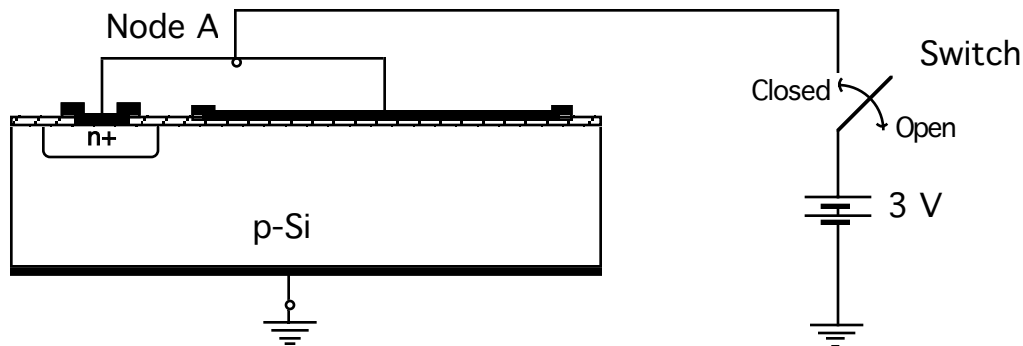
**Problem 2 continued**

- (e) What is the meaning of the  $f_T$  of a BJT, and how does it depend on the base width,  $w_B$ ?
- (f) Why is an npn BJT preferred over a pnp BJT for high current gain and high speed?
- (g) (i) Give an expression for the Miller Capacitance of a common-emitter BJT voltage amplifier with a resistance  $R_C$  in the collector circuit.
- (ii) Suggest an alternative to the common-emitter amplifier that will have a comparable voltage gain and significantly less Miller Effect. You can use more than one transistor.

**End of Problem 2**

**Problem 3** (20 points)

Consider the MOS capacitor/p-n diode circuit illustrated below. The MOS capacitor has an oxide capacitance,  $C_{OX}$  ( $\equiv A_o/t_o$ ), of  $0.2 \text{ pF}^*$ ; a flat-band voltage,  $V_{FB}$ , of  $-0.5 \text{ V}$ ; and a threshold voltage,  $V_T$ , of  $1.0 \text{ V}$ . For the p-n diode, the reverse saturation current,  $I_S$ , is  $10^{-9} \text{ A}$ . The battery is an ideal  $3 \text{ V}$  voltage source, and the switch is either open or closed as specified in the questions.



- (a) The switch has been open for a long time and the diode and MOS capacitor are at thermal equilibrium. What is the condition of the oxide-semiconductor interface?

Accumulated      Depleted      Inverted, because:

- (b) After being open for a long time as in Part (a), the switch is closed. After all transients have died out, what values will the following quantities have?

- (i) The current from the battery,  $I_B$ .

$$I_B = \text{_____}$$

- (ii) The total inversion layer charge in the MOS capacitor,  $Q_N$ .

$$Q_N = \text{_____}$$

**Problem 3 continues on the next page**

\* Recall that a pF is  $10^{-12} \text{ F}$ , and F is coul/V.

### Problem 3 continued

(c) After being closed for a long time as in Part (b), the switch is again opened at a time we will take to be  $t = 0$ .

(i) What is the initial rate of change in the voltage on Node A (relative to ground), i.e., at  $t = 0^+$ ?

$$dV_A/dt @ t = 0^+ = \underline{\hspace{4cm}}$$

(ii) What is the rate of change in the voltage on Node A (relative to ground) when  $V_A$  is 1.5 V?

$$dV_A/dt @ V_A = 1.5 \text{ V} = \underline{\hspace{4cm}}$$

(iii) At what time will the voltage on Node A equal  $V_T$ , i.e. 1 V?

$$t \text{ (at which } V_A = 1 \text{ V)} = \underline{\hspace{4cm}}$$

(iv) Does the magnitude of the rate of change in  $V_A$  with time increase, decrease, or stay the same as  $V_A$  passes from  $V_A > V_T$  to  $V_A < V_T$ , and why?

Increase

Decrease

No change, because

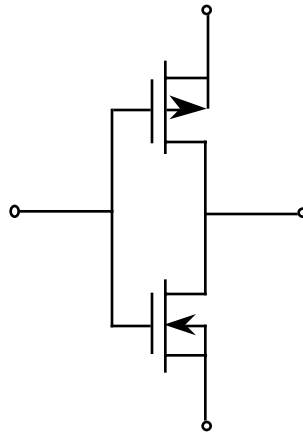
**End of Problem 3**

**Problem 4** (20 points)

You are caught in the digital (6.111) lab late at night and need a linear amplifier to debug your circuit. All you have available are 5 V power supplies and CMOS inverters, but using 6.012 knowledge you try to construct a useful amplifier. The spec. sheets give you the following data on the inverters, and shows you their schematic:

$$K_n = K_p = 1 \times 10^{-4} \text{ A/V}^2; V_{Tn} = 1 \text{ V}, V_{Tp} = -1 \text{ V}; |V_{An}| = |V_{Ap}| = 10 \text{ V}$$

Schematic:

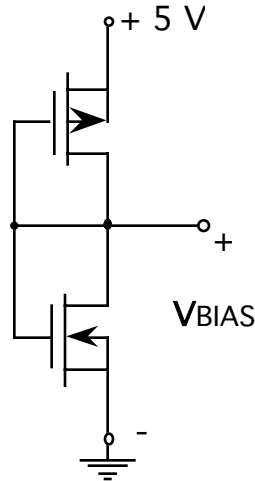


- (a) (i) In the space provided below, sketch the voltage transfer characteristic for the CMOS inverter. Clearly label the different areas of operation for the transistors across the characteristic.

- (ii) Where do you want to operate the inverter for high voltage gain?

Problem 4 continued

(b) In order to bias the input of your CMOS-inverter amplifier, your T.A. suggests the circuit shown below:

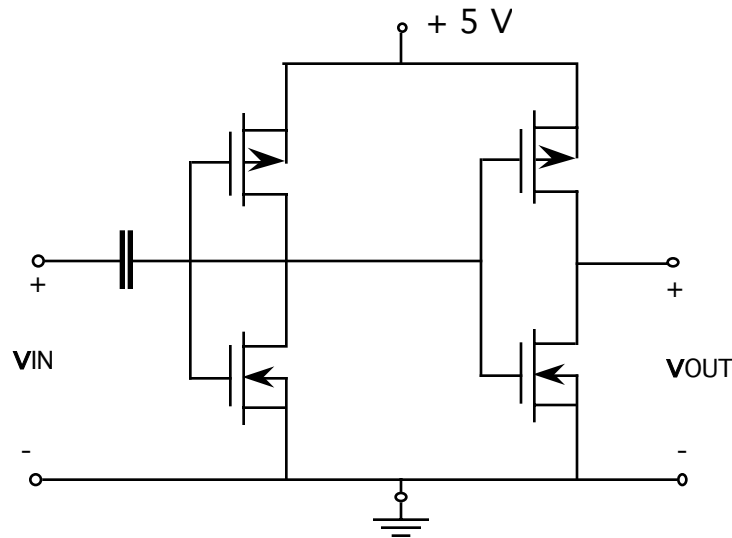


(i) Either graphically or analytically, determine  $V_{BIAS}$ .

$$V_{BIAS} = \text{-----}$$

(ii) Comment on the suitability of this bias circuit for biasing one of your CMOS inverters for use as a linear amplifier.

(c) Assume that the bias circuit your T.A. suggested biases the inverter properly so your final amplifier topology is as shown below:



Problem 4 continues on the next page

### Problem 4 continued

(i) In the space provided below draw a small-signal linear equivalent circuit for this amplifier valid for incremental operation about this bias point. (If you could not answer the earlier parts of this question assume that the bias point is such that all of the MOSFETs are biased in saturation.) Be certain to give values for all of the elements in your model.

(ii) Calculate the small signal input resistance,  $R_{in}$ , of this amplifier.

$$R_{in} = \text{-----}$$

(iii) Calculate the small signal open-circuit voltage gain,  $A_{v,oc}$ , of this amplifier.

$$A_{v,oc} = \text{-----}$$

(iv) Calculate the small signal output resistance,  $R_{out}$ , of this amplifier.

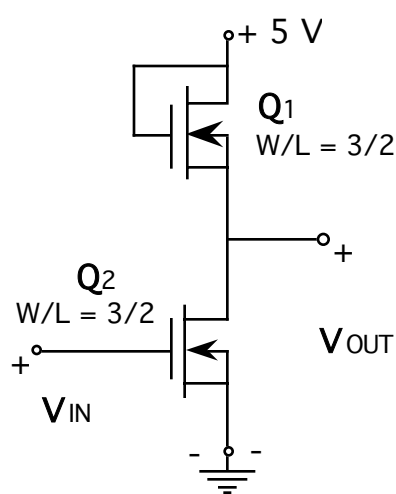
$$R_{out} = \text{-----}$$

(v) Comment on whether or not this is a "good" voltage amplifier. (Be sure to explain your answer.)

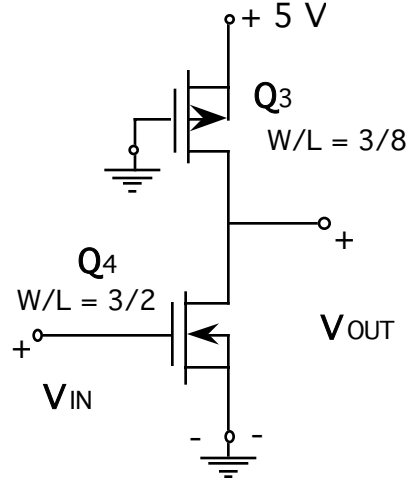
End of Problem 4

**Problem 5 (20 points)**

In this problem you are to consider the two circuits below. They contain n-channel MOSFETs, with  $V_{Th} = 0.75 \text{ V}$  and  $\mu_{e n} / t_o = 46 \mu\text{A}/\text{V}^2$ , and p-channel MOSFETs, with  $V_{Tp} = -0.75 \text{ V}$  and  $\mu_{h p} / t_o = 14 \mu\text{A}/\text{V}^2$ . The width-to-length ratio,  $W/L$ , for each device is indicated in the figure.



Circuit I



Circuit II

(a) With  $v_{IN} = 0 \text{ V}$ , in which region of operation is each transistor biased?

(i)  $Q_1$ :      Saturation      Linear      Cut-off

(ii)  $Q_2$ :      Saturation      Linear      Cut-off

(iii)  $Q_3$ :      Saturation      Linear      Cut-off

(iv)  $Q_4$ :      Saturation      Linear      Cut-off

Problem 5 continues on the next page.

**Problem 5 continued**

(b) What is the output voltage,  $v_{OUT}$ , in each circuit with  $v_{IN} = 0V$ , and what is the static power dissipation,  $P_{STATIC}$ , with this input?

(i) Circuit I:  $v_{OUT} =$  \_\_\_\_\_  
 $P_{STATIC} =$  \_\_\_\_\_

(ii) Circuit II:  $v_{OUT} =$  \_\_\_\_\_  
 $P_{STATIC} =$  \_\_\_\_\_

(c) With  $v_{IN} = 5 V$ , in which region of operation is each transistor biased?

(i)  $Q_1$ :      Saturation              Linear              Cut-off

(ii)  $Q_2$ :      Saturation              Linear              Cut-off

(iii)  $Q_3$ :      Saturation              Linear              Cut-off

(iv)  $Q_4$ :      Saturation              Linear              Cut-off

**Problem 5 continues on the next page.**

**Problem 5 continued**

(d) What is the output voltage,  $v_{OUT}$ , in each circuit with  $v_{IN} = 5V$ , and what is the static power dissipation,  $P_{STATIC}$ , with this input?

(i) Circuit I:  $v_{OUT} =$  \_\_\_\_\_  
 $P_{STATIC} =$  \_\_\_\_\_

(ii) Circuit II:  $v_{OUT} =$  \_\_\_\_\_  
 $P_{STATIC} =$  \_\_\_\_\_

(e) For each circuit, state whether it will perform reasonably as an inverter or not, and explain why.

(i) Circuit I:            Yes            No,            because

(ii) Circuit II:            Yes            No,            because

**End of Problem 5**

**End of the exam**