

YOUR NAME _____

*Department of Electrical Engineering and Computer Science
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6.012 Electronic Devices and Circuits

FINAL EXAMINATION

Open book.

Notes:

1. Unless otherwise indicated, assume room temperature and that kT/q is 0.025 V, $kT/q \ln 10 = 60$ mV, and $n_i = 10^{10}$ cm⁻³ for Si.
2. This test is designed so that most parts can be worked independently of the others.
3. All of your answers and any relevant work must appear on these pages. Any additional paper you hand in will not be graded.
4. Make reasonable approximations and assumptions. State and justify any such assumptions and approximations.
5. Be certain that you have all fifteen (15) pages of this exam booklet and make certain that you write your name at the top of this page in the space provided.
6. You may see your final exam beginning January 5, 1998.

For staff use only

Problem 1	_____
Problem 2	_____
Problem 3	_____
Problem 4	_____
Problem 5	_____

TOTAL

Problem 1 (20 points) Warm-up time

(a) Answer the following short questions in 15 words or less:

(i) What computational advantage do we gain when we can assume low level injections conditions?

(ii) Assuming devices with identical dimensions, would an n-channel MOSFET or a p-channel MOSFET have a higher transconductance at a given drain current bias level, $|I_D|$, and why?

n-channel p-channel, because

(iii) In a photodiode, what is the sign of the optically generated current (following the normal convention of positive flow being from the p-side to the n-side of the junction), and why?

positive negative, because

(iv) Describe a unique feature of the channel of a MOSFET in each of its three main operating regions?

Cut-off:

Linear:

Saturation:

(v) What feature of CMOS digital integrated circuits is most likely to lead a manufacturer of simple hand-held calculators to consider using it over other MOS or bipolar logic families?

Problem 1 continues on the next page.

Problem 1 continued

(b) Consider two geometrically identical bipolar transistors, one npn, the other pnp, in which the magnitudes of the doping levels in the emitter, base, and collector regions are identical. Assume infinite minority carrier lifetimes and $D_e = 3 D_h$. How would the following parameters compare in these two devices? Explain your answers.

(i) Forward common-emitter current gain, β :

greater in npn greater in pnp similar in both, because

(ii) Small signal base-collector capacitance, C_{cb} , at same bias point, V_{CB} :

greater in npn greater in pnp similar in both, because

(iii) Common-emitter short circuit current gain unity-gain frequency, f_T :

greater in npn greater in pnp similar in both, because

(iv) Small signal transconductance, g_m , at the same bias level, I_C :

greater in npn greater in pnp similar in both, because

(v) (1) Excess charge stored in the base at the same base-emitter voltage bias level, V_{BE} . Assume that this bias is in the forward active region):

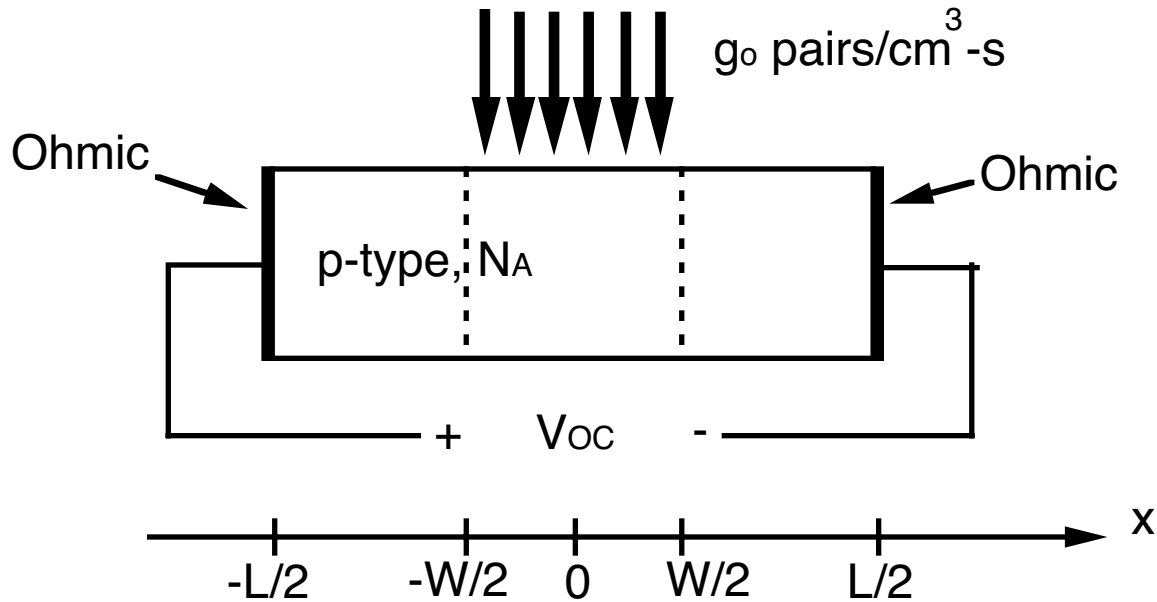
greater in npn greater in pnp similar in both, because

(2) Excess charge stored in the base at the same collector current bias level, I_C . Assume that this bias is in the forward active region):

greater in npn greater in pnp similar in both, because

End of Problem 1

Problem 2 (20 points)



An open circuited p-type silicon sample of length L with acceptor concentration, N_A , of $2 \times 10^{17} \text{ cm}^{-3}$ is uniformly and symmetrically illuminated with light over a distance w in the central region as shown in the figure above. The optical generation function, $g_L(x)$, is g_0 hole-electron pairs/cm³-s for $-\frac{W}{2} < x < \frac{W}{2}$, and zero (0) for all other x . The sample has ohmic contacts on each end.

Assume low level injection and that the minority carrier current is predominately due to diffusion. The electron mobility, μ_e , is $1600 \text{ cm}^2/\text{V}\cdot\text{s}$ and lifetime, τ_e , is 10^{-6} s , while the hole mobility, μ_h , is $600 \text{ cm}^2/\text{V}\cdot\text{s}$. The electron diffusion length is much greater than the sample length L (i.e., $L_e = \sqrt{D_e \tau_e} \gg L$). The sample is at room temperature.

(a) In the absence of light, what are the approximate equilibrium hole and electron concentrations, p_0 and n_0 , respectively, in this sample?

$$n_0 = \text{_____ cm}^{-3}$$

$$p_0 = \text{_____ cm}^{-3}$$

Problem 2 continues on the next page.

Problem 2 continued

(b) What are the hole and electron diffusion coefficients, D_e and D_h , in this sample?

$$D_e = \text{_____ cm}^2/\text{s}$$

$$D_h = \text{_____ cm}^2/\text{s}$$

(c) Find the steady state spatial distribution of excess electrons, $n'(x)$, in the sample after the light illumination has been on for a long time. Plot and label your result in the space provided below. Recall that $L_e \gg L$.

(d) Find the hole and electron current densities, $J_h(x)$ and $J_e(x)$, in the sample. Plot and label your result in the space provided below.

Problem 2 continues on the next page.

Problem 2 continued

(e) Find the electric field distribution, $E(x)$, in the sample. Plot and label your result in the space provided below.

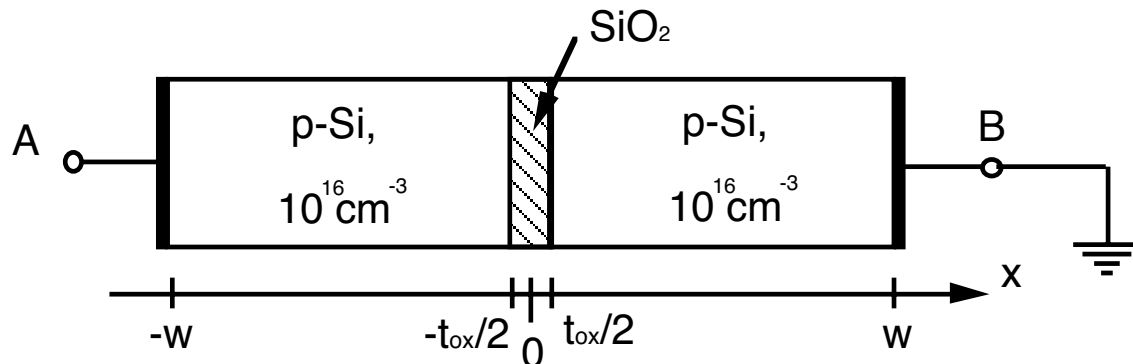
(f) What is the open circuit voltage, V_{OC} , across this sample assuming there are no potential drops across the ohmic contacts?

$$V_{OC} = \text{_____} \text{ V}$$

End of Problem 2

Problem 3 (20 points)

This problem concerns the novel semiconductor-oxide-semiconductor (SOS) structure illustrated below. The two semiconductor regions are both p-type silicon with a net acceptor concentration of 10^{16} cm^{-3} ; the oxide is a 50 nm ($5 \times 10^{-6} \text{ cm}$) thick layer of silicon dioxide. The dielectric constant of silicon, ϵ_{Si} , is 10^{-12} f/cm and of silicon dioxide, ϵ_{SiO_2} , is $3.5 \times 10^{-13} \text{ f/cm}$.



Use the depletion approximation model when solving this problem.

(a) In the space provided below, sketch and label the electrostatic potential, $\phi(x)$, in this structure between $-w/2$ and $+w/2$ when $V_{\text{AB}} = 0$ and the structure is in thermal equilibrium.

(b) A bias is applied to this device sufficient to make the electrostatic potential at $x = t_{\text{ox}}/2$ equal to $-\phi_p$, where ϕ_p is the thermal equilibrium electrostatic potential in the p-type regions, i.e., $(t_{\text{ox}}/2) = -\phi_p$. We call this the onset of inversion on the right side, and name this bias the right-side threshold, V_{TR} .

(i) What is the sign of V_{TR} ? Explain your answer.

positive negative neither (i.e., $V_{\text{TR}} = 0$), because

Problem 3 continues on the next page

Problem 3 continued

- (ii) What is the width of the depletion region to the right of $x = t_{ox}/2$ with this applied bias?

Depletion region width: _____ cm

- (iii) What is the condition of the left-hand semiconductor-oxide interface, the one at $x = -t_{ox}/2$ with this applied bias?

accumulated depleted inverted, because

- (iv) What is the value of V_{TR} ?

$V_{TR} =$ _____ Volts

(c) In the space provided below, sketch and label the net charge density, $\rho(x)$, for $-w/2 < x < w/2$ when the bias voltage, V_{AB} , is $V_{TR} + 2$ Volts; recall V_{TR} was defined in Part (b). Be sure to label the vertical axis and to indicate the magnitude of any impulses (i.e., sheet charge densities).

(d) Define the left-hand threshold, V_{TL} , of the structure as the bias voltage, V_{AB} , at which the potential at $x = -t_{ox}/2$ is $-p$. What is V_{TL} ? (You can give your answer in terms of V_{TR} , if you wish. Making use of symmetry should simplify your calculation.)

$V_{TL} =$ _____ Volts

Problem 3 continues on the next page

Problem 3 continued

(e) NOTE: This part is worth only 4 points so do not spend too much time on it. Consider now a different SOS structure in which the left-hand semiconductor region is doped n-type, rather than p-type, with a net donor concentration of 10^{16} cm^{-3} .

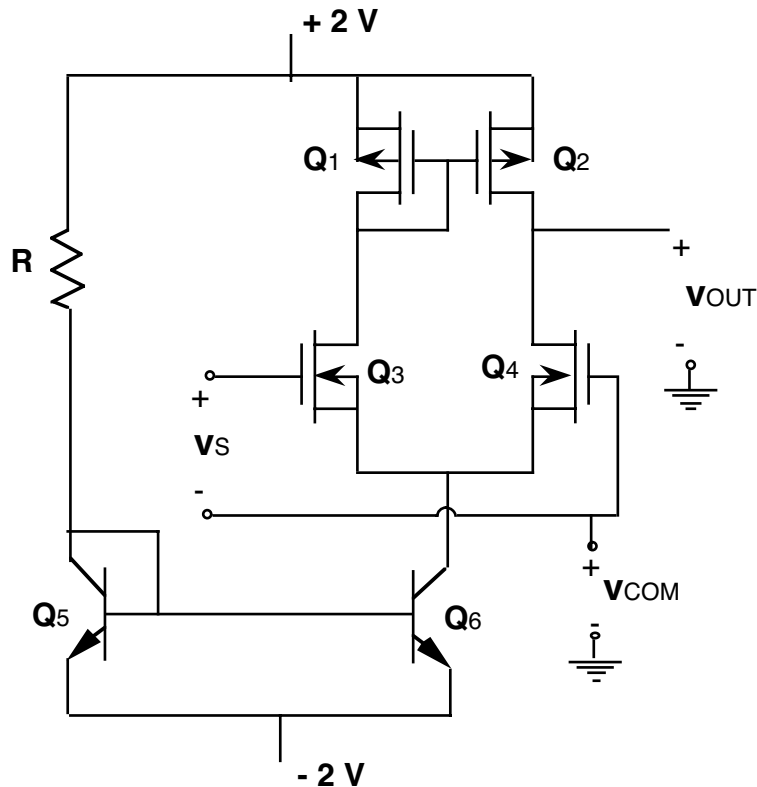
(i) In the space provided below, sketch the electrostatic potential, $\phi(x)$ for $-w/2 < x < w/2$ in thermal equilibrium, i.e., $V_{AB} = 0$. Label the vertical axes but you do not calculate the widths of any depletion regions.

(ii) In the space provided below, sketch and label the electrostatic potential when V_{AB} is V_{TR} for this new structure, where V_{TR} has the same definition as before [see Part (b) above], but will not necessarily have the same value.

(iii) What is the value of V_{TL} for this new structure in terms of V_{TR} for this new structure, where V_{TR} and V_{TL} have the same definitions as earlier? (Making use of the antisymmetry of the problem will simplify your solution.)

$$V_{TL} = \underline{\hspace{2cm}}$$

End of Problem 3

Problem 4 (20 points)


In the differential amplifier shown above Q_1 and Q_2 are identical p-channel MOSFETs with $K = 1.0 \text{ mA/V}^2$, $V_T = -0.5 \text{ V}$, and $|V_{A1}| = 10 \text{ V}$; Q_3 and Q_4 are identical n-channel MOSFETs with $K = 2.0 \text{ mA/V}^2$, $V_T = 0.5 \text{ V}$, and $|V_{A1}| = 20 \text{ V}$; and Q_5 and Q_6 are identical npn BJTs with $\beta_F = 150$, $|V_{A1}| = 50 \text{ V}$, and $V_{BE,ON} = 0.6 \text{ V}$. The BJTs are in saturation when V_{CE} is less than 0.2 V (i.e., when the base-collector junction is forward biased 0.4 V , or more). The MOSFETs must be operated with $|V_{GS} - V_T| > 0.2 \text{ V}$, and the BJTs with $I_C > 10 \mu\text{A}$.

- (a) Select R so the quiescent drain currents in Q_3 and Q_4 are 0.5 mA .

$$R = \text{_____} \text{ Ohms}$$

- (b) What is the quiescent value of the gate-to-source voltage, V_{GS} , on the MOSFET, Q_3 ? Recall that the quiescent drain current in Q_3 is 0.5 mA .

$$V_{GS} = \text{_____} \text{ V}$$

Problem 4 continues on the next page

Problem 4 continued

(c) The voltage v_{COM} is applied to both inputs; the voltage v_s has no DC level and is only a small signal voltage. With $v_s = 0$, over what range of values for v_{COM} will all the transistors in this circuit stay biased in their forward active regions?

$$\text{_____ V} < v_{COM} < \text{_____ V}$$

(d) With $v_s = 0$, and v_{COM} within the range you found in Part (c), what is value of the output voltage, v_{OUT} ?

$$v_{OUT} = \text{_____ V}$$

(e) What is the quiescent (DC) power dissipation in this circuit?

$$P = \text{_____ Watts}$$

(f) This part of the problem concerns the small signal behavior of this amplifier.

(i) In terms of v_{COM} and v_s , what are the differential- and common-mode input voltages, v_{ID} and v_{IC} , respectively?

$$v_{ID} = \text{_____}$$

$$v_{IC} = \text{_____}$$

Problem 4 continues on the next page.

Problem 4 continued

(ii) What is the small-signal, mid-band voltage gain of this circuit for the input v_s , i.e., what is $A_v \equiv v_{out}/v_s$?

$$A_v \equiv v_{out}/v_s = \underline{\hspace{4cm}}$$

(iii) Is it possible to increase the voltage gain, A_v , by changing the bias level, I_{C6} ? If yes, indicate whether I_{C6} should be increased or decreased, and why. If no, explain why not.

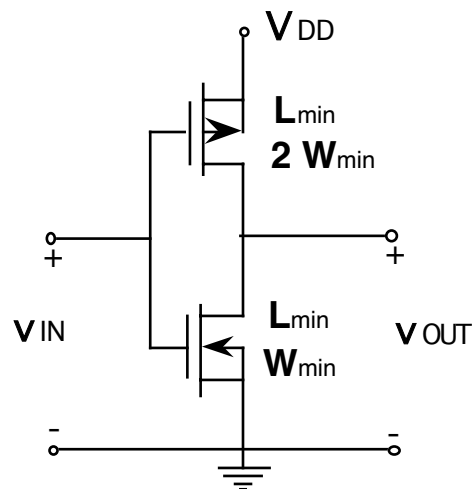
Yes, by increasing decreasing I_{BIAS} because

No, because

End of Problem 4

Problem 5 (20 points)

This problem deals with CMOS inverters fabricated using a process for which the minimum gate length and width are L_{\min} and W_{\min} , respectively. In order to obtain symmetrical transfer characteristics and minimize the gate delay, the inverters are designed to have $V_{Tn} = |V_{Tp}|$, $t_{oxn} = t_{oxp}$, and $K_n = K_p$. All the inverters have minimum length gates, i.e., $L_n = L_p = L_{\min}$, and the width of the p-channel devices is twice that of the n-channel devices, i.e., $W_p = 2W_n$, because the hole and electron mobilities in the channel differ by a factor of two, i.e., $\mu_e = 2\mu_p$. The smallest inverters have $W_n = W_{\min}$ and $W_p = 2W_{\min}$, and we will call the corresponding K value K_{\min} . This minimum-size inverter is below:



The gate delay, t_{GD} , of a minimum-size inverter with a fan-out of one is 100 ps (10^{-10} s). We will call this the minimum gate delay, $t_{GD, \min}$.

(a) What is the gate delay of a minimum-size inverter which has a fan-out of four, i.e., when its output is connected to four stages?

$$t_{GD}(\text{Minimum-size inverter with fan-out} = 4) = \text{_____ s}$$

(b) Suppose that some of the minimum-size inverters on an integrated circuit chip were mistakenly designed with $W_n = W_p$. Determine what impact this has on the gate delay, t_{GD} , of these inverters, and calculate their gate delay.

$$t_{GD}(W_n = W_p = W_{\min}, L_n = L_p = L_{\min}) = \text{_____ s}$$

Problem 5 continues on the next page.

Problem 5 continued

(c) The inverters which drive the bond pads and the wires going to other chips must supply much larger currents because they have much larger capacitances to charge and discharge than do the inverters which simply drive other inverters on the same chip. We will call these "output inverters." Suppose that on the present chip, the MOSFETs in the output inverters must have K values of $100 K_{\min}$.

(i) What are W_n and W_p of the devices in the output inverters?

$$W_n = \underline{\hspace{2cm}}$$

$$W_p = \underline{\hspace{2cm}}$$

(ii) What is the input capacitance of these output stages in terms of the input capacitance of a minimum-size inverter, which you can call C_{\min} ?

$$C_{in} (100 K_{\min} \text{ output stage}) = \underline{\hspace{2cm}}$$

(iii) What would the gate delay be for a minimum-size inverter loaded with a single output inverter stage, i.e., loaded with the capacitance you found above in Part (c)(ii)?

$$t_{GD} (K_{\min} \text{ stage loaded by } 100 K_{\min} \text{ output stage}) = \underline{\hspace{2cm}} \text{ s}$$

(d) Consider inserting an inverter stage with $K = 10 K_{\min}$ between the minimum-size inverter and an output inverter.

(i) In the space provided below draw the circuit schematic for these three inverter stages, indicating next to each device its gate width.

Problem 5 continued

- (ii) What are the gate delays, t_{GD} 's, for the first (K_{min}) and second ($10 K_{min}$) stages in this circuit?

$$t_{GD} (K_{min} \text{ stage loaded by } 10 K_{min} \text{ stage}) = \text{_____ s}$$

$$t_{GD} (10 K_{min} \text{ stage loaded by } 100 K_{min} \text{ stage}) = \text{_____ s}$$

- (iii) What is the total delay going through both the K_{min} and $10 K_{min}$ stages, and how does it compare with your answer in Part (c)(iii)?

$$t_{GD} (\text{Through } K_{min} \text{ and } 10 K_{min} \text{ stages}) = \text{_____ s}$$

- (iv) OPTIONAL (A treat for those with time to kill.) If one intermediate stage before an output stage is good, are two better? How about n ? Discuss:

End of Problem 5

End of the exam

HAPPY HOLIDAYS