

MASSACHUSETTS INSTITUTE OF TECHNOLOGY

Department of Electrical Engineering and Computer Science

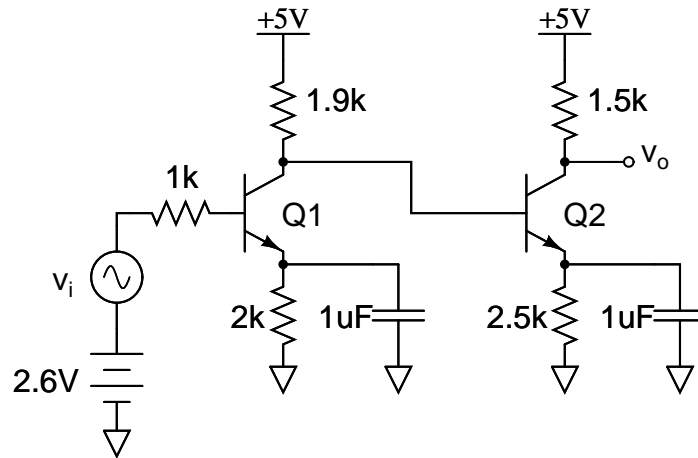
6.301 Solid State Circuits

Spring Term 2003
 Problem Set 3

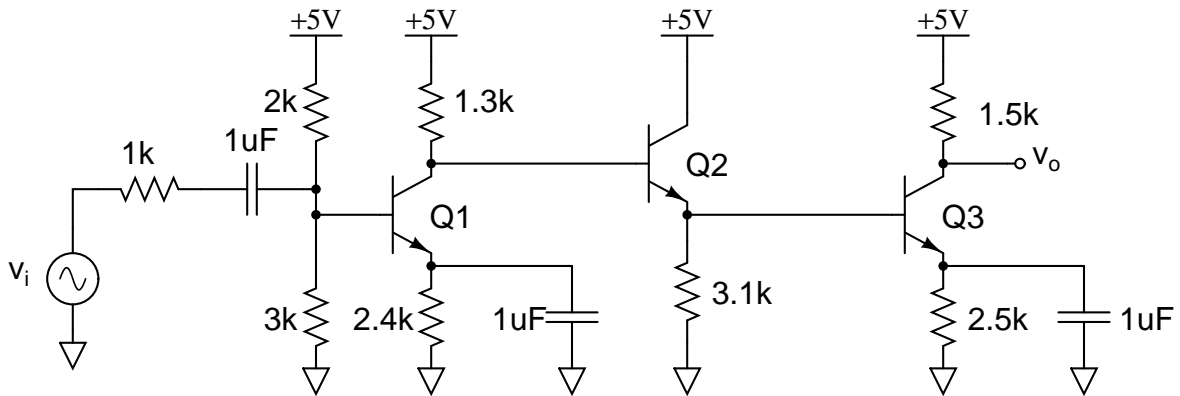
Issued : February 14, 2003
 Due : Friday, February 21, 2003

Problem 1: Find the mid-band gain for each circuit below. Assume that $\beta = 200$, $V_{BE,ON} = 0.6V$, and ignore r_o .

(a) Circuit a

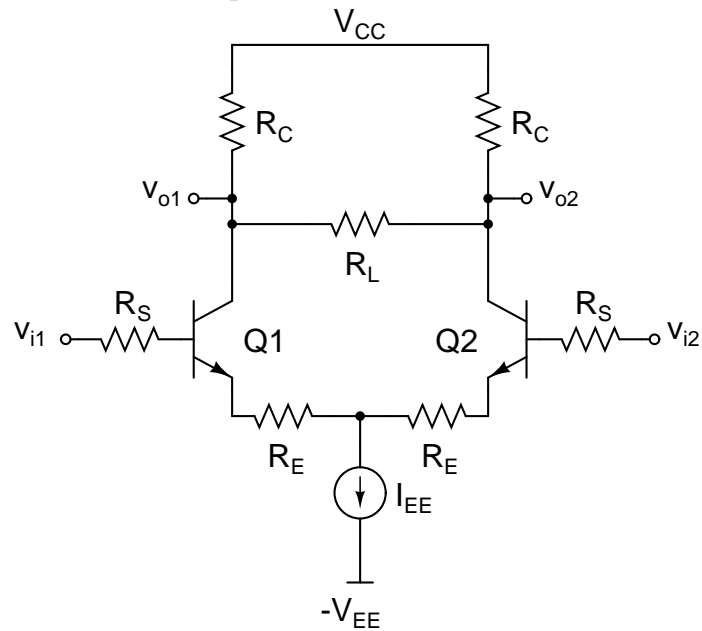


(b) Circuit b



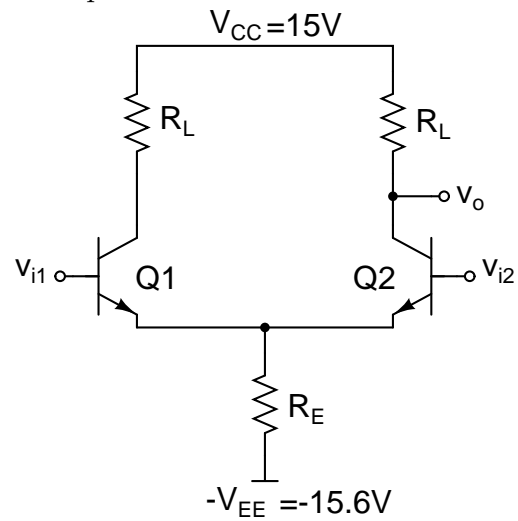
Problem 2: Simulate the CE-EF-CE amplifier in Circuit 1b (above) with HSPICE. Use the following data for your simulations: $I_S = 10^{-15}A$, $\beta_F = 200$, $V_A=100$, $\tau_F = 0.1ns$, $c_{jeo} = 10pF$, and $c_{jco} = 2pF$. Turn in your HSPICE input file, and an Awaves plot showing the low and high frequency roll-offs.

Problem 3: For the differential amplifier shown below:



- (a) Find the differential voltage gain a_{vd} and the common mode voltage gain a_{vc} .
- (b) Find both the differential and common mode input and output resistances ($R_{in,d}$, $R_{in,c}$, $R_{out,d}$, and $R_{out,c}$).

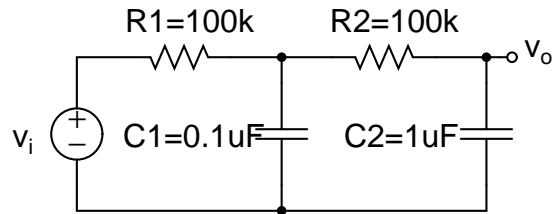
Problem 4: For the single-ended differential amplifier shown below, assume that $\beta = 200$ and $V_{BE,ON} = 0.6V$ for both transistors, and that the DC common mode input voltage is zero. Neglect r_o for this problem.



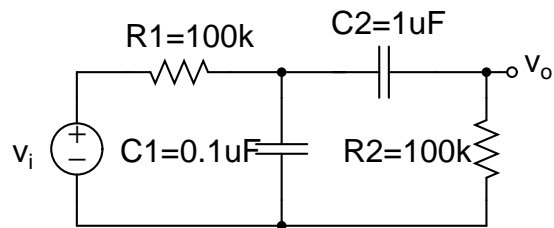
- Express the differential voltage gain a_{vd} as a function of the voltage drop V_L across R_L .
- If $V_{CE,SAT} = 0.3V$, what is the maximum a_{vd} possible?
- Select R_L and R_E so that $R_{in,d} = 1M\Omega$ and $a_{vd} = 300$. What is the common mode rejection ratio (CMRR)?

Problem 5: For each circuit below, find the transfer function v_o/v_i , and draw the Bode plot (magnitude and phase). Sketching the step response is optional but good practice. For the transistor in part (d), assume that $\beta = 200$, $V_{BE,ON} = 0.6V$, and $c_\pi = 20pF$. You may ignore c_μ for this problem.

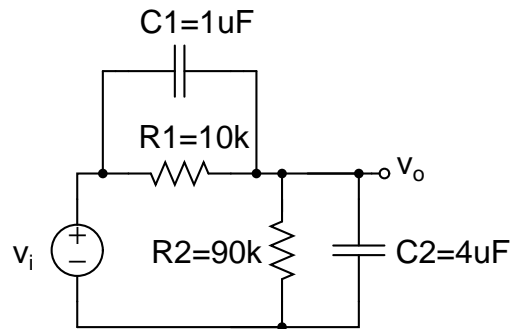
(a) Circuit a



(b) Circuit b



(c) Circuit c



(d) Circuit d

