



# Outline

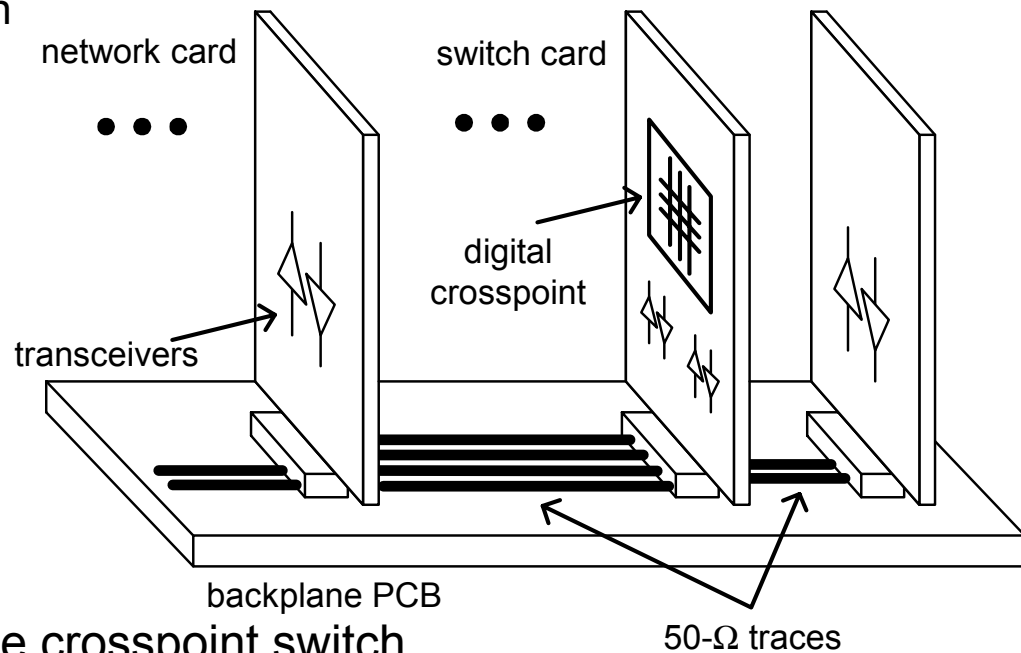
---

- Motivation
- Brief Overview of High-Speed Links
- Design Considerations for Low Power
- DVS Link Design Example
- Summary

# Motivation

---

- Demand for high bandwidth communications
- Advancements in IC fabrication technology
  - Higher performance
  - More complex functionality
  - Chip I/O becomes performance bottleneck
  - Increasing power consumption
- Network router example



- 10's to 100's of links on a single crosspoint switch

# High-Speed Links Overview

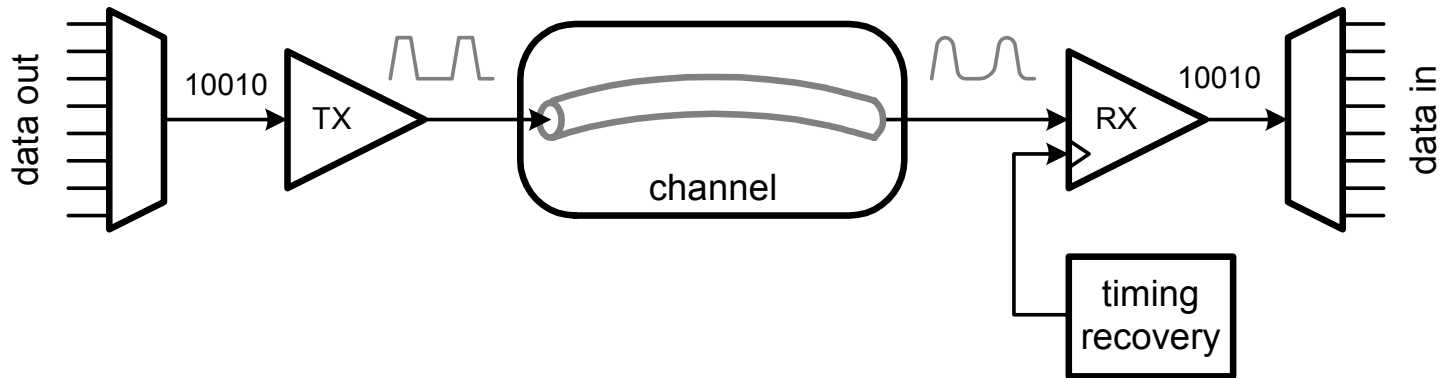
---

- High-speed data communication between chips across an impedance controlled channel
  - Shared communication bus (memories)
  - Point-to-point links
- Types of link architectures and implementations
  - Parallel vs. serial
  - Differential vs. single-ended
  - Low-impedance vs. high-impedance driver
  - Transmitter-only vs. receiver-only vs. double termination
- We will focus on point-to-point serial links using differential high-impedance drivers with double termination for network routers
  - Techniques to reduce power applicable to other link types

# Link Components

---

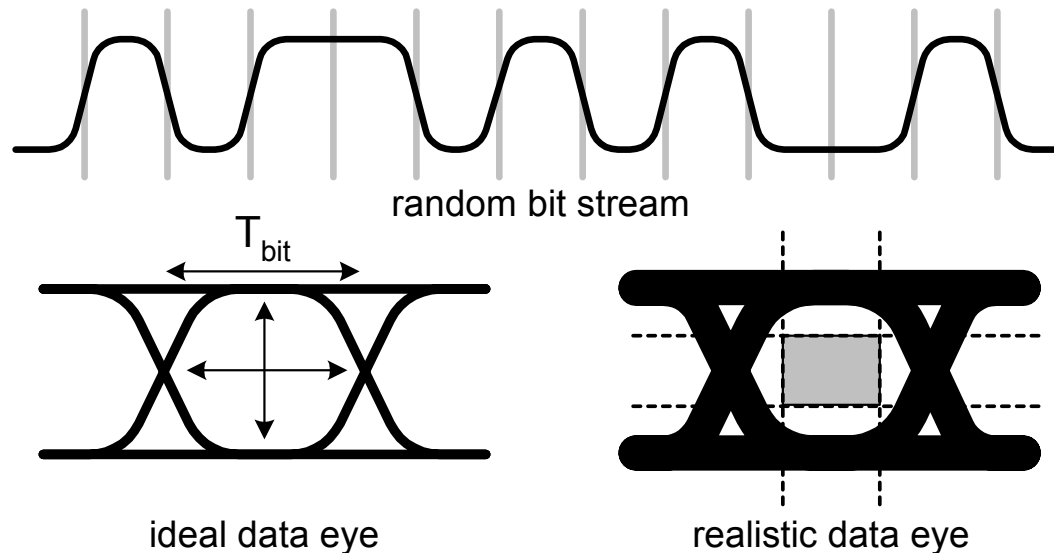
- High-speed links consist of 4 main components



- Serializing transmitter driver
- Communication channel
- De-serializing receiver samplers
- Timing recovery

# Performance Limitations

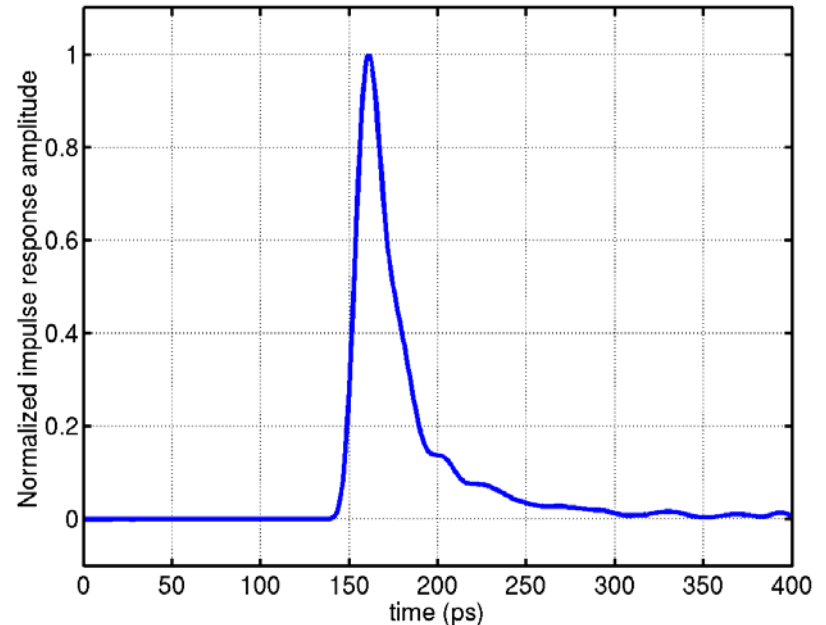
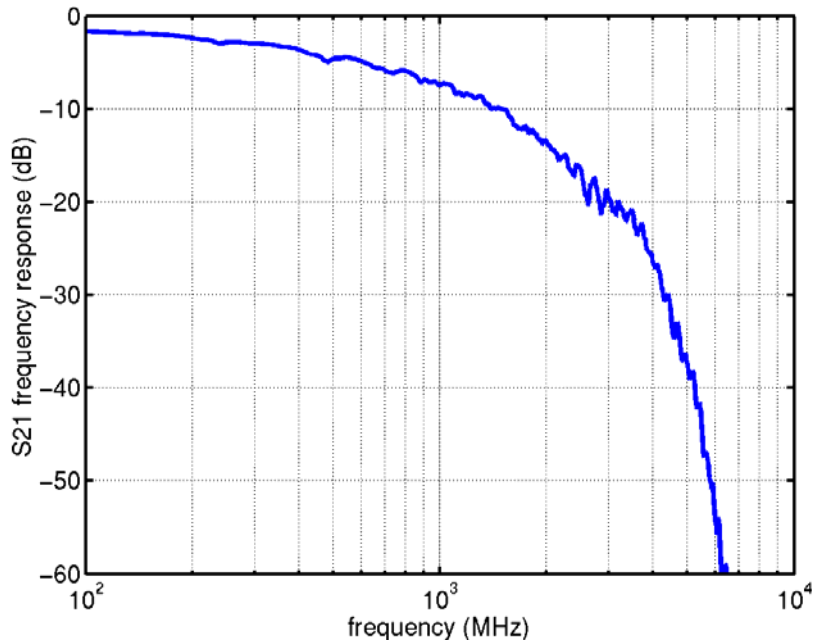
- Important to look at performance because higher performance can lead to lower power by trading off performance for energy reduction
- Several factors limit the performance of high-speed links
  - Non-ideal channel characteristics
  - Bandwidth limits of transceiver circuitry
  - Noise from power supply, cross talk, clock jitter, device mismatches, etc.
- Eye diagrams – a qualitative measure of link performance



# Channel Impairments and ISI

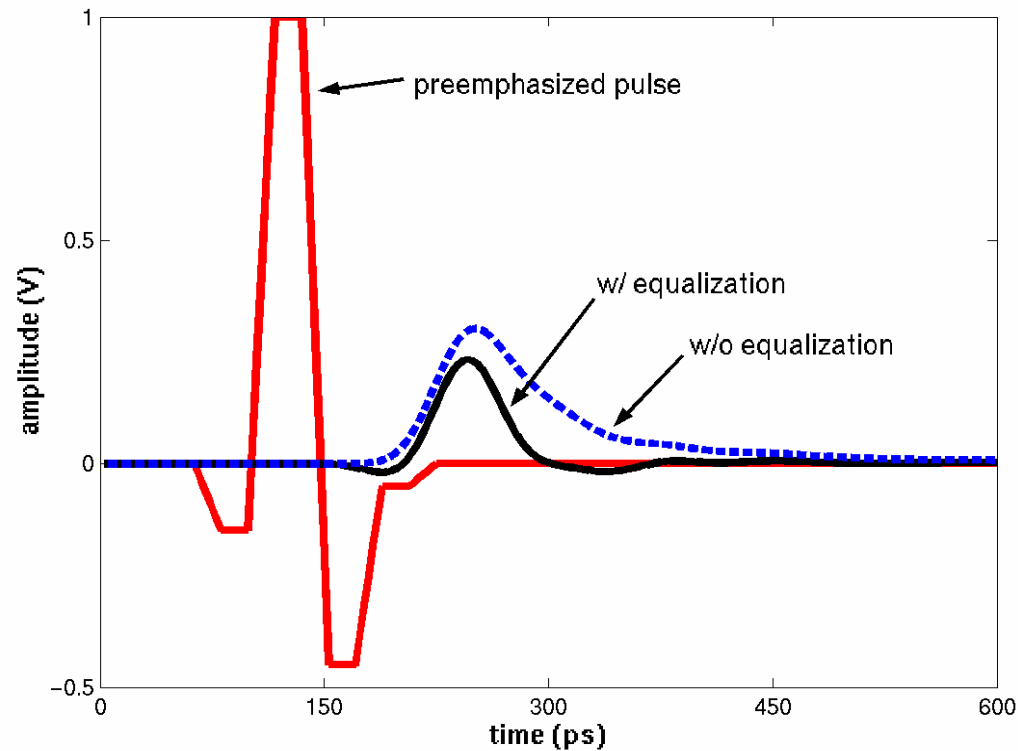
---

- One of the dominant causes of eye closure is inter-symbol interference (ISI) due to channel bandwidth limitations
  - Two ways to view channel impairments



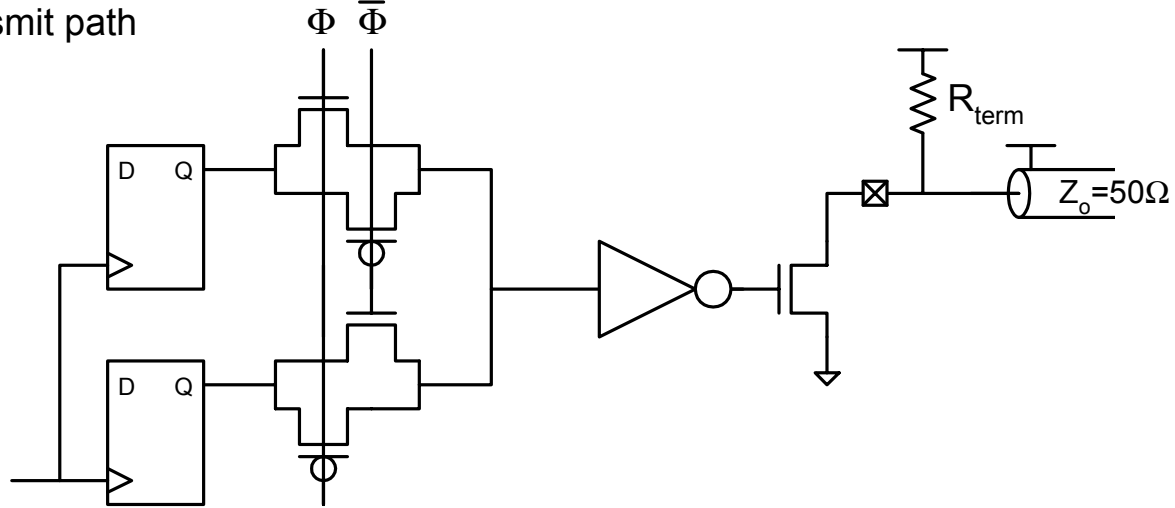
# Equalization

- Placing a high-pass filter in the signal path can counter the roll-off effects of the channel
  - Preemphasis or transmit-side equalization is commonly used

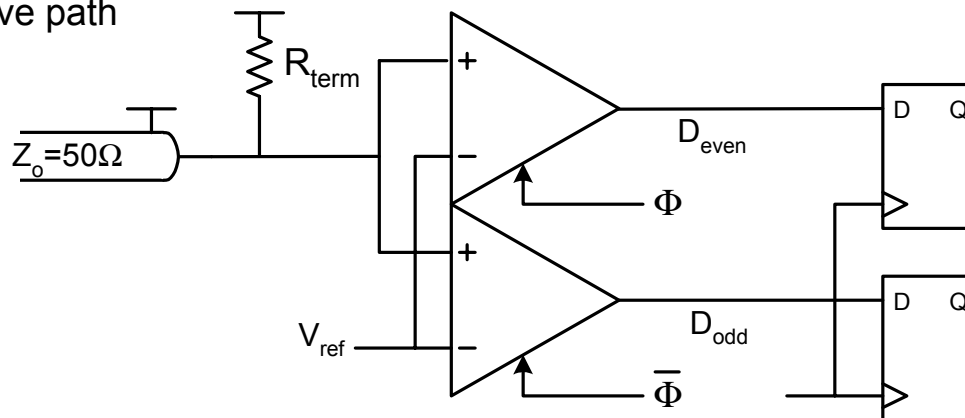


# Critical Path in Links

- The critical path in links can be as short as 1~2 gate delays
  - Transmit path

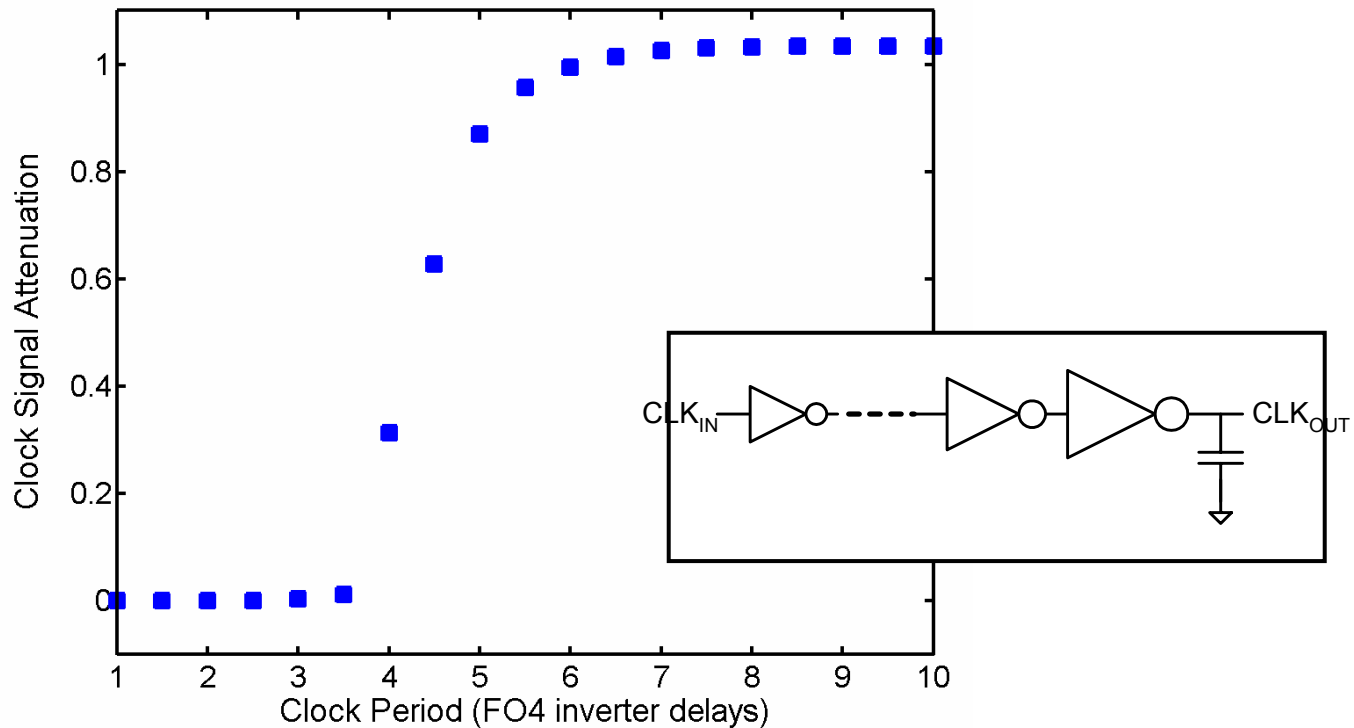


- Receive path



# Clock Frequency Limit

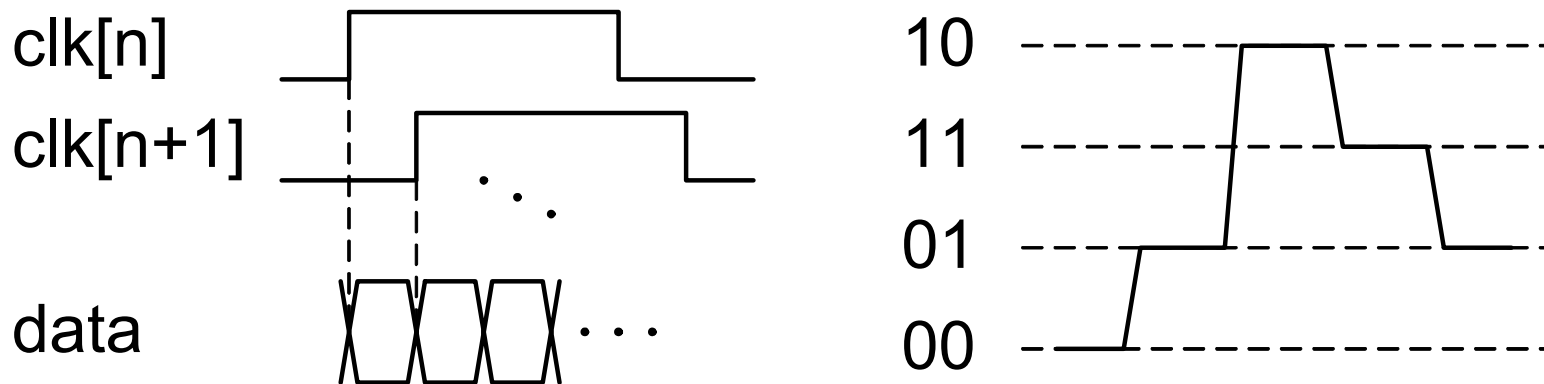
- While a symbol time can be short, there is a limit to the maximum on-chip clock frequency
  - Must distribute a clock driven by a buffer chain



- Overcome this limitation with parallelism

# Parallelism

- Parallelism can increase bit rate even with limited clock frequency
  - Time-interleaved multiplexing
  - Multi-level signaling



- Some performance issues to be wary of
  - Static timing offsets in multi-phase clock generator (DLL or PLL)
  - Requires higher voltage dynamic range in transmitter and receiver
- Parallelism can also be low power

# Sources of Noise

---

- Power supply noise
  - Translates into voltage and timing uncertainty
- Cross talk
  - Near- and Far-End Cross Talk (NEXT and FEXT)
  - High-frequency coupling
- Clock Jitter
  - Timing uncertainty in transmitted and sampled symbol
  - Probabilistic distribution of timing edges (bounded and unbounded components)
- Device mismatches and systematic offsets
  - Deterministic or systematic variation in timing edges from multi-phase clock generators

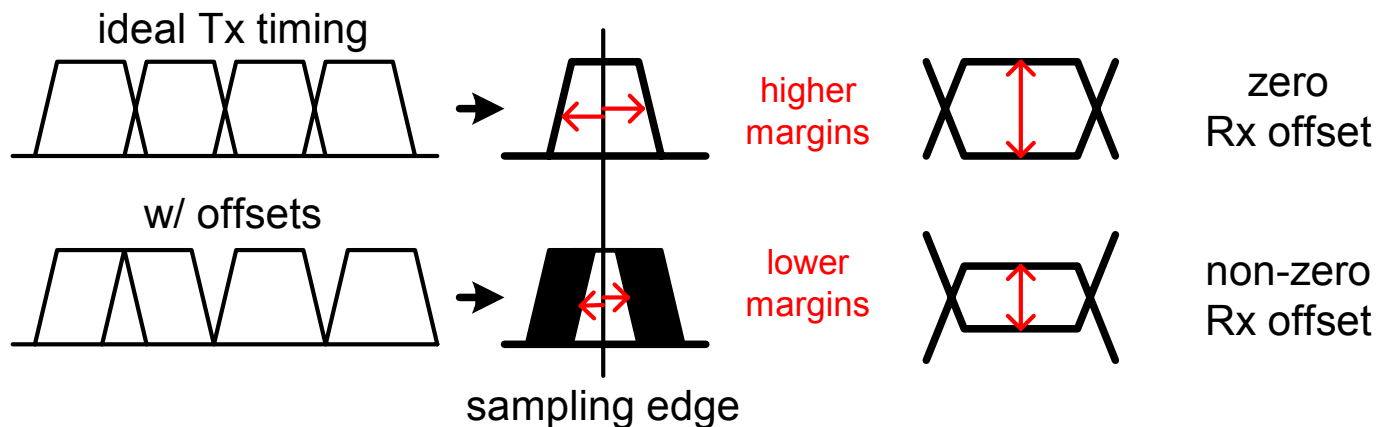
# Considerations for Low Power

---

- Low noise → low power
  - Target some signal to noise ratio (SNR)
  - Reducing noise allows for lower signal power
- Trade speed for lower power
  - Reducing bit rate improves SNR
  - Many noise sources are fixed → ratio of timing uncertainty to bit time improves (have longer bit times)
- Let's look at a few design choices for low power
  - Circuit level
  - Architecture level
  - System level

# Offset Calibration

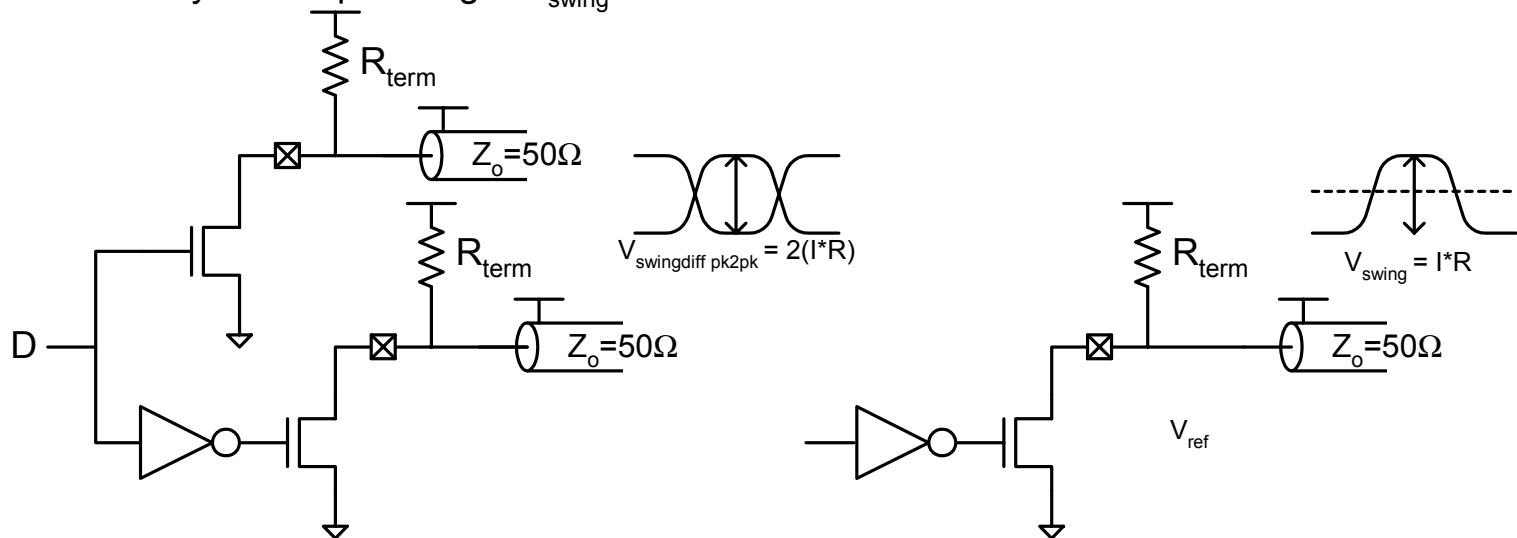
- Two sets of offsets that can manifest itself as voltage and timing uncertainty to close the eye and may require higher power to overcome them:
  - Multi-phase clock generator timing offsets
  - Receiver input voltage offsets



- Static offsets due to systematic (layout) and random (device) mismatches
  - Calibration enables more timing and voltage margins (i.e., lower noise)

# Differential Signaling

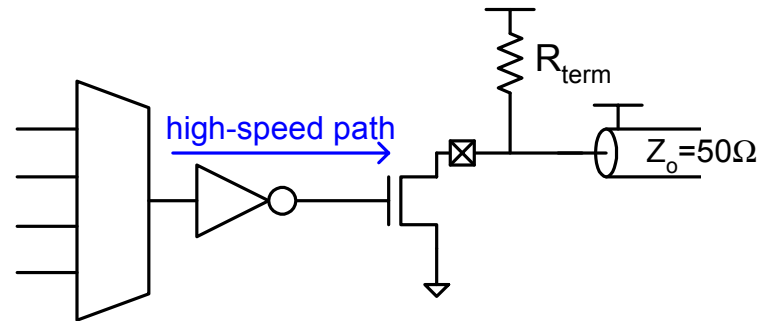
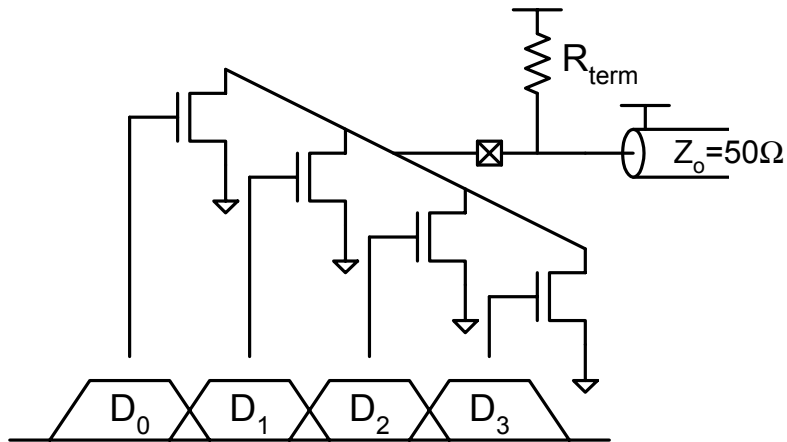
- Differential communication can lead to a lower power solution
  - Immunity to common mode noise
  - Injects less noise into the supplies
- But aren't there now are two channels that switch? Yes, but...
  - Signal amplitudes can be smaller on both channels
  - Alternative is pseudo-differential signaling but needs a reference voltage which can be noisy and require larger  $V_{\text{swing}}$



- What does it cost?
  - Requires two pins per link

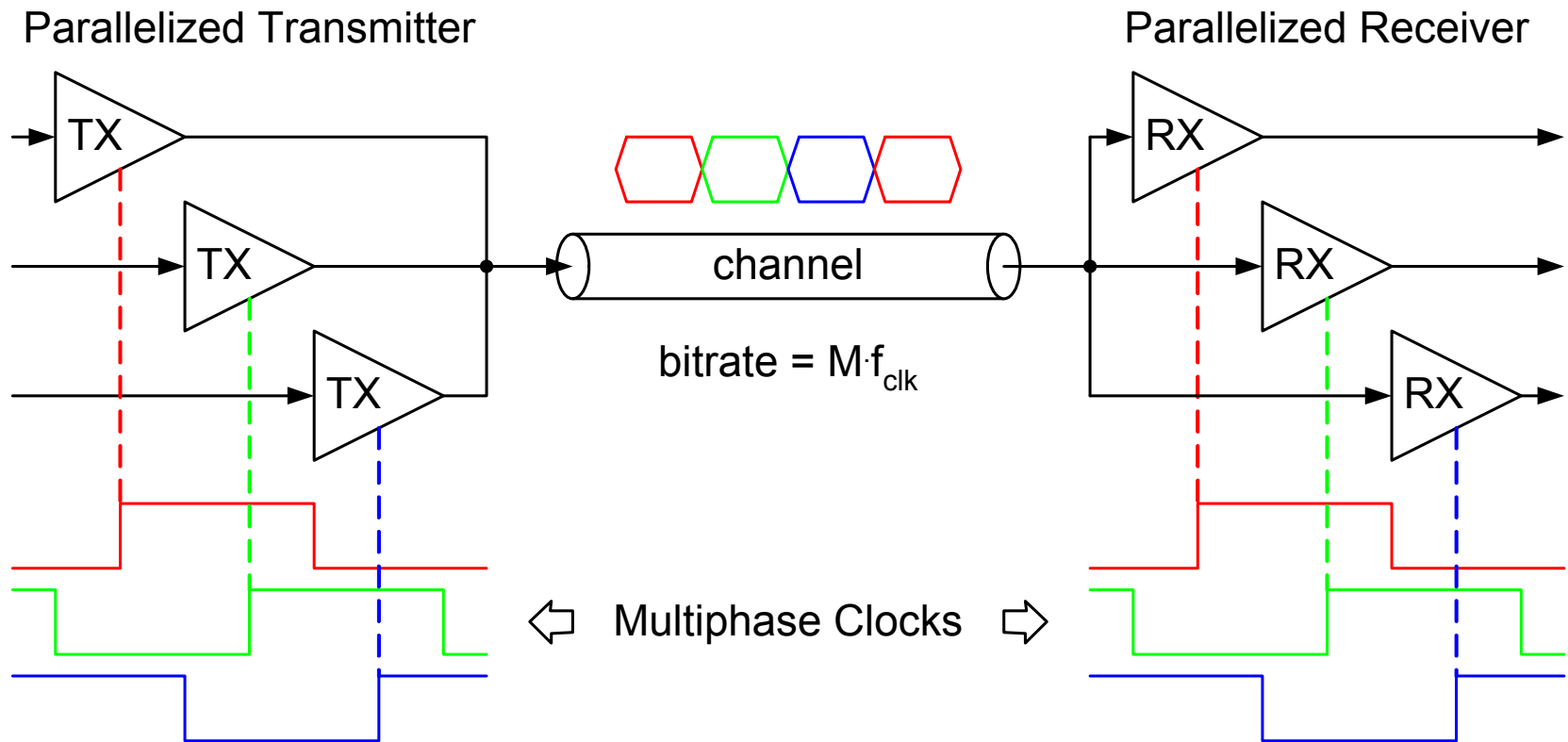
# Signal Multiplexing

- There are different options for choosing where to combine pulses to create sub-clock period symbols
  - Combine at the final transmitter stage vs. farther up stream



- $C_{\text{load}}$  for the clocks higher when combined at the final transmitter vs.
  - Need faster signal path after the multiplexer
- Best choice depends on implementation (see Zerbe, ISSCC2003)

# Multiplexing



# Multiplexing = Low Power?

---

With M:1 multiplexing,  $f_{\text{CLK}} = \text{bit rate}/M$

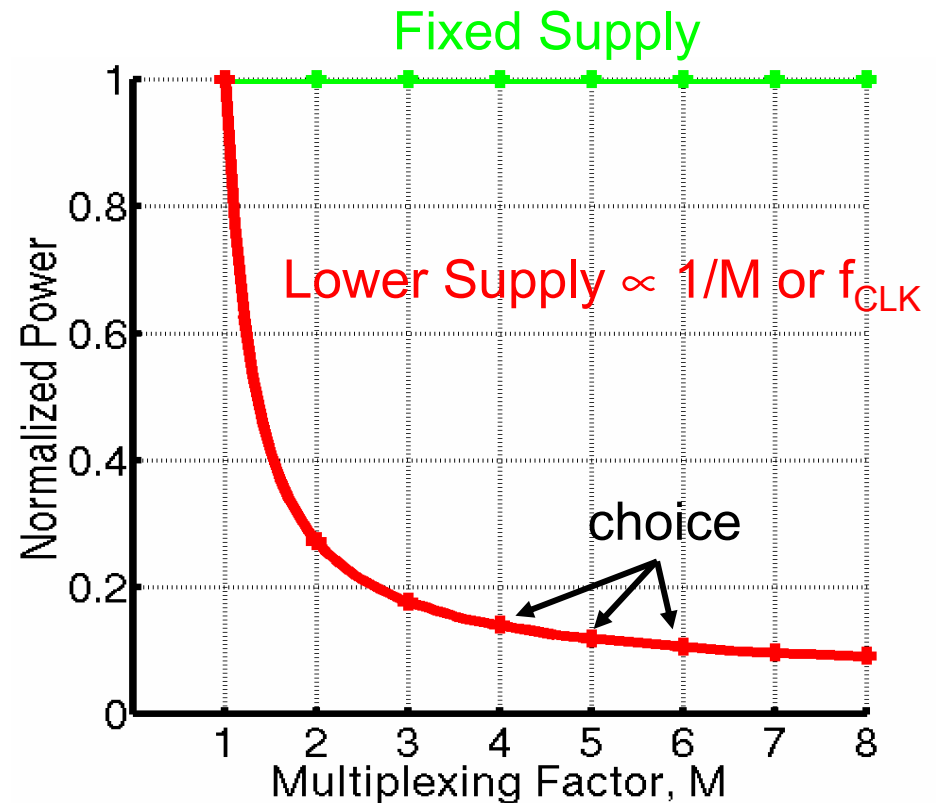
- Power =  $M \cdot C V^2 \cdot f = M \cdot C V^2 \cdot (\text{BR}/M) = C \cdot V^2 \cdot \text{BR}$
- With fixed supply, power does not vary with M

But wait, at lower frequencies, I can lower voltage!

- With lower supply voltage ( $V \propto f_{\text{CLK}} = \text{BR}/M$ ),
- Power decreases as  $\propto 1/M^2$ !

# Power vs. M

- Larger M
  - ⇒ Can reduce voltage
  - ⇒ Lower power
  - ⇒ Less accurate timing
    - static phase offsets
    - jitter
- Cannot make M arbitrarily large b/c there is a lower limit to V<sub>dd</sub>
- Choice: M= 4~6



This begs the questions... What if we make V<sub>dd</sub> adaptive w/  $f_{CLK}$ ?

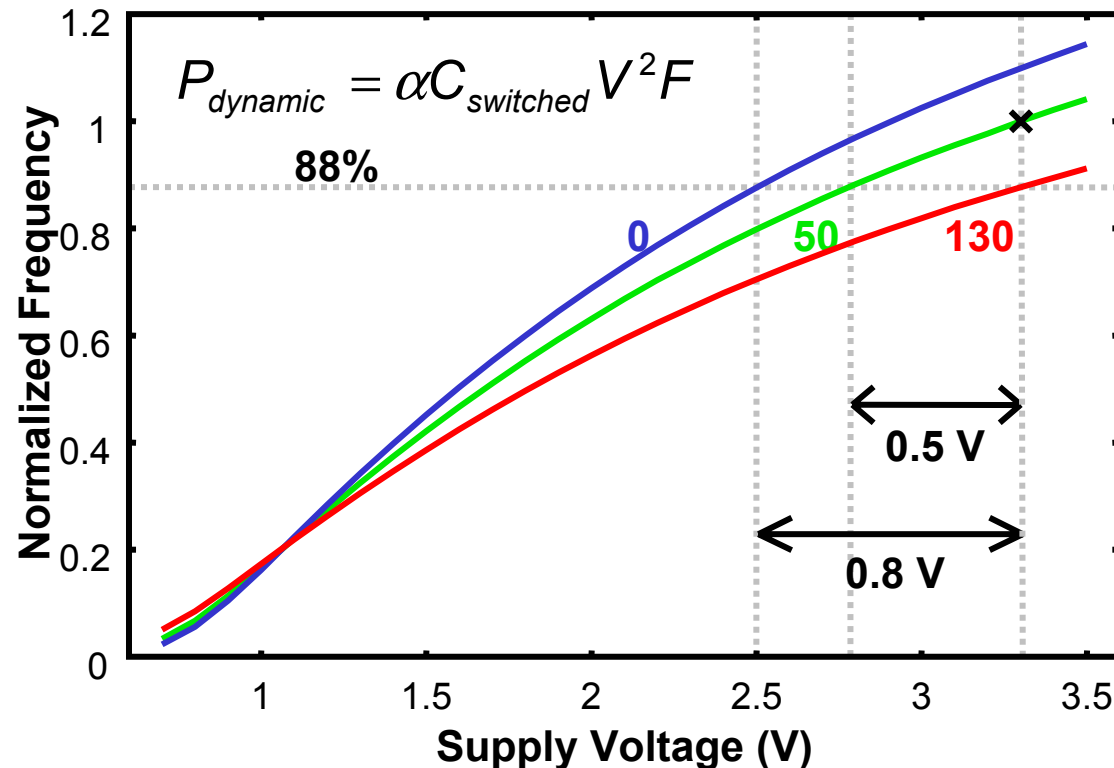
# DVS Links

---

- Dynamic Voltage Scaling (DVS)
  - Technique first introduced for digital systems (e.g., uP, DSP chips)
    - Lot's of work done in both academia and industry (e.g., Intel, Transmeta)
  - Allows trade off between speed and power
- Let's investigate DVS for high-speed links
  - Motivation and potential benefits
  - Design example from Dr. Jaeha Kim (ISSCC2002, JSSC2002, PhD thesis 2002)

# DVS Links

- Dynamic Voltage Scaling (DVS) can reduce power consumption in two ways
  - 1) Digital circuits operate at their most energy-efficient point in the presence of PVT variations by eliminating extra performance margins



# Trade Performance for Energy Savings

- 2) DVS enables trade off between performance and energy
- Reducing frequency alone reduces power but not energy per bit

