SMA5111—Final Project

SiGe-based Technology

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Outline

- Introduction
- SiGe HBT Technology
- Strain Silicon Technology

Introduction

Why SiGe?

- The smaller band gap of Ge compared to Si allows device designers greater scope in terms of band engineering when SiGe is used
- Fast Speed
- Integration capability through BiCMOS on a single chip
- Low Cost—driving force of any technology

Introduction

Why SiGe?

- Strain Si offers further bandgap engineering opportunities
- Applications for SiGe and strain Si include:
  - SiGe HBTs, IR detectors
  - Si, Ge, SiGe channel FETs

Although limited devices production now, the role of SiGe in the Si device industry is expected to increase in the future

SiGe HBT Technology

Advantage:

1. ability to selectively re-engineer the band gap of ordinary silicon, thereby increasing the transistors' inherent switching speeds.
2. By grading the Ge content across the transistor base region, the band gap performance can be significantly and selectively enhanced.

SiGe HBT—Devices Structure

The figure shows schematic cross section of SiGe HBT having a planar self aligned structure with a conventional poly-emitter contact, silicided extrinsic base, and deep- and shallow trench isolation.
The base was grown using

the UHV/CVD technique.

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Ge makes transistors better!!!

$$\frac{\beta(SiGe)}{\beta(Si)} = \frac{e^{\Delta E_{gSiGe}/kT}}{1-\exp(-\Delta E_{gSiGe}/kT)}$$

$$\frac{V_A(SiGe)}{V_A(Si)} = \frac{kT}{\Delta E_{gSiGe}}\left[\exp\left(\Delta E_{gSiGe}/kT\right)-1\right]$$

$$\frac{t_B(SiGe)}{t_B(Si)} = \frac{2kT}{\Delta E_{gSiGe}}\times\left[1-\frac{kT}{\Delta E_{gSiGe}}\left(1-\exp\left(-\Delta E_{gSiGe}/kT\right)\right)\right]$$

Strain Silicon Technology

1. Start with a conventional silicon wafer
2. A thin layer of a SiGe
3. A very thin layer of silicon is added on top of the SiGe layer.
4. The Si layer atoms tend to align themselves with the more widely spaced atoms in the underlying layer

A schematic of a basic strained Si heterostructure. The three basic elements are the bulk Si substrate, the epitaxial SiGe buffer layer, which creates a larger lattice constant, and the epitaxial tensile strained Si film, which provides for greater transistor performance.

Strain Silicon Technology

Strain Si lattice

Intentional Strain of the Channel

--lattice mismatch (Si and Ge)

--increasing Si spacing

--increasing carrier mobility

$Si_{1-x}Ge_x$ x typical 0.15--0.3

Key to the Strain Si Technology—
Low Defect-density Strain Si

1. The development of SiGe relaxed graded-layer technology by Eugene Fitzgerald of MIT provided an effective method for engineering the lattice constant of the SiGe film –(strain in the Si)
2. chemical-mechanical polishing (CMP) process introduced between the epitaxy of the relaxed SiGe buffer layer and the strain Si

Strain Silicon Technology

fabricated with 130 nm Si CMOS technology by United Microelectronics Corporation (UMC) in Taiwan. UMC is developing strained Si devices through a technology partnership with AmberWave Systems. the company showed drive current enhancements of 43% over bulk Si NMOS.

A cross-sectional electron micrograph of a strained

Si transistor fabricated by UMC

Current Involvement

Company	Strained Silicon Announcement	Implement Strained Silicon in production	Initially Strained Silicon Geometry	Demonstrated Device Performance	Initially Strained Silicon Device Type
AmberWave Systems Corp.	2001	Not Available	Not Available	Electron and hole mobility enhancement factor of 1.5-2..2	Various (HBT, MOSFET)
IBM Microelectronics	2001	2005	65 nm	30% improvement in drain current	NMOS with Strained Silicon Channel
Hitachi Ltd.	2001	Not Available	<100 nm	70% improvement for current in NMOS and 51% for PMOS	MOS Transistor with Strained Silicon Channel
Intel Corp	2002	2003	90 nm	10%-20% improvement in current	Demonstrated on 52 megabit SRAM Chip to be used as a prototype in the production of Pentium 4 microprecessor

Source: Lubab Sheet SEMI 2002

The End

Thanks Very Much