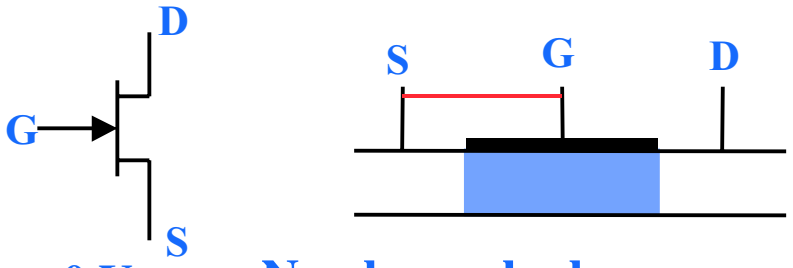
Lecture 11 - Heterojunction FETs - General HJFETs, HFETs

- **Last items from Lec. 10**
  - Depletion mode vs enhancement mode logic
  - Complementary FET logic (none exists, or is likely to anytime soon)
  - Why only GaAs so far?
- **General look back at MESFET processing**
  - Key device components; processing challenges
  - Systematic look at processing sequences
  - Opportunities for exploiting heterostructures
- **General principles of heterostructure use in FETs**
  - General objectives
  - Specific applications
    - Improving substrate isolation
    - Improving gate characteristics
    - Improving channel conductance
- **HFETs - doped channel HJFETs**
  - Basic structure
  - Device enhancement using pseudomorphic layers
    - Strained channels
    - Strained gate

Logic Gates - enhancement and depletion mode FETs

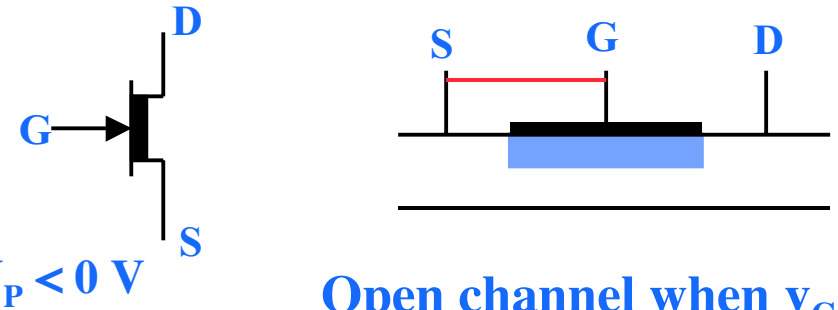
Enhancement mode



$V_P > 0$ V

No channel when $v_{GS} = 0$; $V_P > 0$ V; what we are familiar with from our MOSFET experience.

Depletion mode



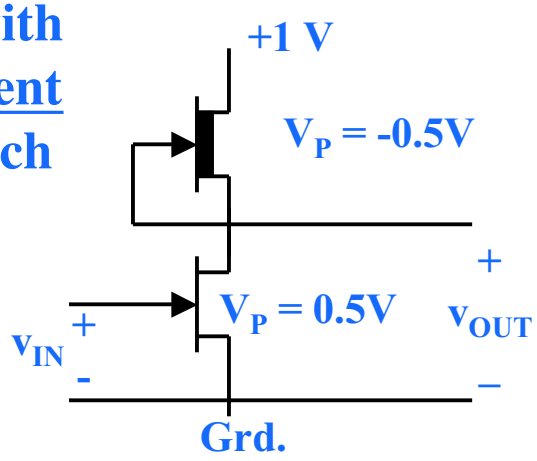
$V_P < 0$ V

Open channel when $v_{GS} = 0$; $V_P < 0$ V; the more common situation in MESFETs and JFETs.

Control of V_P is the #1 process issue with MESFETs

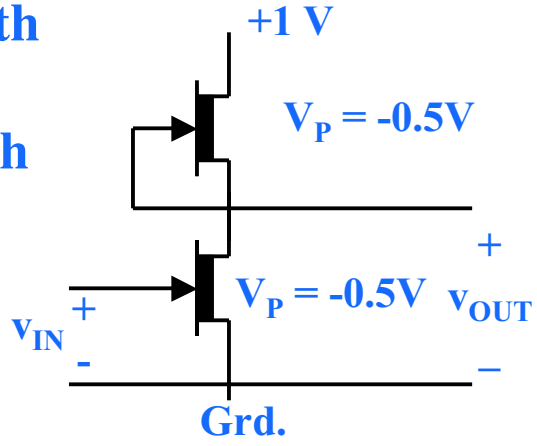
Logic Gates - the problem with depletion mode FETs

Inverter with enhancement mode switch



v_{IN}	Switch	v_{OUT}
0 V (lo)	Off	1 V (hi)
1 V (hi)	On	0 V (lo)

Inverter with depletion mode switch

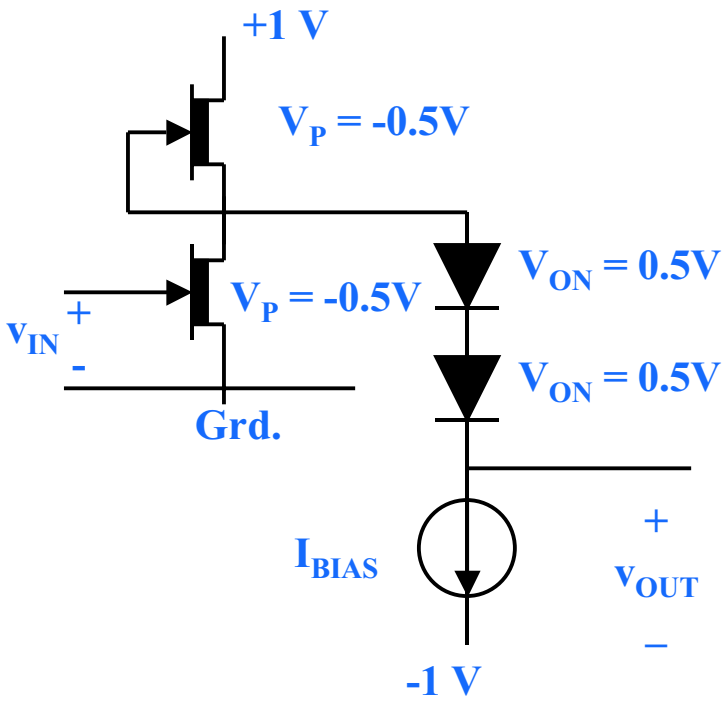


v_{IN}	Switch	v_{OUT}
0 V (hi)	On	0 V (lo)
-1 V (lo)	Off	1 V (hi)

Inverts, but the levels are not consistent. We need to add level shifting!

Logic Gates - living with depletion mode FETs

Adding level shifting to output



v_{IN}	Switch	v_{OUT}
0 V (hi)	On	-1 V (lo)
-1 V (lo)	Off	0 V (hi)

Now the levels are consistent…
but the circuit is more complicated.

Note: The level shifting could also be done at the input.

FET Fabrication Issues

The main pieces of any FET:

- the channel
- the source and drain ohmic contacts
- the gate
- the device isolation
- the encapsulation

Issues particular to MESFETs :

- semi-insulation substrate
- Schottky barrier gate
- threshold control
- gate resistance
- source and drain series resistances

Looking more closely at issues unique to MESFETs

Semi-insulating substrate:

- effectively eliminates back-gate effects if the processing is done properly

Schottky barrier gate:

- limits level of channel doping
- restricts choice of p- or n-type channel
- limits degree of turn-on of channel

Threshold control:

- an issue in any FET
- a function of a, ϕ_b, N_{Dn}
- surface states and their control is a special issue with III-Vs

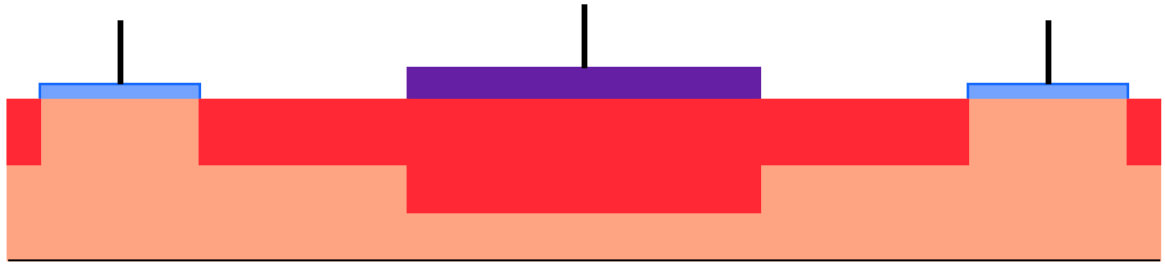
Cont. with issues unique to MESFETs

Gate resistance:

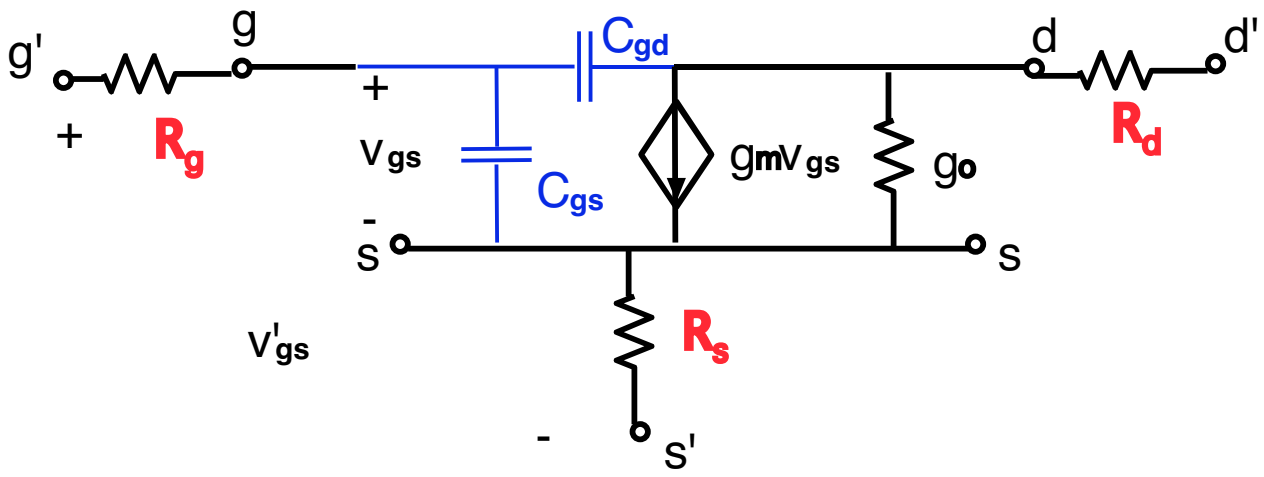
- an important issue in short channel length devices and at high frequencies

Source and drain series resistances:

- agravated by surface depletion
- especially problematic for enhancement mode



The impact of parasitic series resistances: reduced gain and bandwidth

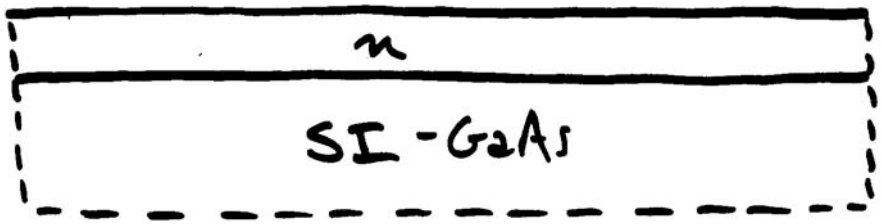


Source and drain series resistances reduce gain at all frequencies.

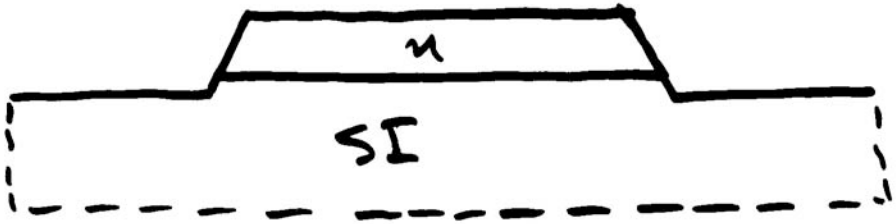
The impact of the gate series resistance appears at high frequencies and reduces the gain and bandwidth.

MESFET Fabrication - Mesa on Doped Epi

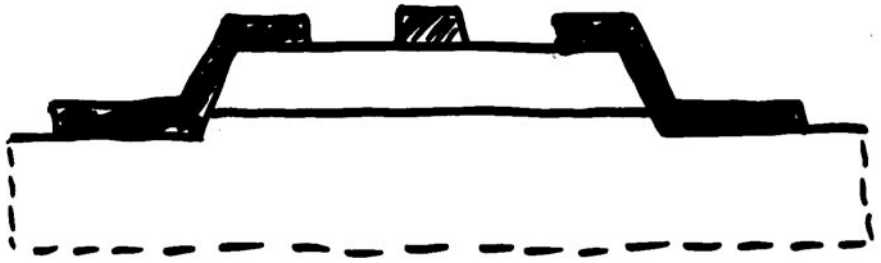
A. Initial epi-wafer



B. Mesa etch



C. Gate and ohmic metal

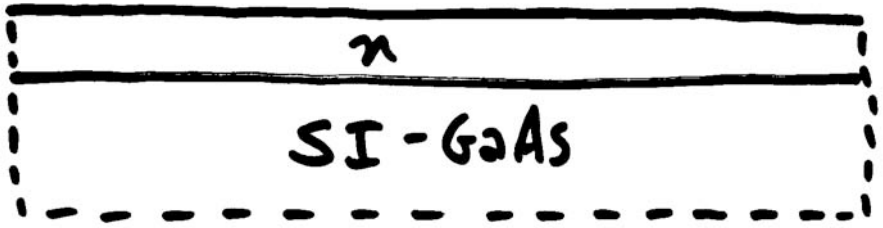


Device-to-device isolation is achieved by mesa-etching. A problem is lack of planarity.

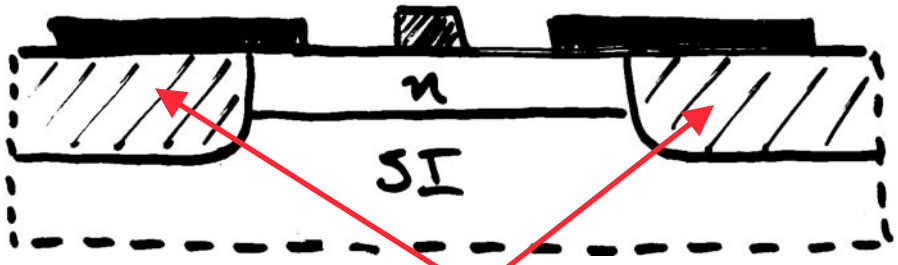
MESFET Fabrication - Proton bombardment isolation

implantation of H^+ ions will make moderately doped GaAs highly resistive

A. Initial epi-wafer



B. Processed device

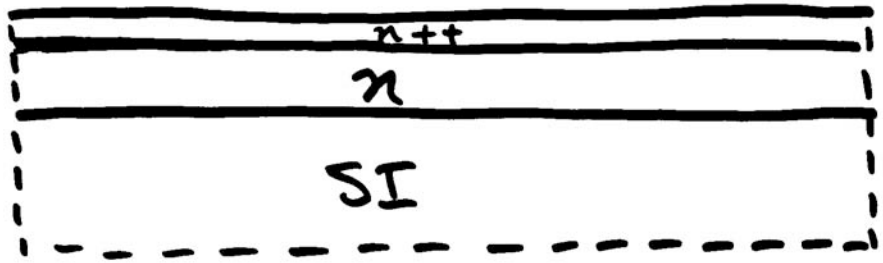


Proton bombarded regions -
multiple energy H^+ implants.

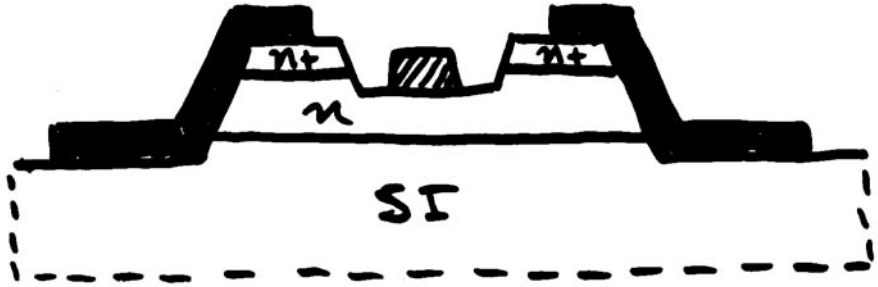
Provides excellent isolation and yields a planar structure.
High processing temperatures will anneal out the damage.

MESFET Fabrication - n+/n Epi with recessed gate

A. Initial epi-wafer



B. Processed device



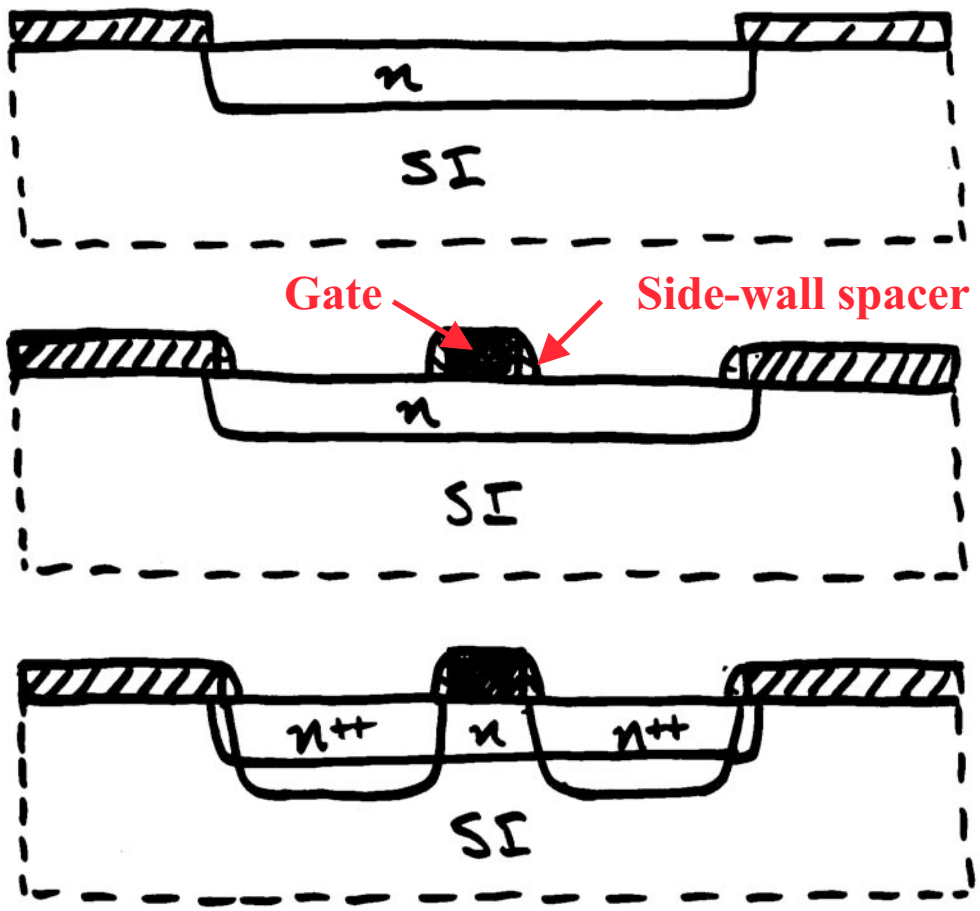
Requires excellent control over etching to be successful. Can be used with proton bombardment if n^+ etched away in field.

MESFET Fabrication - Ion implantion into SI-GaAs

A. Initial epi-wafer

B. Gate deposition, side-wall formation

C. Self-aligned source and drain implants



Epitaxy is avoided, and structure is self-aligned. Consistent activation of implants requires process discipline.

Heterojunction FETs - moving the MESFETs with heterojunctions

Gate characteristics:

- barrier height
- leakage current

Channel conductivity:

- carrier concentration
- carrier mobility

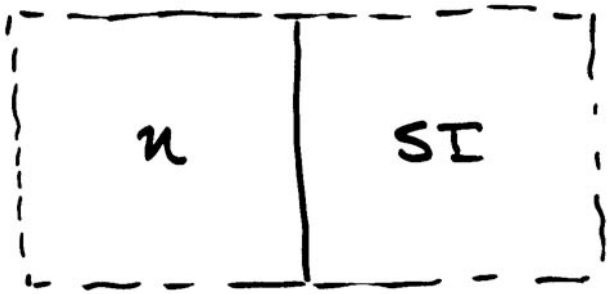
Substrate isolation :

- reducing injection

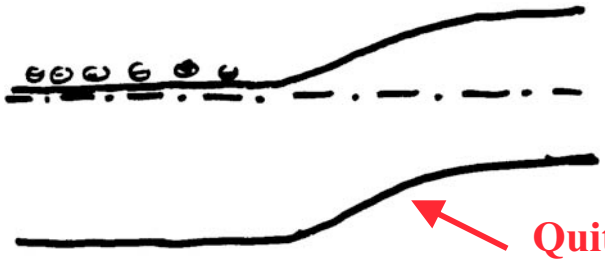
There are improvements we can make in all of these areas

Improving substrate isolation - lower boundary of the MESFET channel is not abrupt

A. Channel-substrate interface



B. Lower confinement



Quite gradual if on undoped SI substrate

- Carriers can "spill out" of the channel into the substrate
  - the gate then has less control (g_m suffers)
  - these carriers don't respond to the signal on the gate (response time suffers)
  - output characteristics don't saturate well (g_o is large)

Spill out into substrate

- a Monte Carlo simulation

A. Spatial distrubution at one instant

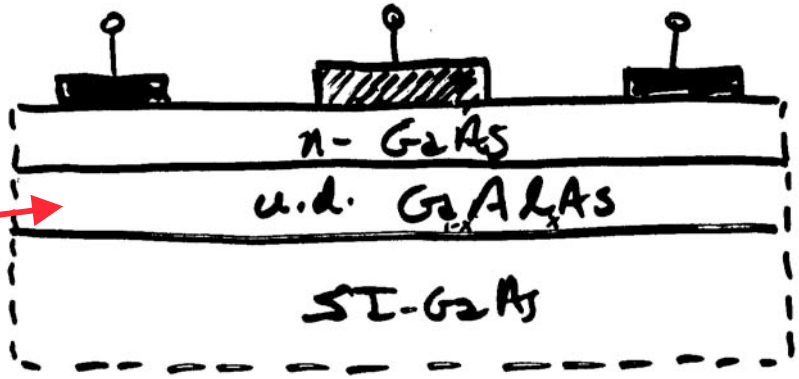
B. Equipotential lines

Ref: Awano, et al, Electronics Letters 19 (1983) 20.

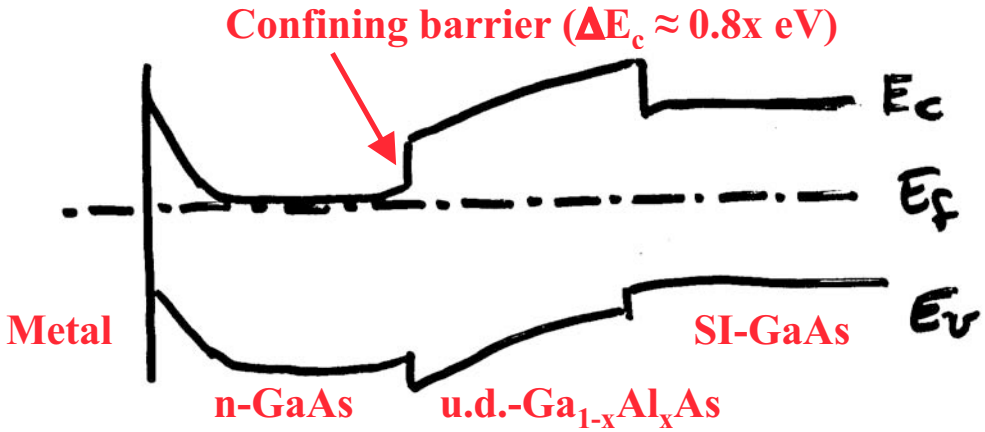
- What are some solutions?
  - wide bandgap buffer layer
  - low temperature, high arsenic content buffer
  - air isolation

Solutions for substrate isolation - wide bandgap buffer layer

Undoped AlGaAs buffer layer



Lower barrier for confinement



- This type of wide bandgap buffer is widely used, but this barrier is not infinite and once in the AlGaAs the carriers can move into the substrate.

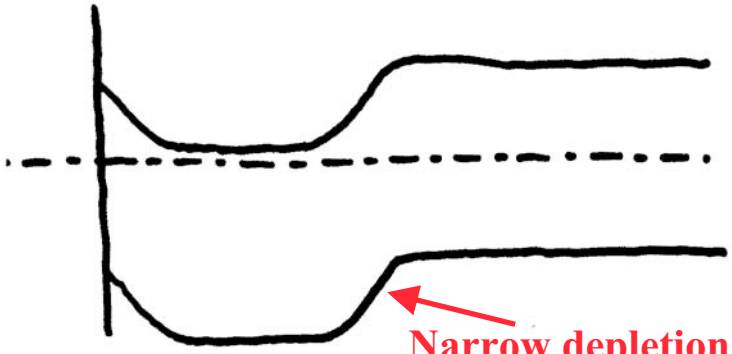
Solutions for substrate isolation - low temperature, high arsenic content buffer

GaAs grown by MBE at ≈ 200˚C with excess As:

1) is semi-insulating
2) has a large mid-gap state density
3) has a very short carrier lifetime

Low-T GaAs developed at MIT Lincoln Labs

With a large electronic state density in the buffer the depletion region is very narrow.



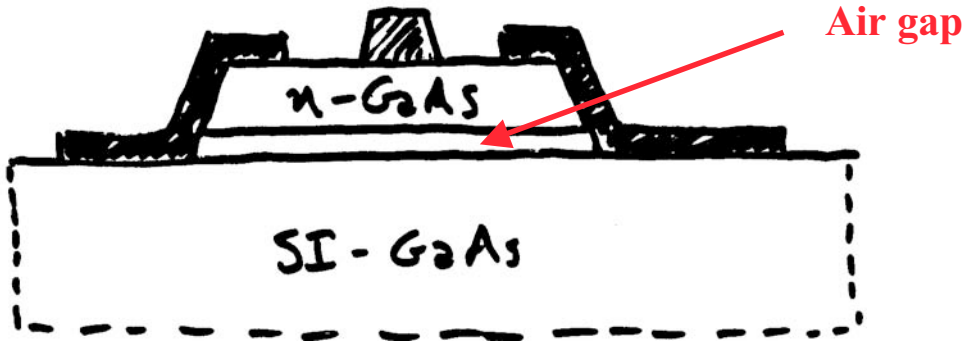
Narrow depletion region results in more abrupt barrier

- Now the barrier may be even higher and the carriers that surmount it have a very short lifetime. Note: The use of Cr- or Fe-doped SI substrates has a similar effect but these have proven difficult to reproduce and control.

Solutions for substrate isolation - air isolation

The availability of selective wet etches makes it possible to use an air buffer:

1) AlAs spacer grown during epitaxy
2) mesa etched through AlAs layer and leads patterned to the substrate
3) selective etch (HF or HCl) used to remove AlAs



- Primarily a research novelty in the FET world, but we will see this idea used to create air gaps for use in other devices later on. .

Improving gate characteristics - limited by low Schottky barrier height

We would really like to have an insulated gate as in a MOSFET, but surface states have precluded realization of stable, hysteresis-free MIS capacitors on the III-Vs.

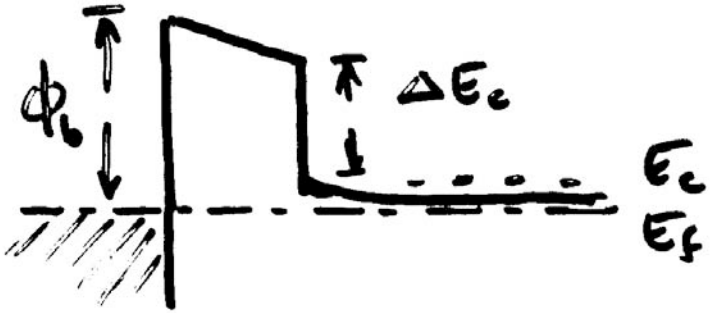
(The closest people have come is to achieve very limited success sulfidizing GaAs and to depositing SiO_2 on InP.)

A wide bandgap semiconductor can be used as a pseudo-insulator to get something approaching MOS action.

- **A wide bandgap gate "dielectric" can have two benefits:**
  - **increase barrier effectiveness, thereby increasing the degree to which the channel can be turned on.**
  - **place the gate closer to the channel carreirs, thereby increasing its control over them, i.e., increasing g_m.**

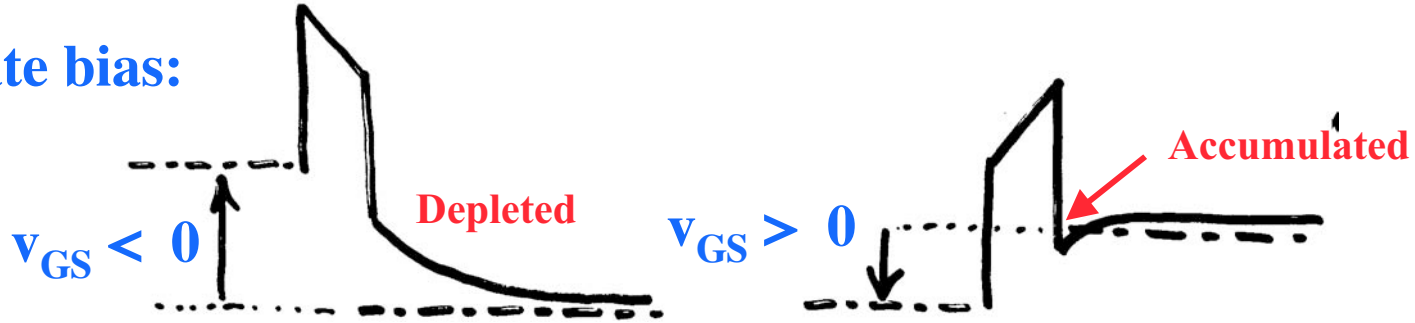
Solutions for the gate - wide bandgap "dielectric"

The structure:



A good rule of thumb with $Al_xGa_{1-x}As$-GaAs HJs is that $\Delta E_c \approx 0.8x$ eV)

With gate bias:



- With forward bias on the gate the channel charge can accually be increased above the background doping with accumulation occuring at the hetero-interface.

Improving channel conductance - g_m and ω_t both improve with higher channel conductance

To get higher channel conductance one must…

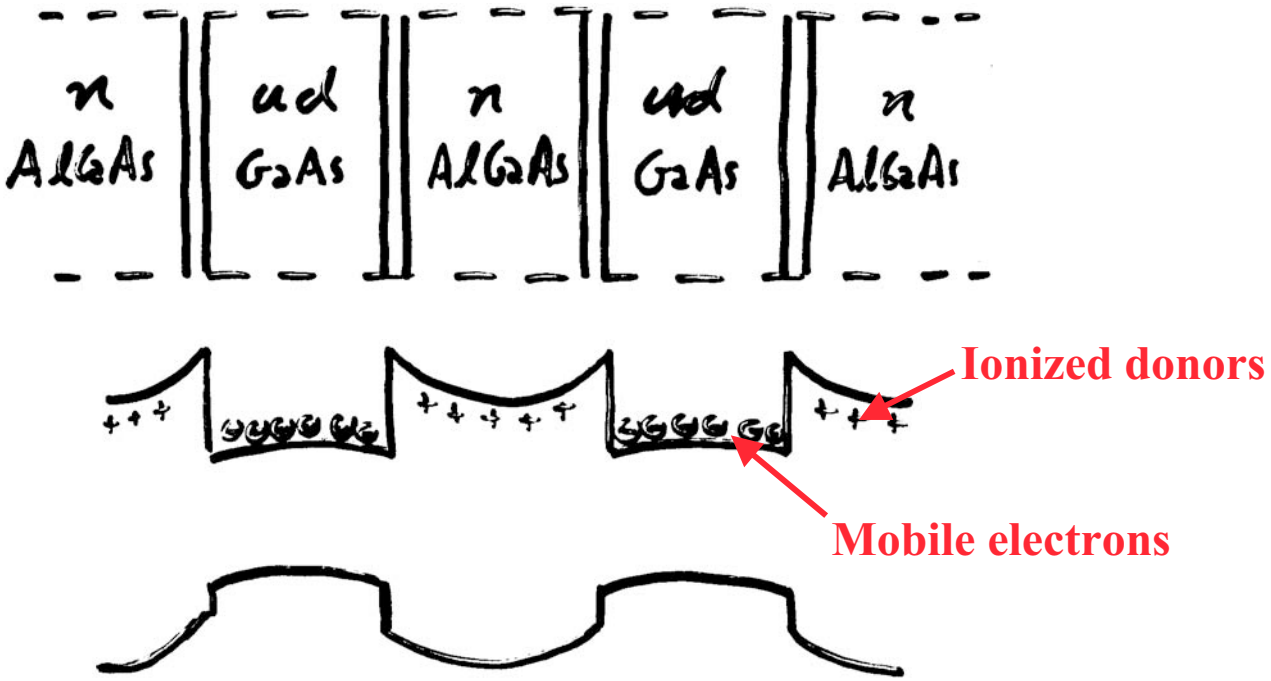
- **use higher mobility materials, and/or**
- **get more carriers into the channel**

To do this:

- **Increase the barriers (top and bottom) to get more carriers into the channel** (we just saw this)
- **Use $In_xGa_{1-x}As$ to increase the electron mobility**
  (we talked about pseudomorphic and metamorphic layers earlier)
- **Use modulation doping**
  (An important cause of scattering are ionized imputies and higher doping levels result in lower mobilities, and conductivity goes up only slightly. Device noise also increased significantly. A solution is modulation doping.)

Modulation doping - separating dopants and carriers

Demonstration structure:



- The objective is to increase the carrier mobility and reduce the noise associated with ionized impurity scattering

Modulation doping - separating dopants and carriers

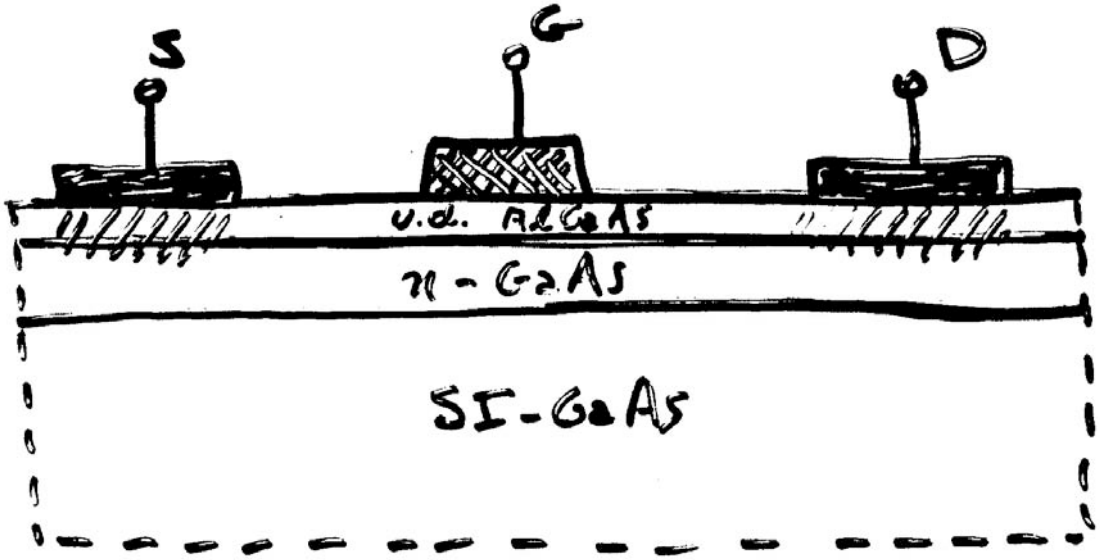
Mobility comparison:

- Carrier mobility is increased and scattering noise is reduced.

Heterojunction FETs - the doped channel HJFET (the HFET)

Structure:

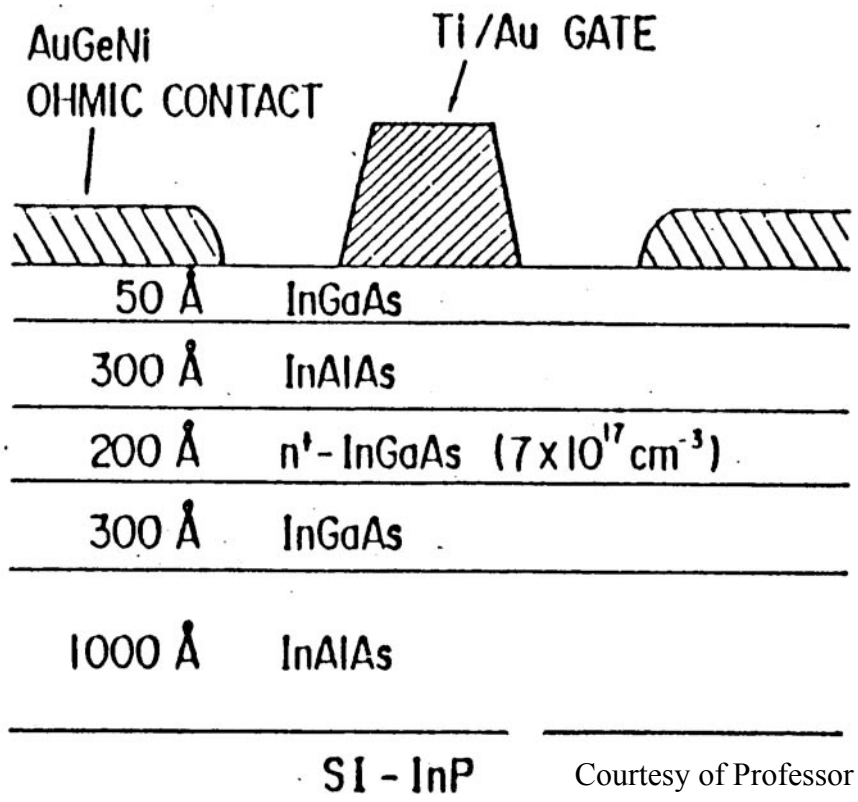
- a wide bandgap layer under the gate



We discussed the impact of this on the gate earlier. Now we will look at some research results.

Doped channel HJFET - the HFET

Using InGaAs and InAlAs on InP: Lattice-matched structure



Courtesy of Professor Jesus Del Alamo.

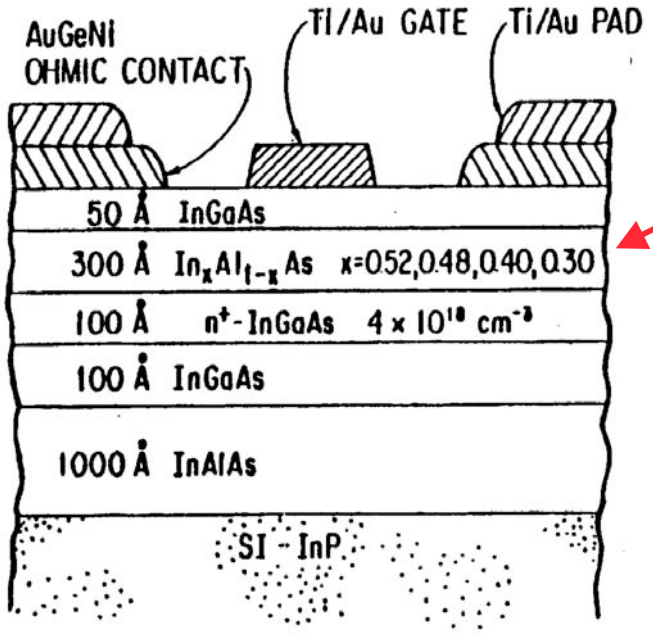
- **The carrier mobility can be increased and the barrier height can be raised if strained layers are used. Both were studied….**

Work of Prof. Jesus del Alamo and his students at MIT.

Image courtesy of Jagdeep Bahl. Used with permission.

Doped channel HJFET - the HFET

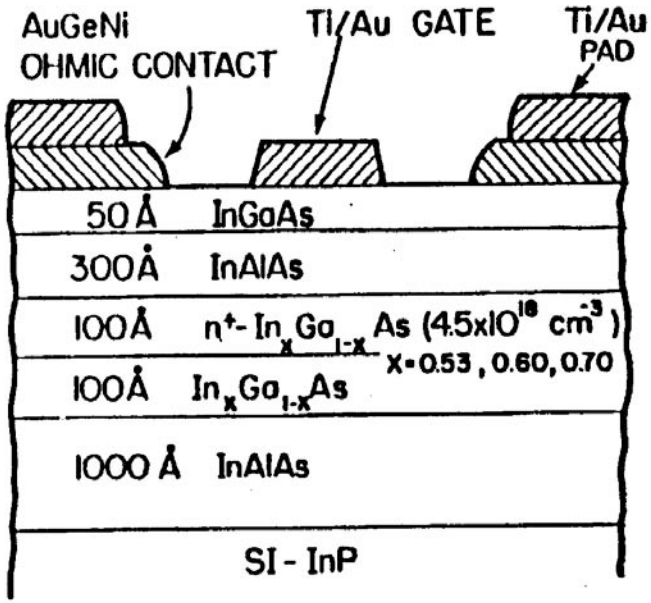
Pseudomorphic InGaAs and InAlAs on InP: strained layers



Pseudomorphic InAlAs barrier

Pseudomorphic, doped InGaAs channel

Courtesy of Professor Jesus Del Alamo.



Courtesy of Professor Jesus Del Alamo.

- **We will look at the results obtained for both approach in turn.**

Work of Prof. Jesus del Alamo and his students at MIT.

Doped channel HJFET - the HFET
Pseudomorphic InAlAs barriers: increasing barrier height

Pseudomorphic InAlAs barrier (x = 0.30, 0.40, 0.48, and 0.52)

(Images deleted)

See S. Bahl, W.J. Azzam, and J. del Alamo, IEEE Trans. Electron Dev. 38 (1991) 1986-1992.

Doped channel HJFET - the HFET

Pseudomorphic InGaAs channels:

increasing channel mobility and barrier height

Pseudomorphic
InAlAs channel
(x = 0.53, 0.60, 0.70)

(Images deleted)

See S. Bahl and J. del Alamo, 2nd Int. Conf. on InP and Related Compounds.