Published February 1, 2003. Distribution restricted to Sponsors until May 1, 2003.

AUTO-ID CENTER

WHITE PAPER

Manufacturing Cost Simulations for Low Cost RFID systems

Gitanjali Swamy, Sanjay Sarma

AUTO-ID CENTER MASSACHUSETTS INSTITUTE OF TECHNOLOGY, 400 TECHNOLOGY SQUARE, SIXTH FLOOR, CAMBRIDGE, MA 02139-4307, USA

ABSTRACT

In a previous Auto-ID publication, "Towards a 5¢ Tag" [1], we speculated on manufacturing and system methods to approach the elusive goal of a 5¢ Radio Frequency Identification (or RFID) tag. We extend our cost analysis in this paper and simulate manufacturing and assembly processes to examine the feasibility of the 5¢ tag. We do so assuming that large volumes are being manufactured achieving which is, of course, another challenge entirely. We experiment with variations in process, throughput and component variables to estimate what will be required to approach the 5¢ goal. As part of this experiment, we examine both the semiconductor manufacturing and the assembly of RFID tags. Our approach consists of two steps: bench-marking the processes employed and the equipment used, and 2) cost model simulation using this benchmark data. Our simulation models are inspired on earlier work on semiconductor costing at SEMATECH and at the University of California at Berkeley.

Published February 1, 2003. Distribution restricted to Sponsors until May 1, 2003.

WHITE PAPER

Manufacturing Cost Simulations for Low Cost RFID systems

Biography

Gitanjali Swamy

Gitanjali Swamy received her bachelors in Electrical Engineering from the Indian Institute of Technology, Kanpur and her M.S. and Ph.D. from U.C. Berkeley in Computer Engineering. Dr. Swamy has worked companies such as Booz Allen & Hamilton, Digital Equipment Corp and Mentor Graphics Corp. She has authored 20 academic publications in a number of IEEE/ACM conferences like ICCAD, DAC and VLSI design.

Sanjay E. Sarma
Research Director

Sanjay Sarma received his Bachelors from the Indian Institute of Technology, his Masters from Carnegie Mellon University and his PhD from the University of California at Berkeley. In between degrees he worked at Schlumberger Oilfield Services in Aberdeen, UK, and at the Lawrence Berkeley Laboratories in Berkeley, California. Prof. Sarma's Masters thesis was in the area of operations research and his PhD was in the area of manufacturing automation. From 1995 to 1999, Dr. Sarma was an Assistant Professor in the Department of Mechanical Engineering at the Massachusetts Institute of Technology. He is now an associate professor.

WHITE PAPER

Manufacturing Cost Simulations for Low Cost RFID systems

Contents

1. Introduction 3
   1.1. Background 3
   1.2. Costing RFID Tag Manufacturing 3
   1.3. Capacity and Volume: Some Editorial Comments 4
   1.4. A Caveat 6
2. Understanding Passive RFID Devices 6
3. Understanding the Manufacturing Process 7
   3.1. Semiconductor Manufacture 7
   3.2. Assembly 10
4. The Simulation Model 12
5. Results 14
6. Conclusions 18
7. Acknowledgement 18
8. Bibliography 19

1. INTRODUCTION

In a previous Auto-ID publication, "Towards a 5¢ Tag", we speculated on manufacturing and system methods to approach the elusive goal of a 5¢ Radio Frequency Identification (or RFID) tag [1]. We extend our cost analysis in this paper and simulate manufacturing and assembly processes to examine the feasibility of the 5¢ tag. We do so assuming that large volumes are being manufactured – achieving which is, of course, another challenge entirely. We experiment with variations in process, throughput and component variables to estimate what will be required to approach the 5¢ goal. As part of this experiment, we examined both the semiconductor manufacturing and the assembly of RFID tags. Our approach consists of two steps: benchmarking the processes employed and the equipment used, and cost model simulation using this benchmark data.

1.1. Background

Over the last three and a half years, the Auto-ID center has created the components of a system which will enable ubiquitous use of RFID tags. The tags designed by the Auto-ID Center and its partner companies are passive wireless RFID devices with a unique number which can uniquely identify almost every object in the supply chain – and indeed almost every object beyond. Typical tags today cost between 40¢ and $1.00 (US) depending on the scale and complexity of the tag.

Auto-ID tags are simpler and cheaper because of our mantra of minimalism. The Auto-ID **system** reduces the information stored on the most basic tag. The tag merely stores an Electronic Product Code™, or EPC™, and the EPC™-associated knowledge resides on the network. Simplicity, along with a platform approach, has the benefit of enabling many applications based on one core technology, and results in economies of scale. It has two implications on the manufacturing process. First, the IC is much smaller, saving silicon cost. Second, the yield is likely to be much higher because the probability of a defect is greatly reduced. This, of course, impacts testing costs. Both factors result in reduced cost per tag [1].

1.2. Costing RFID Tag Manufacturing

Our task was to study the costs involved in RFID manufacturing. Tags consist of integrated chips (IC's) and an antenna-substrate assembly. Figure 1 shows the internals of a typical near-field 13.56 MHz RFID tag complete with a coiled antenna and chip. IC manufacturing has received a great deal of attention from the now mature silicon industry. RFID packaging and conversion, unfortunately, is a relatively new and much smaller industry, and does not have the benefit of the same body of previous research.

Figure 1: RFID IC and Antenna, Courtesy Rafsec OY.

The semiconductor industry has studied the problem of semiconductor costing extensively. In our research, we relied on previous work done by the SEMATECH consortium and the UC Berkeley CSM project [4,5,7,9]. The RFID tag assembly industry is more fragmented and processes are less standard. There is a dearth of established benchmarks of standard processes for RFID tag assembly. For the assembly process, we conducted a benchmark by interviewing several manufacturing companies and profiling 130 machines used in the tag assembly process [6]. We then used our data on these machines as input to a cost model which was based on the CSM analysis.

There are several alternative processes for manufacturing RFID tags. In this study, instead of focusing on a particular process, we experimented with different process parameters and varied everything including the numbers of mask layers, metal layers, poly layers, to antenna costs, system throughputs, die sizes, process technologies, and even capital expense (capex) recovery times. We looked mostly at traditional processes rather than at new processes, which are difficult to model. Our goal was to understand whether a 5¢ cost is achievable at some production quantity, and what the key process parameters are, using these traditional processes.

We elaborate on our analysis in the body of this report. The outputs of our work are a model, benchmark data and some cost estimates. For example, we estimate that currently, it is possible to reduce semiconductor costs to 2.8¢ for a 1 mm x 1 mm RFID chip using a 0.25 µm process with 25 mask, 3 metal and 2 poly layers – a process fairly representative of implementations of the current Auto-ID specification for a UHF IC. Further process innovations may allow us to push the costs lower – a 20 mask, 2 metal process would allow us to push the silicon cost of a 1 mm die below 1¢. A die which is 0.5 mm x 0.5 mm would be proportionally cheaper.

For the assembly portion, assuming antenna costs can be pushed as low as 1¢, it seems possible to assemble the tag for 3.3¢ at very high volumes using a traditional assembly process and at 2.08¢ if we harness innovations in flip-chip manufacturing processes. **Overall tag costs (silicon + assembly) could be brought as low as 4.35¢ using a traditional assembly process and 3.31¢ using innovative flip chip manufacturing processes.**

In our analysis, we assume 300,000 wafer starts per year or 30 billion die starts per year with 100,000 dies/wafer, and an equipment depreciation lifetime of 5 years. If the number of wafer starts for RFID manufacturing at a particular facility is increased to 3,000,000 per year, silicon costs can be brought down to well under 1¢. If the number of wafer starts is decreased to 30,000 wafer starts per year, the silicon cost rises to 6.1¢ per die. In other words, volume matters, as we will show, but the volumes at which scale can be achieved are not astronomical in relation to world-wide fab capacities, as we describe below.

1.3. Capacity and Volume: Some Editorial Comments

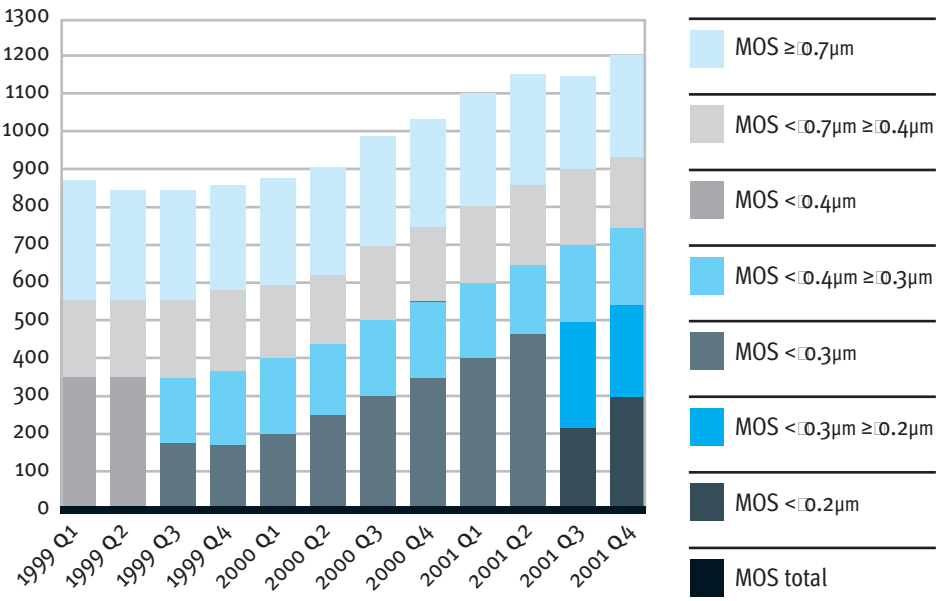
The total worldwide IC manufacturing capacity today is more than 50,000,000 wafer starts per year, and fab capacity utilization for MOS IC's is around 65%. This is shown in Figure 2.

Figure 2: IC Wafer Capacity

Note: All data in the graph are expressed in 8 inch equivalent wafers. The line "Total IC's" in the table includes the "Bipolar" data, which were converted for this purpose from 5 inch to 8 inch equivalent wafers by using the factor 0.391.

Source: SIA/SICAS, http://www.semichips.org/stats/xls/capq2_2001.xls

IC WAFER – FAB CAPACITY IN WAFER STARTS PER WEEK X 1000



8 inch wafers in MOS TOTAL	
BIPOLAR	(5 inch equivalents)
Total IC's	**(8 inch equivalents)**

A question that has been asked recently is whether there is world-wide capacity today to make RFID tags in volumes equal to the demand of the retail industry. Clearly, this is a theoretical question. However, a simple thought experiment helps estimate the answer. Today, 5 billion bar codes are scanned daily according to the EAN.UCC. Let us say that 20% of these items have RFID tags in 2004. Our annual demand, then, is 400 billion IC's a year. (It is unlikely that the other components of the tag, like the antenna, will prove the bottleneck in production.) Let us also say that we can make 100,000 dies per wafer. This implies 4 million wafer starts per year dedicated to world-wide RFID production. This is 20% of world-wide fab capacity, and in today's economy, only slightly higher than the idle capacity of capacity. Should RFID really "take-off," we submit that IC manufacturing capacities will readily scale, and importantly, more and more depreciated equipment can be absorbed into RFID manufacturing, providing a secondary boost to the low-cost dream. The real challenge will be one of road-map management. It is important for the principal users of RFID tags to articulate their needs to the semiconductor and RFID tag industries, and to adhere to these estimates in a responsible and predictable way. This will give manufacturers the confidence to invest in capacity in advance of the need for the capacity, and facilitate a smooth transition into the future. In fact we speculate that the semiconductor industry craves the type of steady production that retail can provide, and with enough confidence, will be happy to cooperate in this industry [17]. In the absence of this pipe-line or road-map management, efficiencies will be lost, and more importantly, we run the risk of what is today an easily avoided speculative bubble.

1.4. A Caveat

It needs to be stressed that because RFID manufacturing is a fragmented and poorly documented industry, and because of commercial impediments to acquiring reliable data, our analysis is very much speculative. We have in essence reconstructed, to the best of our ability, the costs likely faced by RFID manufacturers. The more lasting contribution of our work may well be the model we have developed, which companies may be able to use with their own, more reliable models. We also hope that this model will be improved over time.

2. UNDERSTANDING PASSIVE RFID DEVICES

An RFID tag consists of an RFID chip, an antenna and tag packaging. The RFID circuitry itself consists of an RF front-end, some basic signal processing portions, logic circuitry to implement the algorithms required and EEPROM for storage.

The RFID chip is an integrated circuit implemented in silicon. The RF front-end portion of the chip typically consists of a simple circuit like a resistor-inductor circuit. RFID tags for low-cost, high-volume applications function in the ISM bands at 13.56 MHz and 915 MHz. Ultra high frequency systems like those which operate in the 868–930 MHz range and in the 2.4 GHz range are better suited for line of sight and long range applications. High frequency systems have better propagation characteristics, but poorer range in clear air. Pallets, for example, may use UHF tags, but a box of tomatoes may be better served by a HF tag.

The front-end circuitry impacts the semiconductor process by requiring a process that allows for mixed mode fabrication.

Figure 3

RFID CIRCUIT BLOCK DIAGRAM

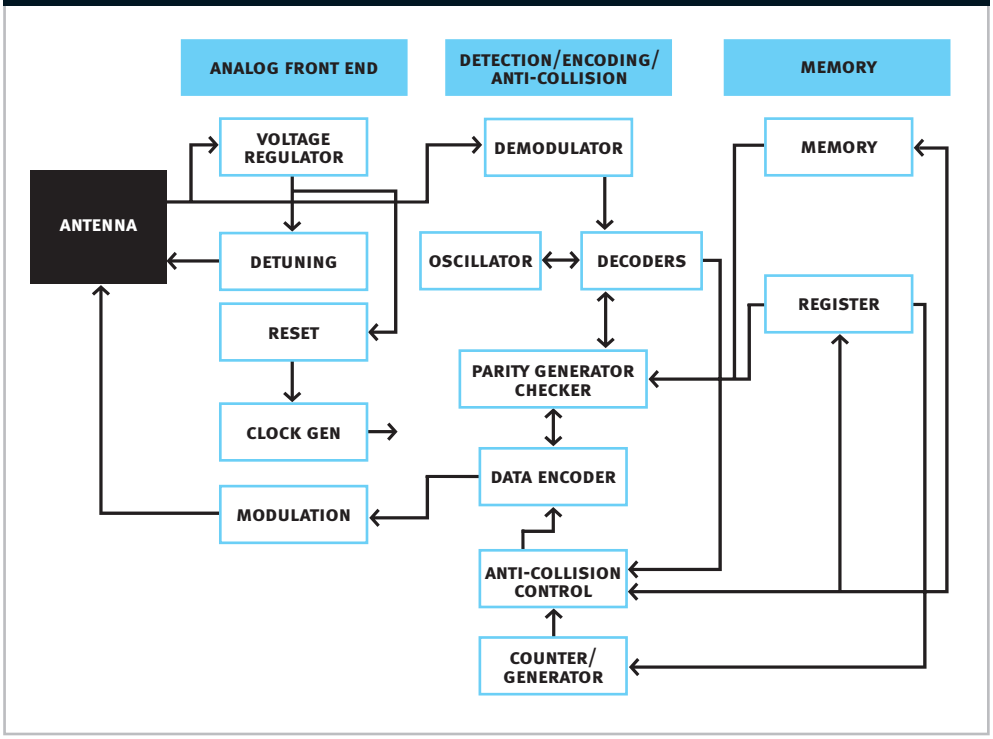


Figure 3 describes a block diagram for RFID IC circuits and lists many of its associated function blocks. The RF front end is connected to the antenna. Typically, at UHF, an electric dipole antenna is used. HF tags use a coil antenna. Passive RF tags have no power source and rely on the signal from the reader to power up. Thus the RF front-end implements modulators, voltage regulators, resets and connections to external antenna.

RFID chips have control logic that typically consists of a few thousand gates. The lowest level Auto-ID chip uses very few gates, in the order of 1500 gate equivalents. Functions in the logic include the error and parity/CRC checkers, data encoders, anti-collision algorithms, controllers, command decoders and so on. More complex RFID chips may include security primitives and even tamper-proofing hardware. The size of the circuit affects the number of mask, metal and poly layers required in the semiconductor process. RFID systems usually use CMOS [8].

A certain amount of information is stored on-chip in an electrically erasable and programmable read only memory (EEPROM). The size of this EEPROM increases as more information is required to be on the RFID chip. The Auto-ID RFID chip specification only requires a 96-bit EEPROM but, for example, the Microchip 450 RFID chip uses a 1024-bit EEPROM. The size of the required EEPROM is a factor in determining the number of mask, metal and poly layers required in the semiconductor fabrication process. It is also a factor in the size of the final semiconductor die. Silicon cost is directly proportional to both the die size and the number of mask, poly and metal layers. For example, in order to fabricate the Fairchild semiconductor FM24C16 EEPROM, which is a 16K memory, a 14 mask, 1 metal, 2 poly layer CMOS process is required [18]. It is possible to trade-off die size against the complexity of the lithography process, but either way, costs are reduced by minimizing the EEPROM requirements on the IC.

The IC in an RFID tag must be attached to an antenna to operate. The antenna captures and transmits signals to and from the reader. The coupling from the reader to the tag provides both the transmission data and the power to operate the passive RFID tag. Typically antennae for passive RFID systems can be either simple dipoles 915 MHz RFID tags or more complex coiled shapes for 13.56MHz systems. Currently, antennae are made of metals or metal pastes, and typically cost as much as 12¢ per antenna to manufacture. However new methods that range from conductive inks and new antenna deposition and stamping techniques are expected to reduce costs below 1¢.

The RFID antenna needs to be electrically and physically connected to the RFID chip. This can be done in a number of ways ranging from wire-bonding to flip-chip. The entire system must then be converted to the packaged form.

3. UNDERSTANDING THE MANUFACTURING PROCESS

The tag manufacturing process has two major components: the semiconductor manufacture and the tag assembly.

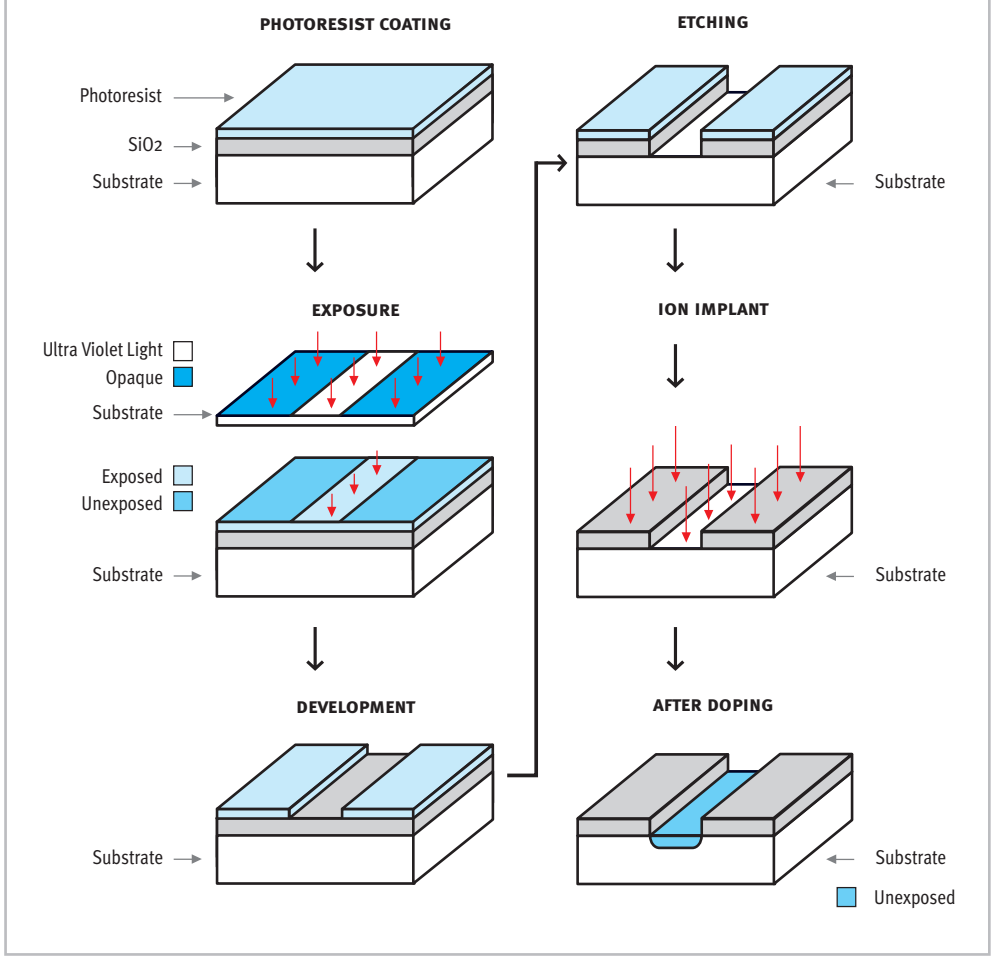
3.1. Semiconductor Manufacture

Typical CMOS semiconductor manufacturing has mask, metal and poly layers. The mask layers are fabricated using photolithography. Basic CMOS features are formed by first growing silicon dioxide on the silicon substrate through an oxidation process. This involves heating the silicon in an oxidizing atmosphere such as water vapor. The silicon dioxide layer is then covered with a photo-resist coating. This coating is exposed through a mask to UV radiation and then the photo-resist layer is etched away. The etching

leaves a patterned silicon surface. After etching, the wafer is exposed to ion implantation with the patterned silicon dioxide acting as an implantation mask. Finally, the implantation is driven deep into the substrate using a thermal cycle. These steps translate to many sub-steps and machines. The basic process is repeated several times with in different combinations, and with different masks, to create complex circuits. Figure 4 illustrates the basic silicon lithography process.

Figure 4

BASIC SEMICONDUCTOR LITHOGRAPHY

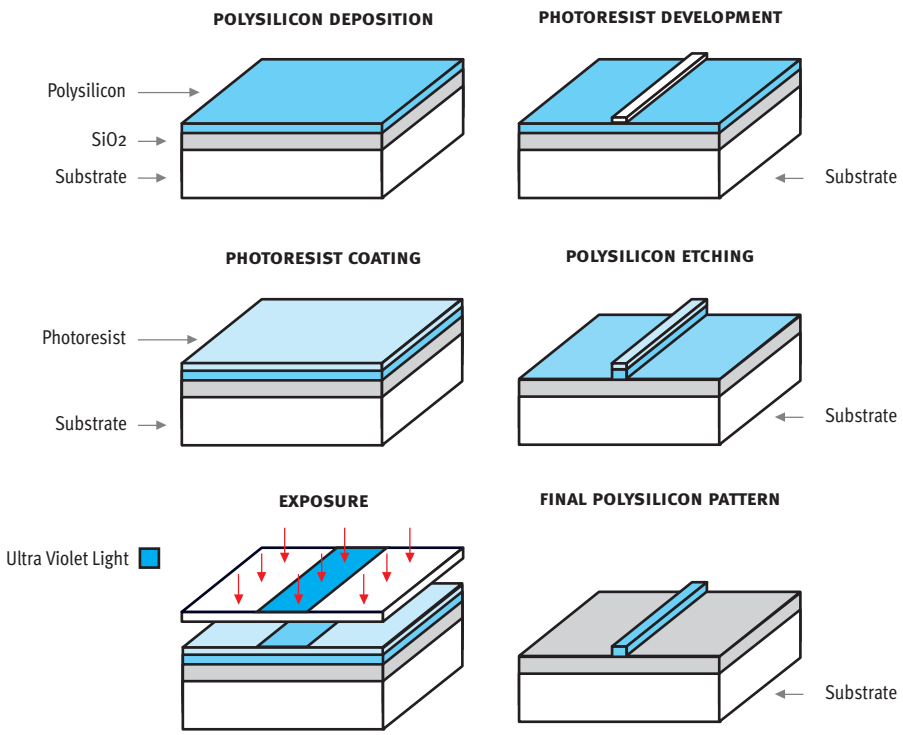


Metal layers are the most expensive to create and involve the most steps. Metal is deposited after creating a silicon dioxide layer that is exposed and etched to reveal contact points. Highly conductive metals like aluminum are usually preferred. Metal layers are created using physical vapor deposition (PVD).

Polysilicon layers are created using a chemical vapor deposition (CVD) process to deposit gate polysilicon on top of the silicon dioxide layer. Subsequently, a similar process consisting of photoresists, masks, UV radiation, etches and cleanings create a polysilicon feature. All MOSFET gates are usually defined in one or two steps. Figure 5 illustrates the steps to create a polysilicon feature on a semiconductor wafer.

Figure 5

STEPS TO CREATE A POLYSILICON FEATURE



The following steps are repeated in the appropriate process sequence until the silicon die is ready:

- **Oxidize:** Furnace oxidation, etc.
- **Expose:** Expose implant, gate, line, contact/pad etc.
- **Measure:** Measure overlay, film, CD etc.
- **Etch:** Etch gate, metal, via.
- **Clean:** Clean metal, oxide, etc.
- **Strip:** Strip film etc.
- **Vapor deposition:** chemical or physical vapor deposition of poly or metal.

Figure 6: Mask Steps 250_a1_82 Semconductor Process Steps

Figure 6 lists some sample steps from the SEMATECH 250_A1_82 logic/memory process.

PROCESS DESCRIPTION	TOOL_TYPE
Expose_Implant	Litho_Iw
Meas_Overlay	Meas_Overlay
Inspect_PLY	Insp_PLY
Meas_CD	Meas_CD
Implant	Implant_HiE
Implant	Implant_HiE
Implant	Implant_LoE
Plasma_Strip	Dry_Strip(I)
Clean_Post_Strip	Wet_Bench(I)

Once the semiconductor wafer has been processed, the next sequence in the process is assembly. Tag assembly consists of a sequence of the following 4–5 process stages:

The first step is the thinning the wafer to reduce its profile and remove excess silicon. Typically a chemical-mechanical polishing technique is used. A conditioner and special scrubbing pads are used in this process. Rates can be low, but because each wafer in RFID may have tens of thousands of dies, the effective per-die rate is quite. For example, a Strasbaugh 6EGCMP wafer thinning machine that can handle 10 wafers an hour, which translates to an equivalent of about a million dies an hour, or 1.2 billion tags a year.

Once the wafer is thinned, the next step is dicing the wafer to create dies. Dicing can be done using a specialized saw but it is also possible to dice using a chemical dicing process. The latter process, though more space efficient, is as yet immature, but certainly the preferable approach for the future. We will concentrate on conventional dicing. For example, a Kulicke and Soffa 7100 dicing machine can process 350 mm/sec. Sometimes an additional step may be implemented before dicing. For example, in the flip-chip process, another process "bumps" the wafer before dicing it. Returning to throughput for these machines, consider a wafer with 20,000 dies of 1 mm each. The total cutting length required is 40,000 mm/wafer, which gives us a throughput of 40 wafers an hour. In other words, a dicing machine has greater throughput from a die-equivalent point-of-view than a polishing machine. Line balancing is therefore an important task in cost estimation.

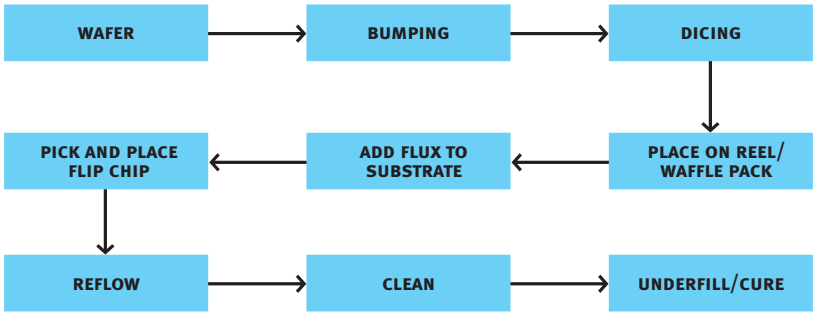
When the dies are ready, the next stage is attaching the die to the antenna and packaging it to create a complete tag. Most of the costs reside in this stage. There are three primary methods that can be used for the assembly:

- **Traditional assembly:** In traditional assembly, the die is brought into position either by reeling it in or loading it into waffle packs. It is placed using a pick and place robot. Next, the die is attached to the packaging typically using a die-attach machine. The attach process uses an adhesive to attach the die to the packaging and the assembly is cured. Once the die is in position, the pads are connected using wire bonding, which is a solid phase welding process involving pads and wires. Either heat or ultrasonic energy is used to complete the bond.

- **Flip chip:** Flip chip assembly is an alternative in which the chip is assembled directly onto the board or tag package. Figure 7 illustrates the steps in a typical flip-chip line.

Figure 7

FLIP CHIP ASSEMBLY PROCESS STEPS



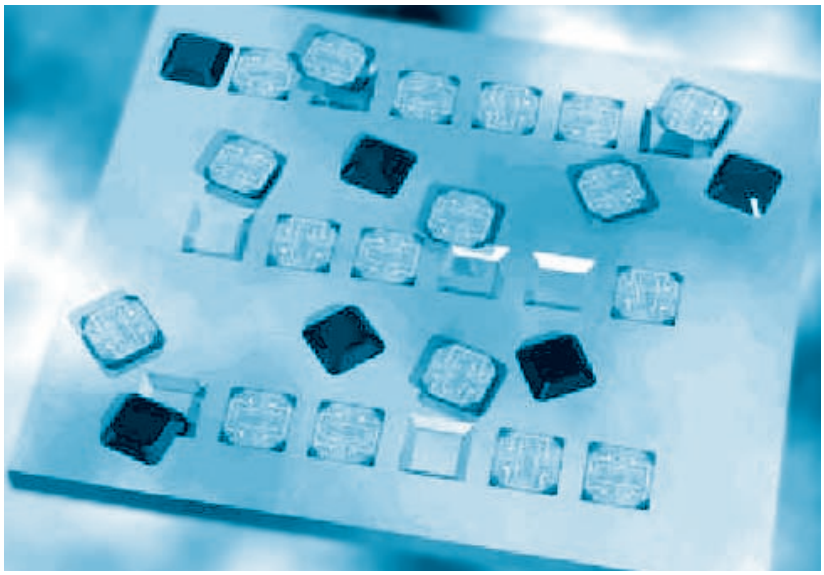
Pads are connected using "bumps" of conductive material such as solder, aluminum or gold. In the flip chip process, the wafer arriving from the fab is first "bumped" to leave a solder bump on top of each pad. After the wafer is bumped, it is then diced and the bumped dies are loaded onto a reel or waffle pack for assembly. Assembly is done using a pick-and-place robot that positions the bumped dies directly on the board or package substrate. For an RFID tag, the die is placed directly on the antenna inlet. The package is compressed and cured to complete the process. The figure below describes the flip-chip process. Sometimes an under-fill epoxy layer is also used between the die and the substrate to support and separate the die from the substrate.

- **Statistical assembly:** We refer to a class of processes which use phenomena like fluid flows and vibratory fields as statistical assembly. The idea is that these processes will never be 100% accurate, but are extremely scalable with low variable costs.

  - FLUIDIC SELF-ASSEMBLY
    Fluidic self-assembly is a new technique for RFID tag assembly. In fluidic self-assembly, the wafer is diced through chemical etching into differently shaped units called nanoblocks. These nanoblock dies have a three dimensional shape. The tag/assembly substrate itself indentations that match the shape of the nanoblock dies. Next the separated dies are suspended in a fluid and flowed across the substrate, where the dies "drop" into the substrate "holes". In Figure 8 We see a pictorial of the nanoblock dies attaching into the substrate holes. Finally the blocks are connected using standard metalization to connect to the pads. [Ref 10]

  - VIBRATORY ASSEMBLY
    In an earlier paper, we speculated on the applicability of vibration to RFID assembly. Recently, Philips Semiconductor stated that their analysis too confirmed the applicability of this process to low cost tag production.

Figure 8: Fluidic Self Assembly of Nanoblocks



The final stage in any process is testing the completed tag to ensure that it functions. This is different from in-wafer testing, which is performed on the complete wafer to ensure functionality of individual dies. RFID tags can be tested using a specialized RFIC test system such as the Advantest T76 series. Basic logical testing, however, can be performed extremely inexpensively on the conversion line.

4. THE SIMULATION MODEL

We modeled semiconductor and assembly processes with the purpose of estimating the cost per tag. The benchmark consisted of interviewing engineers and profiling more than 130 machines that are used in the tag assembly process. The most important elements of the equipment benchmark were throughput, equipment fixed and variable costs, raw material cost, labor and overhead costs, maintenance and replacement costs, utility costs and equipment yields or efficiencies.

The operating unit throughput per machine was a key parameter for benchmarking. This parameter captures the number of units processed in one hour (UPH) and it is different from the spec sheet value because it takes into account the operating efficiency of the machine.

The fixed cost or capital investment of the machine was another critical driver of overall cost. Typically we depreciated equipment over a 5-year schedule using a straight-line depreciation model. The 5-year depreciation model is standard in the rapidly evolving semiconductor industry.

Other costs include individual raw materials costs for materials or chemicals such as compressed air, lubricants, materials such as silicon or antenna inlets, aluminum, gold, distilled water, epoxy, pads, photoresist and etchers. These material costs also added a significant amount of the final tag cost. Variables specific to the semiconductor process such as mask costs were included as well. Finally, an important material variable was antenna inlet cost.

The majority of labor costs were estimated on a per-machine basis in terms of labor required to operate a given machine. However, a small labor overhead consisting of facilities, and of administrative and management overhead was also factored into our model. Yearly maintenance and part replacement costs were factored in as a percentage of total capital costs. Utilities such as water, electricity and floor space were factored in as inputs to our model. It turns out that their impact on the cost is minimal. We also considered individual equipment yield and efficiency numbers in our model. Assembly equipment yields are typically high and yields of 95% or more are industry-accepted.

Once all the stages of process to be costed were determined, the cost was computed based on the equipment associated with each stage of the process. Every time a line is stopped and the product changed, a fixed cost penalty is incurred, called the reset cost. Currently we do not factor in reset losses but assume that the process is run continuously.

We used two types of process runs in our model; a line maximized run and fixed machine-count run. In a line maximized process run, we scaled the number of machines at each stage to balance the line. The number of machines was adjusted to ensure that a maximum number of units were pushed through at each stage of the process. We ensured that the cost per die was minimized by pushing this maximum throughput at each stage.

In a fixed machine process run, a fixed number of machines were used per stage of the process. Costs estimated using this method were obviously higher than for a line maximized run. This number is useful, however, because line balancing assumes larger volumes. Smaller manufacturing operations may not have that luxury, and the fixed machine run may be more representative of initial costs.
The number of wafer or die starts was an input for line maximized simulation runs. Other inputs include the depreciation schedule and the size of each die.

Figure 9 is a snapshot of the assembly cost model. This snapshot shows some of the input parameters in the model. For the semiconductor process we used the number of mask, poly and metal layers as an input and generated a “pseudo” process of all the required equipment. This process was generated automatically by concatenating individual steps required per mask, metal or poly layer. No process optimization beyond

this was assumed. We assume that by using process optimization, we may be able to push the costs lower. Once a process was generated, it was costed to estimate a per-die cost. Figure 10 is a snapshot of the semiconductor cost model. This snapshot shows some of the process steps and associated variables.

Figure 9: Assembly Process Costs
Machine Specs and Costs.

Machine Specs & Costs

Capital Units	Machine Use 0 or 1	Process	Throughtpu Unit/Hr	Pipeline Tput Die/Hr	Used Tput Die/Hr	Utilizatio Hr/Day	Active Life Yr	Yield %	Wattage KW	Floor space Sq Ft	Machine Cost $	Maintainence cost $/Yr	Total Cost $/Yr
Machine/ Process 1	1	Thinning	10	1130400	1130400	16	5	97%	20	100	$425,000	$5,000	**$101,923.4**
Machine/Pr Process 2	1	Dicing	6	678240	678240	16	5	97%	20	21	$300,000	$5,000	**$72,164.0**
Machine/ Process 4	0	Traditional Assembly	3750	3750	NA	16	5	97%	20	200	$935,000	$5,000	**$216,983.4**
Machine/ Process 5	1	Flip Chip Assembly	10000	10000	10000	16	5	98%	20	150	$1,200,000	$5,000	**$273,853.4**
Machine/ Process 7	1	Tag Test	7200	7200	7200	16	5	97%	20	55	$140,000	$5,000	**$37,936.4**
etc													

Raw Material Cost

Raw Material Units	Air $/L	Distilled Water $/L	Nitrogen $/L	Aluminum $/lb	Nickel $/lb	Gold $/lb	Non-conductive/Underfill epoxy $/lb	Other Raw Materials $/Unit	Wafer $/Unit	Antenna Inlets $/Unit	Thinning Pads $/Unit	Thinning Conditioners $/Unit	Bumping cost $/Wafer
	0.003	0.0035337	0.03	0.64	2.88	3432	3	0.0035	0	0.01	270	600	85

Labor Cost

Labor Units	Operator $/Hr	Supervisor $/Hr	Engineer $/Hr	Technical $/Hr	Overhead $/Hr	Management $/Hr
	15	22	62.5	18	20.8	78

Pipeline Thpt(die)	**7200**
Wafer/Die Ratio	**113040**

63,072,000

Utilities Cost

Utilities Units	Water $/L	Power $/KWH	Floor Space $/Sq Ft/Yr	FS Overhead %
	0.01	0.18	20	30%

Figure 10: Sample Process Tool & Mask Steps

†($/pa), *($/pa)

STEP #	PROCESS DESCRIPTION	TOOL TYPE	MASK TYPE	WAFERS/ HOURS	INDIRECT MATERIAL†	DIRECT MATERIAL*	ACTUAL CT (HOURS)
1	Clean_Pre_OxAn	Wet_Bench(I)		125	0.5		1.393263889
2	Oxidation_Sac	Furn_FastRmp		50	0.6		10.41560185
3	Meas_Film	Meas_Film		200	0.0		0.483333333
4	LPCVD_Nitride	Furn_Nitr		30	0.6		14.27951389
5	Meas_Film	Meas_Film		200	0.0		0.483333333
6	Expose_AA	Litho_I	I_Mask	30	0.8	0.70	6.055173611
7	Inspect_PLY	Insp_PLY		200	0.0		0.903689236
8	Meas_CD	Meas_CD		200	0.0		0.903689236
9	Etch_AA	Dry_Etch		25	1.5		4.683229167
10	Plasma_Strip	Dry_Strip(I)		80	0.0		1.557967836
11	Clean_03	VP_HF_Clean		40	0.3		1.283395062
12	Clean_Post_Strip	Wet_Bench(I)		125	0.5		1.393263889
13	Inspect_PLY	Insp_PLY		200	0.0		0.903689236
14	Meas_CD	Meas_CD		200	0.0		0.903689236

Figure 11 is a snapshot of the semiconductor cost model that shows the inputs to the semiconductor costing process. The 250_A1_82 process from SEMATECH was used as a baseline semiconductor process. This is a 0.25 micron process and employs 283 steps. The 250_A1-82 process is used in UC Berkeley ESRC models and we used the equipment benchmarks for this process to cost our semiconductor process. The traditional and flip-chip assembly processes were based on industry standard definitions and interviews.

Figure 11: Input to Cost Model

	Input	Comment	Value					
	Mask Layers		25				Create New Process	
	Metal Layers		3					
	Poly Layers		2					
	Base calculation number dies		50000					
	Number of dies per wafer		114,182				Clear	
	Feature Size in mm		1					
	Total cost per wafer		1321.61					
	Total cost per die		0.01157462					
	Worldwide fab capacity		66,560,000					
	Wafer starts		300,000					
	Utilization		0.45%					
		Sensitivity						
	Poly 1							
		Metal						
	$0.01157462	1	2	3	4	5	6	
Mask	7	0.007118275						
	8	0.007235116						
	10	0.00746513	0.008581733					
	15	0.008039686	0.009164546	0.010289017	0.011411	0.012532		
	20	0.008629255	0.009748212	0.010873598	0.011991	0.013123	0.014244	
	25	0.009209519	0.010328784	0.011453179	0.012579	0.013702	0.01482	
	Mask 25							
		Metal						
	$0.01157462	1	2	3	4	5	6	
Poly	2	0.009338769	0.010454867	0.01157462	0.012709	0.013826	0.014953	
	3	0.00946726	0.010581907	0.011709574	0.012834	0.013958		
	5					0.014217		
	8					0.014606		
	10					0.014863		
	14,1,2	0.008052498						

5. RESULTS

Assuming 300,000 wafer starts per year and 25 mask, 3 metal, 2 poly semiconductor process, it appeared that overall RFID tag costs could be pushed as low as 4.49¢ using a traditional assembly process and 3.31¢ using a flip chip process. The semiconductor or die costs accounts for 1.15¢ and the remaining 2–3¢ are tag assembly costs.

300,000 wafer starts per year translates to around 30 billion die starts per year. This wafer start number accounts for only 0.45% of worldwide semiconductor production. The total worldwide IC fab capacity is 66,000,000 wafer starts per year and currently fabs are severely underutilized. Current fab capacity utilization for MOS IC's is around 65% [16]. If the number of wafer starts is increased to 3,000,000, then the die cost drops to 0.8¢ per die.

Today, we find that it is possible to push semiconductor costs as low as 1.28¢ for a 1 mm x 1 mm square die using a .25 micron process with 25 mask, 3 metal and 2 poly layers. We found companies that had successfully implemented the Auto-ID standard in silicon using a 25 mask, 3 metal and 2 poly layer process. Further innovations may allow us to push the costs lower – thus a 20 mask, 2 metal process would allow us to push the silicon cost below 1C. For the assembly portion, assuming antenna costs can be pushed as low as 1¢, it is possible to assemble the tag for 3.3¢ at very high volumes using a traditional assembly process and 2.08¢ using an innovative flip-chip manufacturing process. If the number of wafer starts is increased by a factor of 10 to a total of 3 million wafer starts per year, the silicon costs can be brought to under 1¢ as well.

In Figure 12 we show the variations in silicon die cost with mask layers. We assume 1 metal and 1 poly layer.

Figure 12: # Mask Layers Vs. Die Cost (1 Metal, 1 Poly)

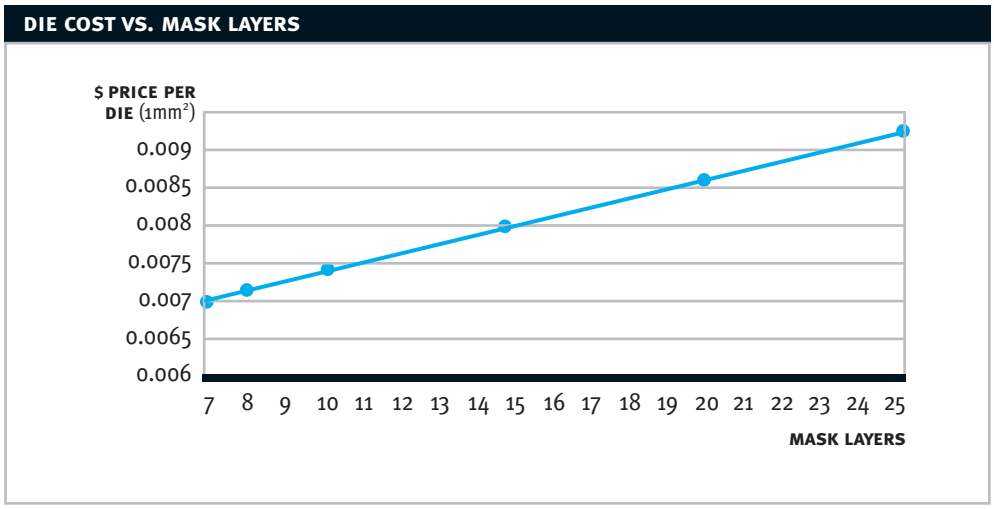


Figure 13 shows the variation silicon die costs with poly layers. We assume 25 mask and 5 metal layers for this case.

Figure 13: Poly Layers Vs. Die Cost (25 Mask, 5 Metal).

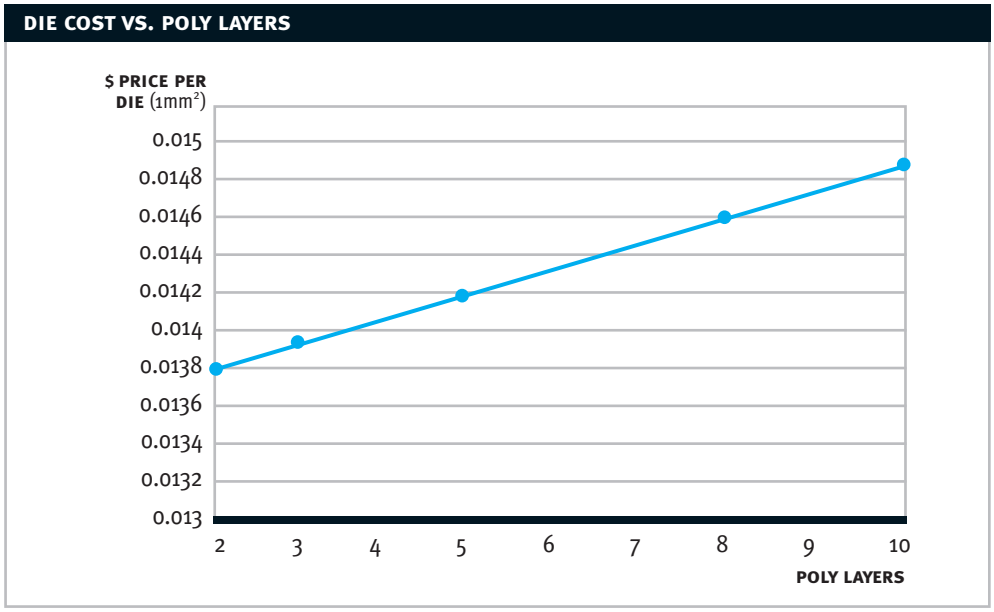
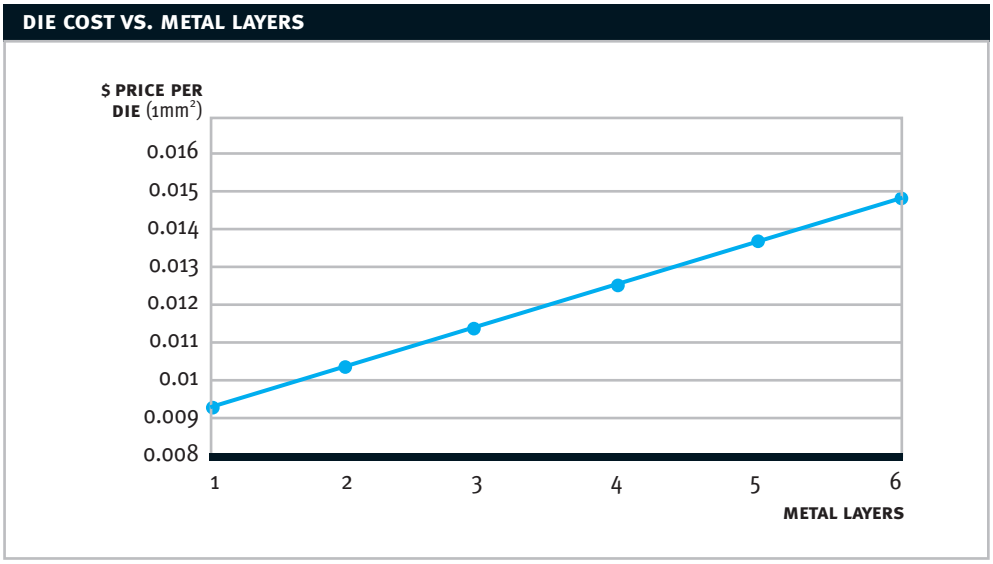


Figure 14 shows variation in silicon die cost with metal layers. We assume 25 mask and 2 poly layers in this case. The silicon die costs are most sensitive to metal costs – a change of 1 metal layer can cause a 10 % change in cost, but it requires 8–10 poly or mask layer increases to get the same effect.

Figure 14: Metal Layers Vs. Die Cost (2 Poly, 25 Mask).



In Figure 15 and Figure 16, we show cumulative tag costs by different stages in the process for traditional and flip-chip assembly. Traditional assembly is by far the most expensive step.

Figure 15: Assembly Costs

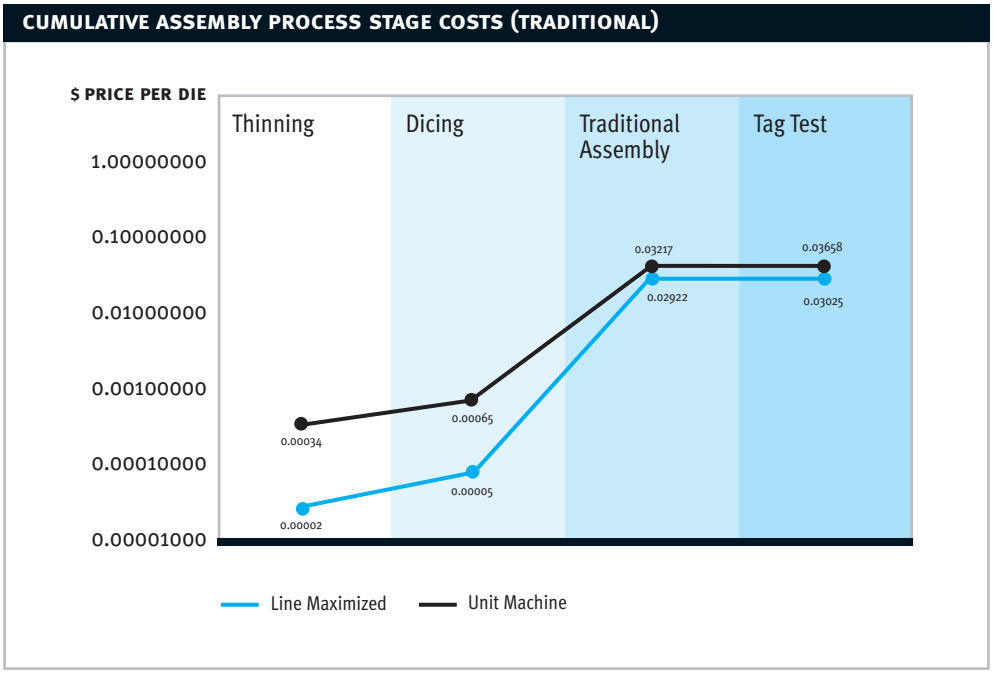
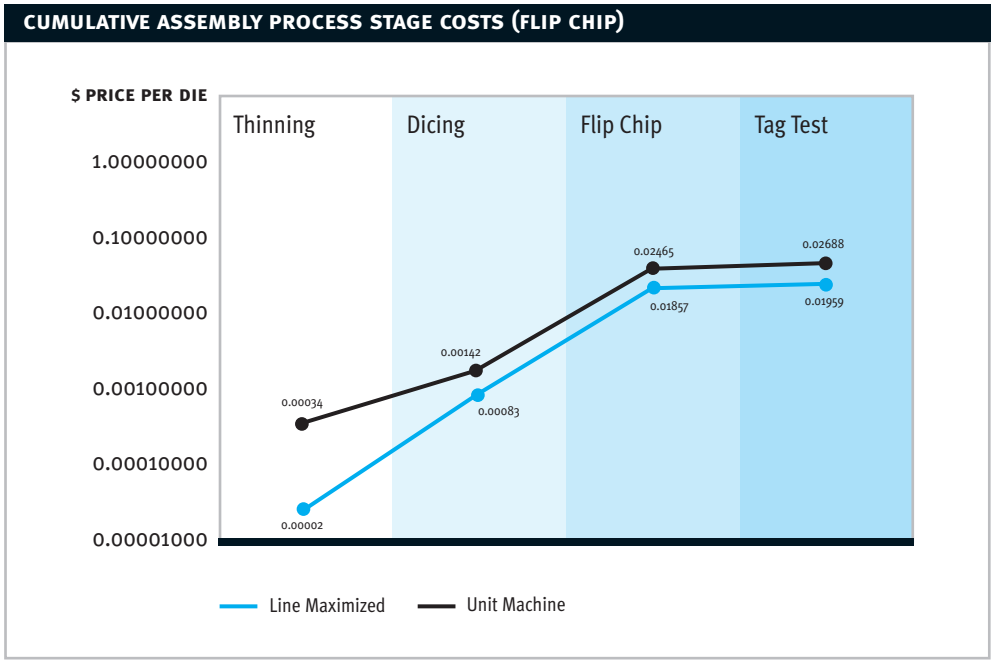


Figure 16: Assembly Costs



In Figure 17 we show the volume or throughput by assembly stage through the assembly process when 3.3 million tags are input into the assembly process.

Figure 18 shows the breakdown of cost by different stages for the flip-chip assembly.

Figure 17: Throughput by Stage

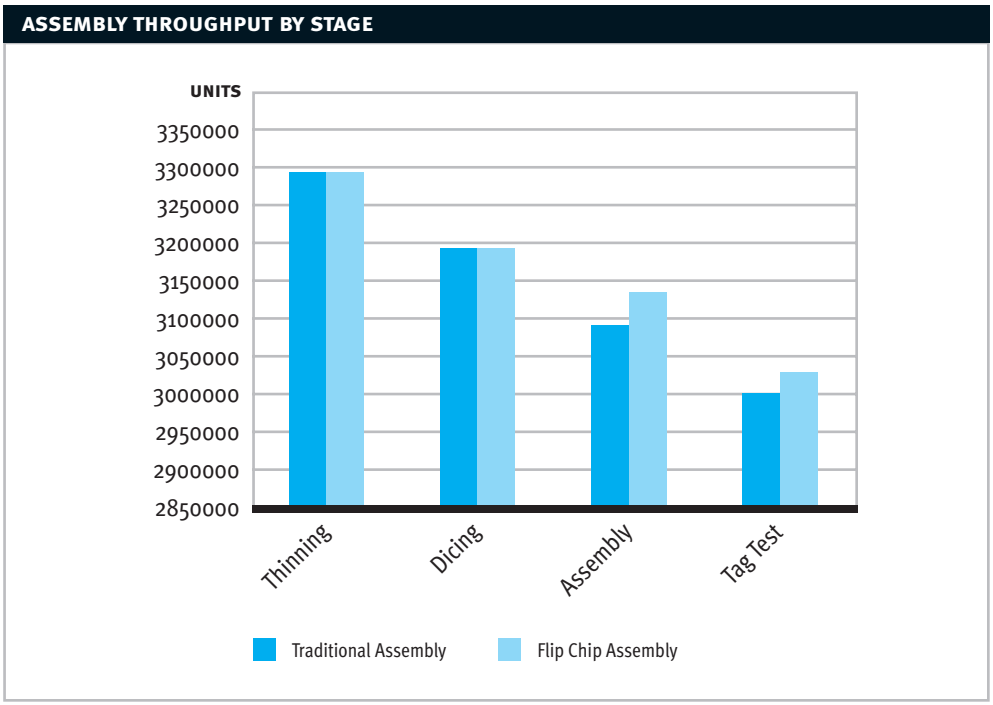
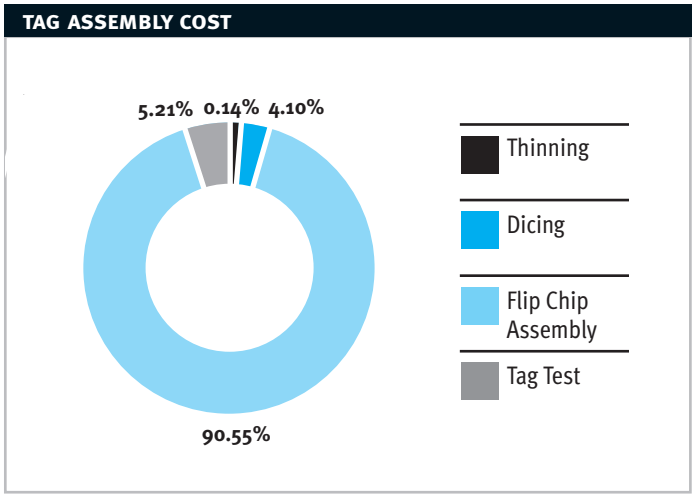


Figure 18



We find that line balancing and throughput improvements are the key drivers on the assembly side of tag manufacturing. Throughput in flip-chip manufacturing, for example, is very dependent on the time it takes to cure the polymers involved. Reducing this time greatly reduces the cost of operation of flip-chip machines, and also has a knock-on effect on the rest of the process – by making it possible to balance the rest of the line, and better using other machines in the line. Our model can be used to perform sensitivity analysis on a number of such variables, and will help focus on the most critical processes and performance metrics for future development.

6. CONCLUSIONS

We have developed a model for costing RFID tags which is similar to the approach used in the semiconductor industry. We speculate that it is indeed possible to achieve a 5¢/tag cost number at a sufficiently high volume of tags using even **existing** technology. The volume required to reach this cost metric is well within the reach of current fab capacities. Process innovations and improvements that drive down antenna costs will also significantly impact the cost per tag. These innovations are connected to each other. For example, lower powered dies will reduce the conductivity required of the antenna, enabling even lower cost printed antennas. In other words, aggressive thinking and innovations in RFID tag manufacturing will reveal numerous synergies which can play off each other in the coming years, providing additional cost reductions. Unfortunately, the industry today seems trapped in "catalog mode" where engineers are forced to pick inappropriate machines from catalogs rather than inventing solutions to critical problems. Volumes, roadmaps and, most importantly, orders will surely unleash a new cycle of much-needed innovation. This is a win-win for all parties.

7. ACKNOWLEDGEMENTS

The authors want to acknowledge the machine benchmark carried out by John Bloomsburg at MIT and the MIT UROP program, which funded the creation of the benchmark. We particularly thank Jim Clayton for his advice. Several engineers from manufacturing and design companies volunteered time and information. We are indebted to them.

8. BIBLIOGRAPHY

Our work is based on a great number of interviews and publications. Only a few of the reference sources listed below are specifically cited in the text for reasons ranging from confidentiality to clarity.

1. **S. Sarma, "Towards the 5¢ Tag".**
   Auto ID White Paper MIT-AUTOID-WH-006, 2001.

2. **N. Weste & K. Eshraghian, "Principles of CMOS VLSI design".**
   Addison Wesley, 1994.

3. **J. Rabaey, "Digital Integrated Circuits".**
   Prentice Hall, 1995.

4. **R. Leachman, J. Plummer & N. Sato-Misawa, "Understanding fab economics".**
   Competitive Semiconductor Manufacturing, University of California, Berkeley, 1999.

5. **Leachman & Hodges, "Berkeley Semiconductor Manufacturing".**
   IEEE Transactions on Semiconductor Manufacturing, May 1996.

6. **J. Bloomsburg, "RFID Tag Manufacturing".**
   MIT UROP, 2002.

7. **R. Wright, "Cost Resource Model Detail".**
   Economic Model Workshop, International Sematech, 2001.

8. **K. Finkenzeller & J. Wiley, "RFID Handbook".**
   2000.

9. **Sematech International Consortium.**
   www.sematech.org, 2002.

10. **"Fluidic Self-Assembly".**
    White Paper, Alien Technology Corporation, 1999.

11. **International Technology Roadmap for Semiconductors.**
    SIA, 2001.

12. **"A Comparison of High Volume Costs for RFID IC's Using Wire Bond and Flip Chip Technology".**
    Alien Technology Corporation, 2001.

13. **J. Clayton, "Silver Filled Polymer Flip Chip Assembly".**
    Polymer Flip Chip Corporation, IMAPS 2002.

14. **G. Levinson, Kulicke & Soffa, "Principles of Dicing".**

15. **"Metals Market Sentiment".**
    PriceWaterhouseCoopers 2002.

16. **"Worldwide IC Capacity Trends".**
    IC Insight Inc., Scottsdale, AZ 2001.

17. **"IC fab capacity shrinks as chipmakers close plants".**
Semiconductor Business News www.semibiznews.com/story/OEG20020319500035.

18. **Fairchild Semiconductor Manufacturing Corp, EEPROM Qualifying Process.**
Advanced Semiconductor Manufacturing Corp of Shangai, 2001.

19. **Kulicke & Soffa, "Flip Chip Technology".**
Flip Chip Division, 2001.

20. **"Semiconductor Equipment And Materials".**
SEMI, www.semi.org, 2002.

21. **Fairchild Semiconductor Spec Sheet FM24C16.**
2002.

22. **Atmel Corporation Product Spec Sheets, AT88RF001, AT88RF0202, AT88RF256-12, ATRF25613, ATRF25613b, ATRFT25613EK.**

23. **Holtek Product Spec Sheets 6720.**

24. **Microchip Product Spec Sheets MCRF200, MCRF250, MCRF355, MCRF450, MCRFFAN680.**

25. **Taiwan Semiconductor Corporation.**
www.tsmc.com. 2002.

26. **Advantest Product Spec Sheets, T7611.**

27. **ASM Pacific Product Spec Sheets AB356, AB520, AB559A, AD339Eagle, AD829A, AD8912, AD898, AD900.**

28. **Datacon Product Spec Sheets, 2200apm, 2200apm+.**

29. **Delta Design Product Spec Sheets, 1688,1888,1888Bowl-to-Tape, 3087 Tri-Temperature, 717 Ambient, 717 Tri-Temperature, Castle EC, Castle Lx Logic, Castle Mx Memory, RFS Handler, Summit Handler.**

30. **EBARA Product Spec Sheets EPO-222.**

31. **ESEC Product Spec Sheets 2008, 2007Hsplus, 2007SSI, 2008 Smart Card, 2008xP, 2008xP3, 2008xSC, Micron 2, Micron 2, Wire Bonder 3088iP, Wire Bonder 3088iP J-Boat, Wire Bonder 3088iP SC.**

32. **Kulicke & Soffa, "Product Spec Sheets 7100, 7300, 7500, 8028, 8060, 8090, 8028PPS, 8028S, BOSS, triton RDA, UCSP1, UCPS2, UCSP50, UCSP65, UCSP75, UCSP80".**

33. **LAM Product Spec Sheets Teres' XD™ Platen, Teres® CMP System.**

34. **Lapmaster Product Spec Sheets Dual-Sided Lapping, Pitch Polishing Machine, Single-Sided Lapping.**

35. **Okamoto Product Spec Sheets GNX-200, GNX-300, SDG60, SPL-12, SPL-120, SPL-15, SPL-24, SPL-500, SPP-4000, SPP-600AT, SPP-900AT, SRG200, TR-350, VG-101, VG-201, VG-201D-200, VG-202MKII, VG-201D-300, VG-502MKII8.**

36. **Shinkawa Product Spec Sheets ACB-400Super, DPS-250, DPS-260, SPA300, SPA310, STC-400, STC-400, UTC-1000, UTC-400BI, UTC-475BISuper, UTC-480BI.**

37. **SpeedFam-IPEC Product Spec Sheets 676, 776, Auriga, AurigaC, Momentum, Momemtum300.**

38. **Strasbaugh Product Spec Sheets 6DS-SP, 6DZ, 6EC CMP, 6EG CMP, 7AA, 7AF.**

39. **Tokyo Electron Product Spec Sheets P-12XL, P-8XL, P-8XLC, WLRAS, WX-8**

40. **Tokyo Seimitsu Product Spec Sheets A-FP-210A, A-PM-50A, A-PM-60, A-WD-10A, A-WD-10A/C, A-WD-110A, A-WD-200T, A-WD-300T, A-WD-5000A, BG200, EM-11A, EM-12A, EM-15A, Em-21, FP200A, UF190A, UF200, UF200FL, UF200S, UF300A**.

41. **Personal Communication Alien Technology.**
2002.

42. **Personal Communication Polymer Flip Chip Corporation.**
2002.

43. **Prof. R. Leachman, "Personal Communication".**
University of California, Berkeley 2002.

44. **Prof. N. Berglund, "Personal Communication".**
U OGI, 2002.

45. **Toray, "Personal Communication".**
2002.

46. **Kulicke, "Personal Communications".**
2002.

47. **Soffa, "Personal Communication".**
2002.

48. **Intel, "Personal Communication".**
2002.

49. **ASM Pacific, "Personal Communication".**
2002.

50. **Advantest, "Personal Communication".**
2002.

50. **Esec, "Personal Communication".**
2002.

51. **Muhlbauer, "Personal Communication".**
2002.