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6.004 Computation Structures Spring 2009

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# MASSACHUSETTS INSTITUTE OF TECHNOLOGY DEPARTMENT OF ELECTRICAL ENGINEERING AND COMPUTER SCIENCE

# **6.004 Computation Structures**

Spring 2009

## **Quiz #1: February 20, 2009**

Name	Athena login	name	Scor	e
Solutions			Avg: 21.4	
	·			
Problem 1 (6 points): Quickies and	Trickies			
(A) You are trying to guess a car	d picked at random from a star Nora tells you it's not an ace; R			
What is the <i>total</i> amount	of information about the card r answer as either a number or	given by Sa		
]	Bits of info (number or formu	ıla):	$\log_2(52)$	2)
(B) Give the four-bit two's comp	plement representation of -6.			
4-bit 2's	complement representation o	f -6:	1010	
(C) Let <i>w</i> be an eight-bit code w distance from <i>w</i> is exact		rds are there	e whose Ha	amming
Number of 8-1	oit code words distance 1 from	n w:	8	
	2 <sup>k</sup> -input XOR could be implen 2 <sup>k</sup> -input, 1-output combination cessarily identical) 2-input 1-ou	al function	be implem	
	C	ircle one:	YES	NO
(E) The propagation delay speci	fied for an inverter is less than	its contami	nation dela	ay
Circle one	e: NEVER SOM	IETIMES	A	LWAYS
	ting of an output node connected PFETs and a single pulldown of lecture), computes <b>F(A, B, C, I</b>	circuit conta		
It is observed that $F(1,0,$	<b>1,1)</b> = <b>1</b> . What can you say ab	out the valu	e of <b>F</b> (1,0	,0,0)?
	(circle one): F(	1.0.0.0) =	1 0 0	an't tell

6.004 Spring 2009 - 1 of 4 - Quiz #1

## Problem 2. (5 points): Variable-length Codes

GradeStore, Inc makes storage devices designed to hold only letter grades issued in college courses. Each grade is one of A, B, C, D, F, or X (for dropped courses), and the grades are distributed according to the following table:

Grade	Probability of occurrence
A	26%
В	34%
C	11%
D	10%
F	8%
X	11%

(A) (1 <sub>1</sub>	point) How	many bits w	ould be red	uired to stor	e each grade	using a fixe	d-length code?
(**) (*)	pomit, 110 "	many ores "	oura oc rec	lanca to stor	e caem grade	asing a min	a rengin coac.

Number of bits: \_\_\_\_\_3

(B) (3 points) Devise a Huffman code to optimize the storage of grades.

The correct Huffman tree is



The specific answers at right are just one of the many possible encodings from this tree.

Encoding for A: \_\_\_\_\_\_

Encoding for B: \_\_\_\_\_\_11

Encoding for D: \_\_\_\_\_\_

Encoding for F: \_\_\_\_\_

Encoding for X: \_\_\_\_\_\_

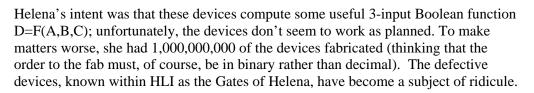
A well-heeled customer wants GradeStore to customize their encoding to include a seventh grade, M, to identify students whose work was incomplete due to their being hit by a meteor. This is a very rare event, and GradeStore expects its probability to be on the order of 0.000000000007%.

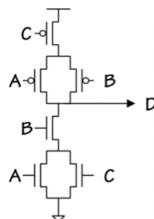
(C) (1 point) How many bits would Huffman encoding allocate to the representation of an M grade?

Bits for encoding of M grade: \_\_\_\_\_4

#### Problem 3. (7 points): Saga of Helena Handbasket

Helena Handbasket, who barely passed 6.004, has been hired to design CMOS gates for Hapless Logic, Inc. Remembering something about PFETs in pullups and NFETs in pulldowns, her first design was a 3-input device whose circuit is shown to the right.





Helena has brought you in as a consultant. Your first task is to figure out how badly Helena blew the design of her 3-input logic device – in particular, whether it drives the output D to a valid logic level for every combination of the inputs A, B, and C.

(A) (2 points) Are there logical (0/1) values of A, B, and C for which D is not driven at all? If so, give values for A, B, and C that leave D undriven; else write NONE.

A, B, C values for undriven D, or "NONE": 
$$B = 0$$
 and  $C = 1$  (A can be 0 or 1)

(B) (2 points) Are there logical values of A, B, and C for which D is pulled down and up simultaneously? If so, values for A, B, and C that cause such a conflict; else write NONE.

Nora Nanda, Helena's assistant, suggests that the devices might be salvaged by using them to compute useful functions of fewer than 3 inputs. She proposes that a two-input function of X and Y, for example, might be computed by connecting each of the three inputs A, B, and C to either X, Y, or the logical constants 0 (ground) or 1 (vdd), and reading the output on D.

(C) (1 point) Can Nora's approach be used to compute **NAND** of X and Y? If so, choose values (X, Y, 0, or 1) for each of A, B, and C such that D is  $\overline{XY}$ ; else circle NO.

Choose A, B, C values or circle NO: 
$$A = X$$
;  $B = Y$ ;  $C = 0$ ; or NO

(D) (1 point) Can Nora's approach be used to compute **NOR** of X and Y? If so, choose values (X, Y, 0, or 1) for each of A, B, and C such that D is  $\overline{X + Y}$ ; else circle NO.

Choose A, B, C values or circle NO: 
$$A = X$$
;  $B = 1$ ;  $C = Y$ ; or NO

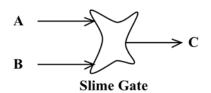
(E) (1 point) Can Nora's approach be used to compute  $X + \overline{Y}$ ? If so, choose values (X, Y, 0, or 1) for each of A, B, and C such that D is  $X + \overline{Y}$ ; else circle NO.

Choose A, B, C values or circle NO:  $A = \underline{\hspace{1cm}}; B = \underline{\hspace{1cm}}; C = \underline{\hspace{1cm}}; O$ 

#### Problem 4 (7 points): Organic Logic

Organic Logic, Inc, is a Cambridge startup that has developed an interesting device built using unidentified organic sludge from the depths of the Charles River; they would like to use it to perform logic functions. Their device, termed a Slime Gate, has two inputs **A** and **B**, and one output **C** (in addition to power and ground connections):

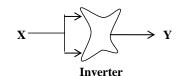
With a 3-volt power supply, they have noted that Slime Gates reliably behave as follows:



- The output C is always in the range 0 volts < C < 3 volts.
- When both A and B have been at less than 1 volt for a nanosecond or more, the voltage at C is greater than 2.5 volts
- When either or both of A and B have been at more than 2 volts for at least a nanosecond, C carries a voltage of less than 0.5 volts.

Aside from the above constraints, the voltage at C is generally unpredictable; it varies widely between individual Slime Gate devices.

As an O.L.I. consultant, you have proposed the circuit to the right as an inverter in the evolving family of Slime Gate logic:



(A) (3 points) Give logic representation parameters yielding maximum noise margins and for which your diagram depicts a valid inverter.

$$V_{OL}$$
:  $0.5 \text{ V}$ ;  $V_{IL}$ :  $1 \text{ V}$ ;  $V_{IH}$ :  $2 \text{ V}$ ;  $V_{OH}$ :  $2.5 \text{ V}$ 

**(B)** (2 points) Give appropriate specifications for propagation and contamination delays for this inverter:

$$t_{pd}$$
: \_\_\_\_\_ ns;  $t_{cd}$ : \_\_\_\_\_ ns

(C) (1 point) Suppose the Slime Gate is used as a 2-input logic gate in this same family, as shown to the right. What, if any, function of P and Q is represented by the output R?

$$\begin{array}{c} P \\ Q \\ \hline \\ 2\text{-input gate} \end{array}$$

Boolean function of P and Q, or "None": P + Q (NOR)

(**D**) (1 point) Is the Slime Gate, based on the description above, a *lenient* device?

**END OF QUIZ!**