

Now that we have some sense about how MOSFETs function, let's use them to build circuits to process our digitally encoded information.

We have two simple rules we'll use when building the circuits, which, if they're followed, will allow us to abstract the behavior of the MOSFET as a simple voltage-controlled switch.

The first rule is that we'll only use n-channel MOSFETs, which we'll call NFETs for short, when building pulldown circuits that connect a signaling node to the GROUND rail of the power supply.

When the pulldown circuit is conducting, the signaling node will be at 0V and qualify as the digital value "0".

If we obey this rule, NFETs will act as switches controlled by  $V_{GS}$ , the difference between the voltage of the gate terminal and the voltage of the source terminal.

When  $V_{GS}$  is lower than the MOSFET's threshold voltage, the switch is "open" or not conducting and there is no connection between the MOSFET's source and drain terminals.

If  $V_{GS}$  is greater than the threshold voltage, the switch is "on" or conducting and there is a connection between the source and drain terminals.

That path has a resistance determined by the magnitude of  $V_{GS}$ .

The larger  $V_{GS}$ , the lower the effective resistance of the switch and the more current that will flow from drain to source.

When designing pulldown circuits of NFET switches, we can use the following simple mental model for each NFET switch: if the gate voltage is a digital 0, the switch will be off; if the gate voltage is a digital 1, the switch will be on.

The situation with PFET switches is analogous, except that the potentials are reversed.

Our rule is that PFETs can only be used in pullup circuits, used to connect a signaling node to the power supply voltage, which we'll call  $V_{DD}$ .

When the pullup circuit is conducting, the signaling node will be at  $V_{DD}$  volts and qualify as the digital value "1".

PFETs have a negative threshold voltage and  $V_{GS}$  has to be less than the threshold voltage in order for the PFET switch to be conducting.

All these negatives can be a bit confusing, but, happily there's a simple mental model we can use for each PFET switch in the pullup circuit: if the gate voltage is a digital 0, the switch will be on; if the gate voltage is a digital 1,

the switch will be off - basically the opposite behavior of the NFET switch.

You may be wondering why we can't use NFETs in pullup circuits or PFETs in pulldown circuits.

You'll get to explore the answer to this question in the first lab of Assignment 2.

Meanwhile, the short answer is that the signaling node will experience degraded signaling levels and we'll lose the noise margins we've worked so hard to create!

Now consider the CMOS implementation of a combinational inverter.

If the inverter's input is a digital 0, its output is a digital 1, and vice versa.

The inverter circuit consists of a single NFET switch for the pulldown circuit, connecting the output node to GROUND and a single PFET switch for the pullup circuit, connecting the output to  $V_{DD}$ .

The gate terminals of both switches are connected to the inverter's input node.

The inverter's voltage transfer characteristic is shown in the figure.

When  $V_{IN}$  is a digital 0 input, we see that  $V_{OUT}$  is greater than or equal to  $V_{OH}$ , representing a digital 1 output.

Let's look at the state of the pullup and pulldown switches when the input is a digital 0.

Recalling the simple mental model for the NFET and PFET switches, a 0-input means the NFET switch is off, so there's no connection between the output node and ground, and the PFET switch is on, making a connection between the output node and  $V_{DD}$ .

Current will flow through the pullup switch, charging the output node until its voltage reaches  $V_{DD}$ .

Once both the source and drain terminals are at  $V_{DD}$ , there's no voltage difference across the switch and hence no more current will flow through the switch.

Similarly, when  $V_{IN}$  is a digital 1, the NFET switch is on and PFET switch is off, so the output is connected to ground and eventually reaches a voltage of 0V.

Again, current flow through pulldown switch will cease once the output node reaches 0V.

When the input voltage is in the middle of its range, it's possible, depending on the particular power supply voltage used and the threshold voltage of the MOSFETs, that both the pullup and pulldown circuits will be conducting for a

short period of time.

That's okay.

In fact, with both MOSFET switches on, small changes in the input voltage will produce large changes in the output voltage, leading to the very high gain exhibited by CMOS devices.

This in turn will mean we can pick signaling thresholds that incorporate generous noise margins, allowing CMOS devices to work reliably in many different operating environments.

This is our first CMOS combinational logic gate.

In the next video, we'll explore how to build other, more interesting logic functions.