We'll get a good understanding of how the register operates as we follow the signals through the circuit.

The overall operation of the register is simple:

At the rising 0-to-1 transition of the clock input, the register samples the value of the D input and stores that value until the next rising clock edge.

The Q output is simply the value stored in the register. Let's see how the register implements this functionality.

The clock signal is connected to the gate inputs of the master and slave latches.

Since all the action happens when the clock makes a transition, it's those events we'll focus on.

The clock transition from LOW to HIGH is called the rising edge of the clock.

And its transition from HIGH to LOW is called the falling edge.

Let's start by looking the operation of the master latch and its output signal, which is labeled STAR in the diagram.

On the rising edge of the clock, the master latch goes from open to closed, sampling the value on its input and entering memory mode.

The sampled value thus becomes the output of the latch as long as the latch stays closed.

You can see that the STAR signal remains stable whenever the clock signal is high.

On the falling edge of the clock the master latch opens and its output will then reflect any changes in the D input, delayed by the tPD of the latch.

Now let's figure out what the slave is doing.

It's output signal, which also serves as the output of D register, is shown as the bottom waveform.

On the rising edge of the clock the slave latch opens and its output will follow the value of the STAR signal.

Remember though that the STAR signal is stable while the clock is HIGH since the master latch is closed,

so the Q signal is also stable after an initial transition if value saved in the slave latch is changing.

At the falling clock edge [CLICK], the slave goes from open to closed, sampling the value on its input and entering memory mode.

The sampled value then becomes the output of the slave latch as long as the latch stays closed.

You can see that that the Q output remains stable whenever the clock signal is LOW.

Now let's just look at the Q signal by itself for a moment.

It only changes when the slave latch opens at the rising edge of the clock.

The rest of the time either the input to slave latch is stable or the slave latch is closed.

The change in the Q output is triggered by the rising edge of the clock, hence the name "positive-edge-triggered D register".

The convention for labeling the clock input in the schematic icon for an edge-triggered device is to use a little triangle.

You can see that here in the schematic symbol for the D register.

There is one tricky problem we have to solve when designing the circuitry for the register.

On the falling clock edge, the slave latch transitions from open to closed and so its input (the STAR signal) must meet the setup and hold times of the slave latch in order to ensure correct operation.

The complication is that the master latch opens at the same time, so the STAR signal may change shortly after the clock edge.

The contamination delay of the master latch tells us how long the old value will be stable after the falling clock edge.

And the hold time on the slave latch tells us how long it has to remain stable after the falling clock edge.

So to ensure correct operation of the slave latch, the contamination delay of the master latch has to be greater than or equal to the hold time of the slave latch.

Doing the necessary analysis can be a bit tricky since we have to consider manufacturing variations as well as environmental factors such as temperature and power supply voltage.

If necessary, extra gate delays (e.g., pairs of inverters) can be added between the master and slave latches to increase the contamination delay on the slave's input relative to the falling clock edge.

Note that we can only solve slave latch hold time issues by changing the design of the circuit.

Here’s a summary of the timing specifications for a D register.

Changes in the Q signal are triggered by a rising edge on the clock input.

The propagation delay t_PD of the register is an upper bound on the time it takes for the Q output to become valid and stable after the rising clock edge.

The contamination delay of the register is a lower bound on the time the previous value of Q remains valid after the rising clock edge.

Note that both t_CD and t_PD are measured relative to the rising edge of the clock.

Registers are designed to be lenient in the sense that if the previous value of Q and the new value of Q are the same, the stability of the Q signal is guaranteed during the rising clock edge.

In other words, the t_CD and t_PD specifications only apply when the Q output actually changes.

In order to ensure correct operation of the master latch, the register’s D input must meet the setup and hold time constraints for the master latch.

So the following two specifications are determined by the timing of the master latch.

t_SETUP is the amount of time that the D input must be valid and stable before the rising clock edge and t_HOLD is the amount of time that D must be valid and stable after the rising clock.

This region of stability surrounding the clock edge ensures that we’re obeying the dynamic discipline for the master latch.

So when you use a D register component from a manufacturer’s gate library,

you’ll need to look up these four timing specifications in the register’s data sheet in order to analyze the timing of your overall circuit.

We’ll see how this analysis is done in the next section.