Now we get to the fun part!

To build other logic gates, we'll design complementary pullup and pulldown circuits, hooked up as shown in the diagram on the right, to control the voltage of the output node.

"Complementary" refers to property that when one of the circuits is conducting, the other is not.

When the pullup circuit is conducting and the pulldown circuit is not, the output node has a connection to V_DD and its output voltage will quickly rise to become a valid digital 1 output.

Similarly, when the pulldown circuit is conducting and the pullup is not, the output node has a connection to GROUND and its output voltage will quickly fall to become a valid digital 0 output.

If the circuits are incorrectly designed so that they are not complementary and could both be conducting for an extended period of time, there's a path between V_DD and GROUND and large amounts of short circuit current will flow, a very bad idea.

Since our simple switch model won't let us determine the output voltage in this case, we'll call this output value "X" or unknown.

Another possibility with a non-complementary pullup and pulldown is that neither is conducting and the output node has no connection to either power supply voltage.

At this point, the output node is electrically floating and whatever charge is stored by the nodal capacitance will stay there, at least for a while.

This is a form of memory and we'll come back to this in a couple of lectures.

For now, we'll concentrate on the behavior of devices with complementary pullups and pulldowns.

Since the pullup and pulldown circuits are complementary, we'll see there's a nice symmetry in their design.

We've already seen the simplest complementary circuit: a single NFET pulldown and a single PFET pullup.

If the same signal controls both switches, it's easy to see that when one switch is on, the other switch is off.

Now consider a pulldown circuit consisting of two NFET switches in series.

There's a connection through both switches when A is 1 and B is 1.

For any other combination of A and B values, one or the other of the switches (or both!) will be off.

The complementary circuit to NFET switches in series is PFET switches in parallel.

There's a connection between the top and bottom circuit nodes when either of the PFET switches is on, i.e., when A is 0 or B is 0.

As a thought experiment consider all possible pairs of values for A and B: 00, 01, 10, and 11.

When one or both of the inputs is 0, the series NFET circuit is not conducting and parallel PFET circuit is.

And when both inputs are 1, the series NFET circuit is conducting but the parallel PFET circuit is not.

Finally consider the case where we have parallel NFETs and series PFETs.

Conduct the same thought experiment as above to convince yourself that when one of the circuits is conducting the other isn't.

Let's put these observations to work when building our next CMOS combinational device.

In this device, we're using series NFETs in the pulldown and parallel PFETs in the pullup, circuits that we convinced ourselves were complementary in the previous slide.

We can build a tabular representation, called a truth table, that describes the value of Z for all possible combinations of the input values for A and B.

When A and B are 0, the PFETs are on and the NFETs are off, so Z is connected to V_DD and the output of the device is a digital 1.

In fact, if either A or B is 0 [CLICK, CLICK] that continues to be the case, and the value of Z is still 1.

Only when both A and B are 1 [CLICK], will both NFETs be on and the value of Z become 0.

This particular device is called a NAND gate, short for "NOT-AND", a function that is the inverse of the AND function.

Returning to a physical view for a moment, the figure on the left is a bird's eye view, looking down on the surface of the integrated circuit, showing how the MOSFETs are laid out in two dimensions.

The blue material represents metal wires with large top and bottom metal runs connecting to V_DD and GROUND.

The red material forms the polysilicon gate nodes, the green material the n-type source/drain diffusions for the NFETs and the tan material the p-type source/drain diffusions for the PFETs.

Can you see that the NFETs are connected in series and the PFETs in parallel?

Just to give you a sense of the costs of making a single NAND gate, the yellow box is a back-of-the-envelope calculation showing that we can manufacture approximately 26 billion NAND gates on a single 300mm (that's 12 inches for us non-metric folks) silicon wafer.

For the older IC manufacturing process shown here, it costs about $3500 to buy the materials and perform the manufacturing steps needed to form the circuitry for all those NAND gates.

So the final cost is a bit more than 100 nano-dollars per NAND gate.

I think this qualifies as both cheap and small!