

Optical Receiver Design Project

November 18, 2005

Due: December 6, 2005 on the MIT course website (no later than 12:55PM)
(late project reports not accepted)

1. Overview

The explosive growth in data communications has stimulated the development of optical systems for high channel capacity (typically 4-16 channels) and high bandwidth. In a fiber optic system, a transmitter encodes the data in the form of laser pulses that are transmitted over a long optical fiber. At the other end, a receiver detects the attenuated optical signal and amplifies it to digital levels.

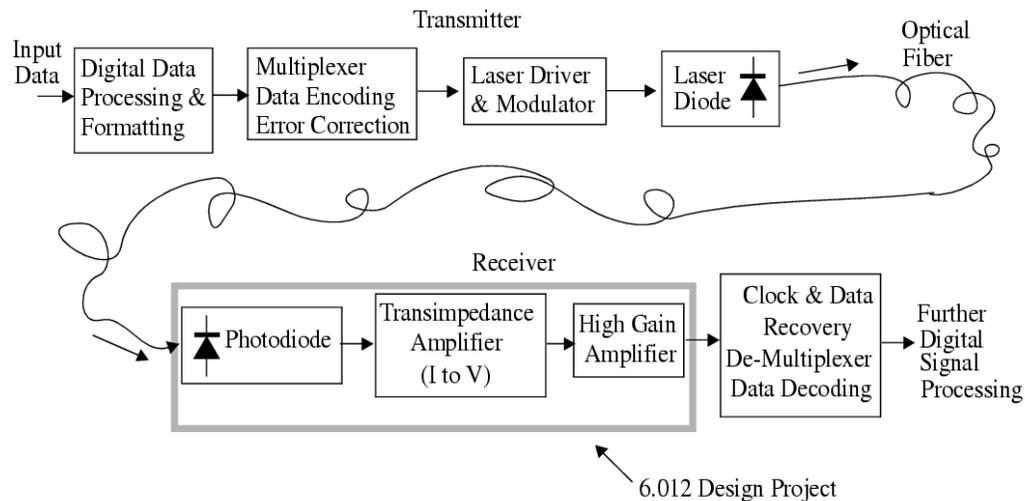


Figure 1: Block diagram of an optical transmitter and receiver.

A block diagram of an optical transmitter and receiver is shown in Figure 1. On the transmitter path, the data is multiplexed, encoded, and error correction bits are added. A laser driver and modulator drive the laser diode, which transmits an optical signal over the fiber. After some loss in the fiber, the optical signal is detected at the receiver end by the photodiode. A transimpedance amplifier converts the small photodiode current into a voltage, which is then amplified to digital levels for subsequent digital signal processing. The transimpedance amplifier is also called a transresistance amplifier in 6.012; for cultural reasons, we will stick with the transimpedance amplifier terminology.

Integration of all of the functions on either side of Figure 1 onto a single CMOS chip would save costs, but the implementation has eluded system designers in part due to the complexity of realizing high-performance receiver circuits in CMOS. The goal of this design project is to design a fast, high gain, low noise, and low power optical receiver in an inexpensive CMOS process.

2. Design problem statement

Figure 2 shows the schematic of the optical receiver. It consists of three CMOS stages: a transimpedance amplifier, a saturating or limiting amplifier, and an output driver. We describe these three stages next.

Light creates electron-hole pairs that produce a current I_{light} in the reverse-biased photodiode. The diode can be modelled as a current source of value I_{light} which flows in the reverse bias direction of the diode. Although the laser diode produces a large square wave pulse at the other end of the fiber, dispersion and loss make the diode current I_{light} appear sinusoidal. This current is only guaranteed to have a peak value of about $10 \mu\text{A}$. Depending on the system, loss in the fiber could be lower and the peak diode current could be larger. However, to ensure proper operation for all systems, the worst-case (i.e. minimum) current must be used for the design. The receiver should operate at speeds up to 1 MHz.

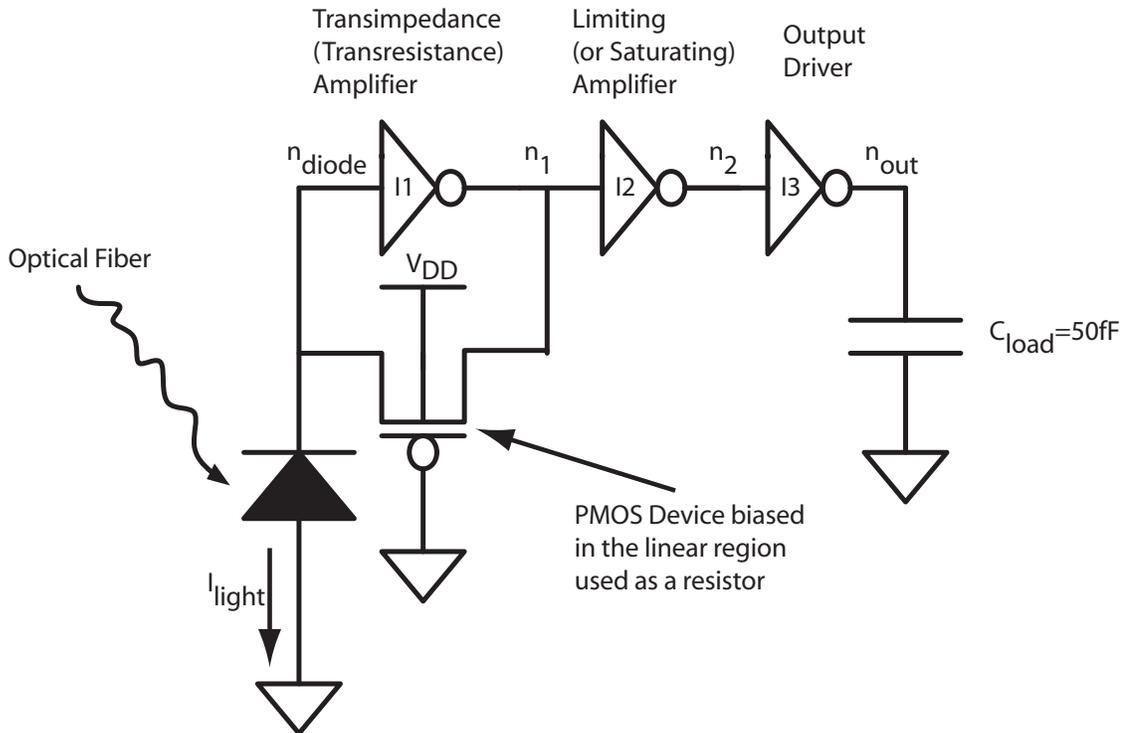


Figure 2: Schematic of optical receiver.

The first-stage CMOS inverter I1 and feedback resistor constitute a transimpedance amplifier that converts the photodiode current into a voltage V_1 at node n_1 . A feedback resistor sets the gain of

the stage, which must be large to reduce the effects of noise in later stages.

To set a reasonable design point you might first want to start by using a simple linear resistor and determine what value you could use to meet your design goals. Unfortunately, though linear resistors can be realized in silicon technology by using undoped poly for large resistor values, this approach consumes a lot of area. With the knowledge of device physics that you have acquired in 6.012, in order to minimize the cost you have decided to realize this resistor using a PMOS biased in the linear region. An additional concern in this amplifier is that the gain needs to be as constant as possible over the expected range of I_{light} values. This means that the resistor value should be as constant as possible over the range of voltages at its terminals, or, in other words, as linear as possible. Power must be minimized in this design, so no extra bias circuitry can be afforded. The PMOS device is to be connected as shown in Fig. 2 with the gate of the PMOS connected to GND and the bulk connected to V_{DD} . The design decision that you need to make is to size the PMOS appropriately to achieve the desired value of the resistor.

The closed-loop small-signal gain $\frac{V_1}{I_{light}}$ of this first transimpedance amplifier needs to be as constant as possible over the range of I_{light} values shown in Figure 3. You will need to derive an expression for this closed-loop gain $\frac{V_1}{I_{light}}$, where V_1 is the voltage at node n_1 . Notice that since I_{light} is small, V_{diode} (the voltage at node n_{diode}) and V_1 will stay close to the midpoint of inverter I1, and I1 will be held in the high-gain region. Thus the transistors in inverter I1 will stay in the saturation region, and the small signal model can be used over the full range of input current. For the I_{light} shown in Figure 3, V_1 should have a peak-to-peak amplitude of at least $0.1 V_{pp}$ (peak-to-peak voltage), as indicated in Figure 3. For noise immunity, V_1 should be near the middle of the total voltage range. Therefore, the minimum of V_1 should be at 2.5 V, as indicated in Figure 3. To ensure that the photodiode stays in reverse bias, and in an attempt to keep the depletion region width constant, the reverse biased diode voltage V_{diode} should vary by no more than 10 mV peak-to-peak ($10 mV_{pp}$). To understand how V_{diode} varies with the input current and output voltage, you will also need to derive an expression for V_{diode} as a function of I_{light} and V_1 .

The second stage is called a limiting or saturating amplifier. This high-gain CMOS stage amplifies the small voltage V_1 . For maximum amplification, V_1 should be in the high gain region of inverter I2. The open-loop voltage gain of the limiting amplifier A_{v2} should be large enough to ensure that V_1 is amplified to full logic levels. To scale $0.1 V_{pp}$ at node n_1 to $5 V_{pp}$ at node n_2 requires a gain of 50. Since the gain away from the midpoint of the inverter will be less than the maximum gain A_{v2} , the specification is $|A_{v2}| \geq 90$.

The output CMOS stage drives both the wire capacitance and the input capacitance of the digital signal processing circuits. This can be modelled as a constant 50 fF load capacitor. The output driver should be high speed to maximize the frequency at which the receiver can operate. Since the output will be routed to the digital side of the chip, it should also have good noise margins. Specifically, $t_{PHL}, t_{PLH} \leq 0.5$ nsec and $NM_L, NM_H \geq 1.4$ V between the input and output of inverter I3.

Power consumption is a big differentiator in system design. To get the edge over competitors, power should be minimized. Since the input and output voltages of inverter I1 are so small, I1 will stay in the high gain region, dissipating static power. To simplify your hand calculations, calculate the power dissipated in I1 when $I_{light}=0$. There is also dynamic power required to charge and discharge the parasitic and load capacitance at nodes n_1 , n_2 and n_{out} . The total power consumption should

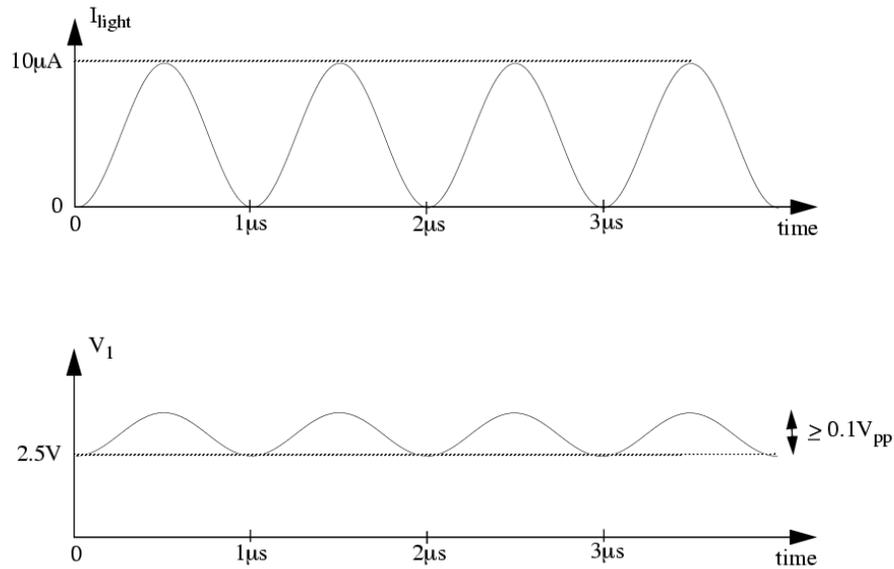


Figure 3: Current due to light shining on the reverse biased diode as a function of time. Also shown is the desired minimum peak-to-peak voltage at node n_1 .

be minimized, which means that only enough power should be used to adequately meet the other specifications.

The cost of the optical receiver is related to the amount of silicon die area that is used. To maximize profits, the die area should be minimized. This means that transistor sizes should be as small as possible without compromising any of the other design specifications.

In summary, the design challenges and specifications are:

1. Derive an expression for the closed-loop transimpedance small-signal gain $\frac{V_1}{I_{light}}$. To make this equation easier to use, write it in terms of the open-loop voltage gain A_{v1} of the first inverter I1. Assume a low-frequency small signal model, i.e. that all of the capacitors in the model are open circuits. To simplify your derivation replace the PMOS with a real resistance. Design this gain to be large enough that V_1 is at least $0.1V_{pp}$ for $I_{light}=10\mu\text{A}$.
2. Derive an expression for V_{diode} as a function of I_{light} and V_1 . Design so the swing on node V_{diode} is less than $10mV_{pp}$ ($\Delta V_{diode} \leq 10mV_{pp}$).
3. Choose the size of feedback PMOS transistor needed to achieve the desired value of resistance.
4. Design the logic threshold V_{M2} of inverter I2 so the voltage V_1 at node n_1 is in the high-gain region of I2.
5. $|A_{V2}| \geq 90$.

6. At the output, $t_{pHL}, t_{pLH} \leq 0.5$ nsec and $NM_L, NM_H \geq 1.4V$. Note that t_{pHL} and t_{pLH} are defined between the input and output of I3.
7. Minimize power dissipation P_{diss} . This means that no more power should be used other than that required to meet the specifications.
8. Minimize area. Again, enough area should be used to meet the specifications.

3. Device models

The SPECTRE model parameters for minimum-size CMOS transistors in our technology can be found in the CADENCE tutorial on the 6.012 OCW website . All minimum size transistors have dimensions: $L_{nmin} = 1.5 \mu m$, $W_{nmin} = 3 \mu m$, $L_{pmin} = 1.5 \mu m$, $W_{pmin} = 6 \mu m$. The design may require the use of larger transistors than the minimum size. Due to processing constraints, W and L can scale up in increments no smaller than $0.5 \mu m$. The parameter LAMBDA must be changed according to the transistor gate length, as indicated in CADENCE tutorial on the 6012 ocw website. Read §4.6 of Howe & Sodini to see how transistor capacitances scale with geometry. Note that processing constraints do not allow the dimensions of these transistors to be reduced below the minimum sizes.

4. Deliverables

The deliverables of this design problem are as follows.

1. (20 points) A *one-page design review abstract*. This is an abstract summarizing your project for a design review meeting. At the design review, your design (as well as others for other parts of the chip) will be presented. It should bring other designers that will attend the review up to speed on your design. The abstract should concisely state the nature of the problem, the key design issues and trade-offs involved, your design strategy arguing why it is a good one, and the important results. The abstract should be typed and well-written to ensure that you keep your job in this tough economy!
2. (60 points) A technical report with the following parts:
 - (a) *Summary of design decisions and hand calculations*. Here you should show a schematic diagram of your complete design. On the schematic you should indicate the selected transistor dimensions. You should describe and comment on the following:
 - i. Derivation of expression for closed-loop gain of the transimpedance amplifier $\frac{V_i}{I_{light}}$ in terms of the open-loop voltage gain A_{v1} of inverter I1. Comment on how the feedback resistor and inverter I1 should be designed (i.e. how the transistors should be sized.).
 - ii. Describe and defend your PMOS transistor sizing to implement the feedback resistor.
 - iii. Hand calculations of the closed-loop voltage gain for the transimpedance amplifier. Also include hand calculations for the value of the feedback resistor, A_{v1} and V_{M1} .
 - iv. Hand calculations for V_{M2} , A_{v2} .
 - v. Hand calculations for t_{PHL} , t_{PLH} , NM_L , NM_H of inverter I3. Notice that the equations for t_{PHL} and t_{PLH} derived in class assume that the input switches instantaneously. Is this true of the voltage V_2 at node n_2 ? Why might your hand calculations for propagation delay not quite match the CADENCE simulations?
 - vi. Hand calculations for the static and dynamic power dissipation. Remember to use $I_{light} = 0$ to simplify your hand calculation for the static power of inverter I1.
 - vii. Hand calculations for the die area consumed by each transistor as well as the total design area. The area for each transistor can be estimated as $W * (L + 2 * L_{diff})$. Compare the area of your feedback transistor to the area that would be needed to

implement the same resistance as an integrated circuit polysilicon resistor. Assume the polysilicon resistor has $R_{sh}=100 \frac{\Omega}{\text{square}}$ and minimum dimensions of $0.5 \mu\text{m}$.

Your hand calculations should be commented appropriately. You should describe the thought process that you followed in your design, the trade-offs that you faced and how you arrived at your design.

- (b) *CADENCE schematics and printouts.* You should carry out the following CADENCE simulations:
- DC transfer characteristics of the transimpedance amplifier stage. Two simulations should be performed. One without the feedback resistor and a DC voltage at the input so A_{v1} and V_{M1} can be found. The second DC sweep should replace the input with a current source and include the feedback transistor so that you can find the closed-loop gain $\frac{V_1}{I_{light}}$ of the transimpedance amplifier. You may want to create separate CADENCE schematics for these simulations. Turn in a printout of the schematics and plots of the waveforms V_{diode} , V_1 , V_2 , and V_{out} .
 - Transient simulation of the transimpedance amplifier stage. Please turn in a printout of the transient simulation of V_1 for the I_{light} given in Figure 3.
 - DC transfer characteristics of the limiting amplifier. From this simulation, extract A_{v2} and V_{M2} .
 - DC transfer characteristics of the output driver. From this simulation, extract NM_L and NM_H .
 - Transient simulation for the entire design showing waveforms for V_{diode} , V_1 , V_2 and V_{out} . Use the Analog Design Environment in CADENCE to extract the propagation delays at the output t_{pHL} and t_{pLH} as well as the total power dissipation. To avoid initial transitory effects, use 3rd or 4th clock cycles for the t_{pHL} and t_{pLH} extractions. Turn in a printout of the waveforms to substantiate your results

The final CADENCE netlist of the entire design (the one used for the transient simulation, part (v)) should be submitted to the [MIT course website](#). The netlist can be found in `<your home dir>/simulation/<name of the test bench>/spectre/schematic/netlist/input.scs`

Brief analysis: You should comment on how, as a result of Cadence simulations, you had to change some of the design parameters from those selected in the hand calculations in order to meet the specifications.

- (c) *Suggestions for future work.* Although the receiver in this project is only running at a speed of 1 MHz, modern day optical communications systems are running at speeds of 1 Gb/s and up. Speculate briefly on what you would need to change to reach these speeds, and what other design parameters might suffer. A few sentences should suffice.
- (10 points) *Answer sheet with summary of results.* Please use the sheet at the end of this handout to summarize your results. Fill in the transistor sizes used for each inverter and the feedback transistor, give the expression you derived for the closed-loop gain of the transimpedance amplifier in terms of A_{v1} , and give the expression derived for V_{diode} in terms of I_{light} and V_1 . Compare and summarize the results of your hand calculations and CADENCE simulations. Also fill in the missing specifications, and don't forget to include units in all of your answers.
 - (10 points) *Post-mortem and evaluation.* On a separate page, please give us feedback on this assignment. Answer at least the following questions: Were the instructions clear? What did you learn from doing this assignment? What was the most frustrating part of the assignment?

The most satisfying part? How many hours did it take you? Please feel free to offer other opinions, suggestions or advice; don't be afraid to be candid. The grader will check that you have at least provided an answer to the above questions, then he or she will separate this page from the rest of your work before the rest of the project is graded.

5. Rules and assorted advice

You are encouraged to work on this design problem with a partner. However, both members of the team must have carried out all aspects of the design problem. It is not allowed to break the design problem into two pieces and have each partner carry out only one of these pieces. Each individual must also turn in a complete set of deliverables as outlined above. The partner's name should be identified in the answer sheet.

Since we are piloting the **MIT course** submission for the first time, please make a sample submission to the **MIT course website** well before the project is due.

The deadline for this assignment is firm. The **website** will not accept late submissions.

Use **CADENCE on MIT Server** . For help on how to get started in Cadence, refer to the documentation that is available in the Project category of the 6.012 **OCW web site** .

Hint for getting started on the transimpedance amplifier stage design: Think about what the voltages V_1 and V_{diode} are when $I_{light} = 0$. How about when $I_{light} = 10 \mu A$?

Hint for getting started with your design: start your simulations with just the first stage transimpedance amplifier design and an ideal feedback resistor. Understand the simulations of this circuit and meet the specifications before replacing your resistor with a transistor. Similarly, you may want to simulate each stage independently before connecting them together.

Hint for hand calculation of dynamic power: think about the voltage swings and capacitances at each node. Which node(s) should dominate the dynamic power and which nodes can you ignore?

To measure the power dissipation please refer to the second **CADENCE** tutorial on the 6.012 **OCW website** . Choose $t=4 \mu s$ to start since it is sufficiently away from any startup transients. Measure until $t=5 \mu s$ so that the measurement is taken over one period of the input.

For the diode, you can use a current source from analogLib called isin and set the dc current to 5u the amplitude to 5u and the frequency to 1 MHz.

When doing hand calculations, include the drain-body, source-body and gate-source capacitance for your transistors, as they all have a significant effect on the speed and power dissipation of the circuit. To simplify the hand calculations, assume the gate-source capacitance is equal to $\frac{2}{3}WLC_{ox}$. Also assume that the source-body and drain-body capacitors are bias independent with a value equal to the zero voltage capacitance. This will produce a conservative design, as the average capacitance is smaller than this. In general, a "hand calculation" means the use of simple equations to calculate

results. In this case, these are the equations derived in class and in the book for delay, noise margins, etc.

Give yourself plenty of design room for the coarseness of hand calculations. In the end, it is the output of the CADENCE simulation that will be used to determine whether your design meets specs.

The design process is outlined below. It involves thinking about and understanding the circuit, not using Excel or another program to try to optimize parameters (you'll find that this won't work anyway!)

1. Think about how the circuits should work.
2. Perform hand calculations to get a rough idea of the tradeoffs of the circuit parameters (device sizes, etc) with the relevant design parameters.
3. Come up with a rough hand calculation for the device sizes required to meet the specifications.
4. Simulate your circuit in CADENCE to verify that it functions and meets the specifications. If it does not meet the specifications, use your analytical models to guide the direction in which you need to change the device sizes. Revise your device sizes and re-simulate.

The effort involved in this assignment is substantial. You should start early. There are many aspects to this design problem that will require sustained attention on your part for a substantial amount of time. This assignment cannot be done at the last minute!

Ask us plenty of questions. While every effort has been made for the specs to be reasonable and for the design project to be well described, there might be residual ambiguities. The first line of advice is the TA's. After that, don't hesitate to approach the recitation instructors and the lecturer.

6.012 Optical Receiver Design Project Quick Final Checklist

	abstract
	schematic diagram of your circuit with transistor sizes labelled
	derivation of $\frac{V_1}{I_{light}}$ with appropriate comments
	description of sizing of feedback transistor
	hand calculations for $A_{v1}, V_{M1}, V_{M2}, A_{v2}, t_{pHL}, t_{pLH}, NM_L, NM_H$
	hand calculation for power dissipation P_{diss}
	hand calculation for the die area consumed by your design
	comparison of area for your feedback transistor and a metal resistor
	CADENCE simulations showing $A_{v1}, V_{M1}, V_{M2}, A_{v2}, t_{pHL}, t_{pLH}, NM_L, NM_H$
	CADENCE simulations showing $\frac{V_1}{I_{light}}$
	CADENCE transient simulations showing V_{diode}, V_1, V_2 and V_{out}
	Submit your design to the 6.012 MIT Server
	suggestions for future work
	answer sheet with summary of results
	post-mortem and evaluation

Optical Receiver Design Project - Summary Answer Sheet

Name: _____ Recitation: _____

Partner's name: _____

Size	Feedback Transistor	I1	I2	I3	units
W_n					
L_n					
W_p					
L_p					

Specification	Hand calculation	CADENCE simulation	Required specs
closed-loop gain of transimpedance amplifier $\frac{V_1}{I_{light}}$			
ΔV_{diode}			≤ 10 mV
A_{v1}			_____
V_{M1}			_____
V_{1pp}			$\geq 0.1 V_{pp}$
$ A_{v2} $			≥ 90
V_{M2}			_____
t_{pHL} (of V_2 to V_{out})			≤ 0.5 nsec
t_{pLH} (of V_2 to V_{out})			≤ 0.5 nsec
NM_L (of I3)			≥ 1.4 V
NM_H (of I3)			≥ 1.4 V
P_{diss}			minimum
Total area of transistors in design		_____	minimum
Total area with poly resistor		_____	minimum

Expression for closed-loop gain of the transimpedance amplifier $\frac{V_1}{I_{light}}$:

Expression for V_{diode} as a function of V_1 and I_{light} :