6.012 - Microelectronic Devices and Circuits Lecture 24 - Intrin. Freq. Limits - Outline

Announcements

Final Exam - Tuesday, Dec 15, 9:00 am - 12 noon

Review - Shunt feedback capacitances: C_μ and C_{gd}
Miller effect: any C bridging a gain stage looks bigger at the input
Marvelous cascode: CE/S-CB/G (E/SF-CB/G work, too - see μA741)
large bandwidth, large output resistance
used in gain stages and in current sources

Using the Miller effect to advantage: Stabilizing OP Amps - the µA741

• Intrinsic high frequency limitations of transistors

General approach MOSFETs: f_T

biasing for speed impact of velocity saturation design lessons

BJTs: f_{β} , f_{T} , f_{α} biasing for speed design lessons

Summary of OCTC and SCTC results $\log |A_{vd}|$ (Mid-band Range) $(WLO)^* (WH)^* ($

- **OCTC**: an estimate for ω_{HI}
 - ω_H* is a weighted sum of ω's associated with <u>device capacitances</u>: (add RC's and invert)
 - 2. Smallest ω (largest RC) dominates ω_{HI}^*
 - 3. Provides a lower bound on ω_{HI}
- **<u>SCTC</u>**: an estimate for ω_{LO}
 - 1. ω_{LO}^* is a weighted sum of w's associated with <u>bias capacitors</u>: (add ω 's directly)
 - 2. Largest ω (smallest RC) dominates ω_{LO}^*
 - 3. Provides a upper bound on ω_{LO}

The Miller effect (general)

Consider an amplifier shunted by a capacitor, and consider how the capacitor looks at the input and output terminals:



The cascode when the substrate is grounded: High frequency issues:

L.E.C. of cascode: can't use equivalent transistor idea here because it didn't address the issue of the C's!



Common-source gain without the Miller effect penalty!

Multi-stage amplifier analysis and design: The µA741 Figuring the circuit out: **Emitter-follower/** common-base "cascode" differential gain stage + V o -⑦ V+ $Q_9 Q_{12}$ Q_{13} 0. 1₃ Q_{14} Noninverting **1**1 $\frac{30 \text{ pF}}{C_1} \begin{bmatrix} \frac{R_2}{45 \text{ k}\Omega} \end{bmatrix}$ input Q_1 3-0 Q_2 -2 Ro $R_5 | 35 \leq$ 25 Ω Inverting LVV input kΩ -6) Q_3 Q_4 Q₁ Q2 Output 75 kΩ EF R_{10} Q16 Q₁₄ 0 50 Ω ۲ĩ, v 12 Q CB Q17 -KQ11 Q19 Q_{10} Q_3 Q_6 Q4 Q_5 0+ Offset null $\begin{array}{c} R_{12} \\ S_{12} \\ S_{12} \\ S_{11} \\ S_{11$ v_{out} 1₂ R_4 Q₂₀ $\gtrsim 15 \text{ k}\Omega$ R_3 R_2 R_1 $50 k\Omega$ $1 k\Omega$ $1 k\Omega$ v (4) V^{\cdot} Q16 Q₁₇ Offset null Q₆ Q5 The full schematic © Source unknown. All rights reserved. This content is excluded from our Creative Commons license. Push-pull output For more information, see http://ocw.mit.edu/fairuse. v **Current mirror load Simplified schematic Darlington common**emitter gain stage

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Multi-stage amplifier analysis and design: Understanding the µA741 input "cascode"

Begin with the BJT building-block stages:



Multi-stage amplifier analysis and design: Two-port models Two different "cascode" configurations, this time bipolar:



In a bipolar cascode, starting with an emitter follower still reduces the gain, but it also gives twice the input resistance, which is helpful.

Clif Fonstad, 12/8/09

Multi-stage amplifier analysis and design: MOSFET 2-port models Reviewing our building-block stages:



Multi-stage amplifier analysis and design: Two-port models Two different "<u>cascode</u>" configurations:



With MOSFETs, starting a cascode with a source follower costs a factor of two in gain
because r_{out} for an SF is small, so it isn't very attractive.Lecture 24 - Slide 9

Multi-stage amplifier analysis and design: The µA741



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Intrinsic performance - the best we can do

We've focused on ω_{HI} , the upper limit of mid-band, but even when $\omega > \omega_{HI}$ the $|A_v| > 1$, and the circuit is useful. For example, for the common source stage we had

$$A_{v}(j\omega) = \frac{-g_{t}(g_{m} - j\omega C_{gd})}{\{(j\omega)^{2}C_{gs}C_{gd} + j\omega[(g_{l} + g_{o})C_{gs} + (g_{l} + g_{o} + g_{t} + g_{m})C_{gd}] + (g_{l} + g_{o})g_{t}\}}$$



Intrinsic performance - the best we can do, cont.

Consider the two possibilities shown below, one for a voltage input and output where the metric would be the open circuit voltage gain, $A_{v,oc}$, and the other for a current input and output with the metric being the short circuit current gain, $A_{i,sc}$ (commonly written β_{sc}):



Of these two alternatives, β_{sc} is the more useful. $A_{v,oc}$ is derived with a voltage source driving a capacitor, something that doesn't give a meaningful result and leads to ever increasing input power. It also does not involve g_m and C_{gs} . Consequently, short circuit current gain is used as the intrinsic high frequency performance metric for transistors.

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Intrinsic ω_{HI} 's for MOSFETs - short-circuit current gain



The common-source short-circuit current gain is:

$$\beta_{sc}(j\omega) = \frac{i_d(j\omega)}{i_g(j\omega)} = \frac{g_m - j\omega C_{gd}}{j\omega (C_{gs} + C_{gd})}$$

there is one pole at $\omega = 0$, and one zero, ω_z :

$$\omega_z = \frac{g_m}{C_{gd}}$$

The short circuit current gain, β_{sc} , is infinite at DC ($\omega = 0$), and its magnitude decreases linearly with increasing frequency.

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Intrinsic ω_{HI} 's for MOSFETs - short-circuit current gain, cont.



The magnitude of β_{sc} decreases with ω , but it is still greater than one for a wide range of frequencies.

$$\left|\beta_{sc}(j\omega)\right| = \sqrt{\frac{g_m^2 + \omega^2 C_{gd}^2}{\omega^2 (C_{gs} + C_{gd})^2}}$$

The transistor is useful until $|\beta_{sc}|$ is less than one. The frequency at which this occurs is called ω_t . Setting = 1 and solving for ω_t yields:

$$\omega_{t} = \sqrt{\frac{g_{m}^{2}}{\left[\left(C_{gs} + C_{gd}\right)^{2} - C_{gd}^{2}\right]}} \approx \frac{g_{m}}{\left(C_{gs} + C_{gd}\right)}$$

MOSFET short-circuit current gain, $\beta_{sc}(j\omega)$, cont.



MOSFET short-circuit current gain, $\beta_{sc}(j\omega)$, cont.



Lessons: Bias at well above V_T ; make L small, use n-channel.

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An aside: looking back at CMOS gate delays

<u>CMOS</u>: switching speed; minimum cycle time (from Lec. 15) <u>Gate delay/minimum cycle time</u>:

For MOSFETs operating in strong inversion, no velocity saturation:

$$\tau_{MinCycle} = \frac{12nL_{\min}^2 V_{DD}}{\mu_e [V_{DD} - V_{Tn}]^2}$$

Comparing this to the channel transit time:

$$\tau_{ChTransit} = \frac{L_{\min}}{\overline{s}_{e,Ch}} = \frac{L_{\min}}{\mu_e E_{Ch}} = \frac{L_{\min}}{\mu_e (V_{DD} - V_{Tn})/L_{\min}}$$

We see that the cycle time is a multiple of the transit time:

$$\tau_{Min\,Cycle} = \frac{12nV_{DD}}{\left(V_{DD} - V_{Tn}\right)} \tau_{Channel\,Transit} = n' \tau_{Channel\,Transit}$$

When <u>velocity saturation</u> dominated, we found the same thing:

$$\tau_{Min.Cycle} \propto \frac{L_{min}V_{DD}}{s_{sat}[V_{DD} - V_{Tn}]} = n'\tau_{ChanTransit}$$
 where $\tau_{ChanTransit} = \frac{L}{s_{sat}}$

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Intrinsic ω_{HI} 's for MOSFETs - $\beta_{sc}(j\omega)$ and ω_t w. velocity saturation

What about the intrinsic ω_{HI} of a MOSFET operating with full velocity saturation?

The basic result is unchanged; we still have:

$$\omega_t = \sqrt{\frac{g_m^2}{\left[\left(C_{gs} + C_{gd}\right)^2 - C_{gd}^2\right]}} \approx \frac{g_m}{\left(C_{gs} + C_{gd}\right)} \approx \frac{g_m}{C_{gs}}$$

However, now g_m is different:

$$g_m = W s_{sat} C_{ox}^*$$

With this we have:

$$\omega_t \approx \frac{g_m}{C_{gs}} = \frac{W s_{sat} C_{ox}^*}{W L C_{ox}^*} = \frac{s_{sat}}{L} = \frac{1}{\tau_{ch}}$$

In the case where <u>velocity saturation</u> dominates, we once again find that it is the channel transit time that is the ultimate limit.

Do you care to speculate on the intrinsic ω_{HI} of a BJT?

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Intrinsic ω_{HI} 's for BJTs - short-circuit current gain



The common-emitter short-circuit current gain is:

$$\beta_{sc}(j\omega) = \frac{i_c(j\omega)}{i_b(j\omega)} = \frac{g_m - j\omega C_{\mu}}{\left[g_{\pi} + j\omega \left(C_{\pi} + C_{\mu}\right)\right]}$$

there is one pole, call it ω_p , and one zero, ω_z :

$$\omega_p = \frac{g_{\pi}}{\left(C_{\pi} + C_{\mu}\right)}, \qquad \qquad \omega_z = \frac{g_m}{C_{\mu}}$$

Of these two, ω_p is much smaller and this is the 3dB point of the common-emitter short-circuit current gain. We give it the name ω_{β} : $\omega_{\beta} = \frac{g_{\pi}}{\sqrt{1-y_{\mu}}}$

$$\omega_{\beta} = \frac{g_{\pi}}{\left(C_{\pi} + C_{\mu}\right)}$$

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Intrinsic ω_{HI} 's for BJTs - short-circuit current gain, cont.



The magnitude of β_{sc} decreases above ω_{b} , but it is still greater than one initially:

$$\beta_{sc}(j\omega) = \sqrt{\frac{g_m^2 + \omega^2 C_\mu^2}{\left[g_\pi^2 + \omega^2 \left(C_\pi + C_\mu\right)^2\right]}}$$

The transistor is useful until $|\beta_{sc}|$ is less than one. The frequency at which this occurs is called ω_t . Setting = 1 and solving for ω_t yields:

$$\omega_{t} = \sqrt{\frac{\left(g_{\pi}^{2} + g_{m}^{2}\right)}{\left[\left(C_{\pi} + C_{\mu}\right)^{2} - C_{\mu}^{2}\right]}} \approx \frac{g_{m}}{\left(C_{\pi} + C_{\mu}\right)}$$

BJT short-circuit current gain, $\beta_{sc}(j\omega)$, cont.



BJT short-circuit current gain, $\beta_{sc}(j\omega)$, cont.



Lessons: Bias at large I_c ; make w_B small, use npn.

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Lecture 24 - Intrinsic Limits of Transistor Speed - Summary

- Intrinsic high frequency limits for transistors General approach: short-circuit current gains
- Limits for MOSFETs:

Metric - CS short-circuit current unity gain pt: $\omega_T = g_m / [(C_{gs} + C_{gd})^2 - C_{gd}^2]^{1/2}$ ω_T is approximately $g_m / C_{gs} = 3\mu_e (V_{GS} - V_T)/2L^2$

 $g_{m} = (W/L)\mu_{e}C_{ox}^{*}(V_{GS}-V_{T}) \text{ and } C_{gs} = (2/3)WLC_{ox}^{*}$

so
$$\omega_{\rm T} \approx 3\mu_{\rm e}(V_{\rm GS}-V_{\rm T})/2L^2 = 1/\tau_{\rm ch}$$

minimize L (win as L²; as L in velocity saturation)

use n-channel rather than p-channel $(\mu_e >> \mu_h)$

• Limits for BJTs:

6.012 Microelectronic Devices and Circuits Fall 2009

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