### 6.012 - Microelectronic Devices and Circuits - Fall 2009

## Inverter Switching Transient Analysis



The generic inverter stage (a) with the non-linear charge store shown explicitly.
The charging cycle (b), and the discharging cycle (c).
The charge store will in general be a non-linear function of the output voltage; so too are the currents. Thus the differential equations we must solve are
and

$$
\text { Charging: } \quad \mathrm{dq}_{\mathrm{N}}(\mathrm{vOUT}) / \mathrm{dt}=\mathrm{i}_{\mathrm{CH}}(\text { voUT }),
$$

Discharging: $\quad \mathrm{dq}_{\mathrm{N}}\left(\mathrm{v}_{\text {OUT }}\right) / \mathrm{dt}=\mathrm{i}_{\mathrm{DCH}}\left(\mathrm{v}_{\mathrm{OUT}}\right)$.

These are in general very complicated and difficult to solve by any means. If, however, the charge store can be modeled as a linear capacitor, $\mathrm{C}_{\mathrm{L}}$ (i.e., $\mathrm{q}_{\mathrm{N}} \approx \mathrm{C}_{\mathrm{L}}$ voUT), as illustrated below, then we can write,

$$
\text { Charging: } \quad \mathrm{dvoUT} / \mathrm{dt}=\mathrm{i}_{\mathrm{CH}}(\text { voUT }) / \mathrm{C}_{\mathrm{L}}
$$

and

$$
\text { Discharging: } \quad d v o u t / d t=i_{D C H}(v o U T) / C_{L}
$$

These are now differential equations for $\operatorname{vOUT}(t)$ that we should at least be able to solve numerically, if we can not do so analytically. They also show us the value of knowing the size and shape of $\mathrm{i}_{\mathrm{CH}}$ and $\mathrm{i}_{\mathrm{DCH}}$. (See Figure 6.14 in the course text, and the discussion accompanying it, for more on this topic).


Charging (a) and discharging (b) cycles with a linear load capacitor and zero static load current. Note that for MOS inverters the static current into the stage load, isL (voUT), is zero.

Finally, if the charge store can be modeled as a linear capacitor and the charging and discharging currents can also be approximated as being constant, then

$$
\tau_{\mathrm{LO} \rightarrow \mathrm{HI}} \approx \mathrm{C}_{\mathrm{L}}\left(\mathrm{~V}_{\mathrm{HI}}-\mathrm{V}_{\mathrm{LO}}\right) / \mathrm{I}_{\mathrm{CH}}
$$

and

$$
\tau_{\mathrm{HI} \rightarrow \mathrm{LO}} \approx \mathrm{C}_{\mathrm{L}}\left(\mathrm{~V}_{\mathrm{HI}}-\mathrm{V}_{\mathrm{LO}}\right) / \mathrm{I}_{\mathrm{DCH}}
$$

We will find that we can use such an approximation to advantage when we are analyzing CMOS inverters.

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