Massachusetts Institute of Technology 6.101 Analog Electronics Lab Spring 2007 Problem Set 2 Due Wednesday, February 28, 2007

Refer to Chapters 2 and 5 of *Circuit Analysis and Design*, 3rd *Edition* by Donald Neamen for text that supports this problem set. Remember to use 5% standard resistor values. Assume V_T=26mV

Problem 1. Neamen 5.27 (2nd ed: 3.16)

Problem 2. This problem refers to Figure 1. You are told that V_A is set so that $V_{OUT} = 50 \text{mV}$. If $v_a = 6 \sin(100 \text{t}) \text{ mV}$, then what is v_{Out} ? What is v_{OUT} ?

Problem 3. This problem refers to Figure 2.

- (a) Choose R so that the transistor is biased with $I_C = 4mA$, assuming $V_{BE} = 0.6V$, and β is large. Remember to use a standard value.
- (b) You get a really bad transistor with β =10. If you use the design from part (a), what will I_C be, assuming V_{BE} = 0.6V?

Problem 4. Neamen 5.42 (2nd ed: 3.32)

Problem 5.

- (a) It is often the case the DC bias stability is achieved by placing a resistor at the emitter connection of a BJT (for example, this is done in Figure 2 with a 100ohm resistor). However, this resistance drastically decreases the overall gain of Common Emitter circuits. If our input is a small signal AC wave, what can be added to the emitter connection to allow for higher values of gain while not affecting the DC bias stability of the circuit?
 - (b) What determines the Q-point when doing load line analysis? What factors should be considered when deciding on a Q-point? What are the x and y intercepts of the load line?

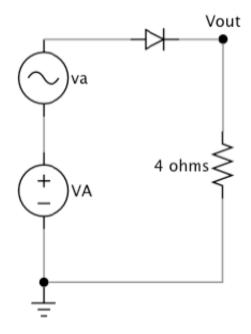


Figure 1: Figure for Problem 2

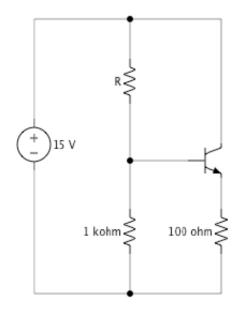


Figure 2: Figure for Problem 3