

**MASSACHUSETTS INSTITUTE OF TECHNOLOGY**  
**Department of Electrical Engineering and Computer Sciences**

**Introductory Digital Systems Lab (6.111)**

**Quiz #1 - Spring 2003**

Prof. Anantha Chandrakasan and Prof. Don Troxel

**Student Name:** \_\_\_\_\_

Problem 1 (40 Points): \_\_\_\_\_

Problem 2 (42 Points): \_\_\_\_\_

Problem 3 (18 Points): \_\_\_\_\_

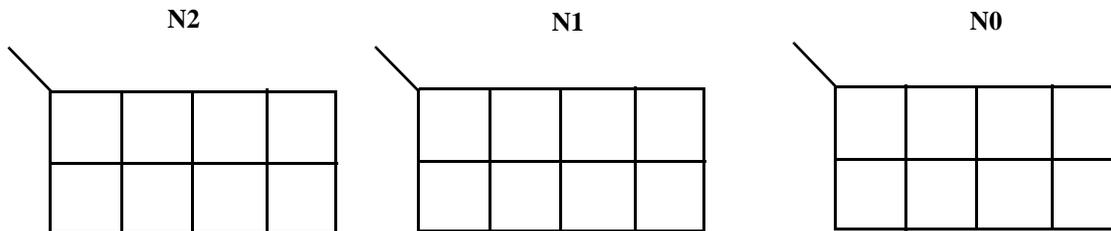
Total (100 Points): \_\_\_\_\_

**Problem 1: Counters**

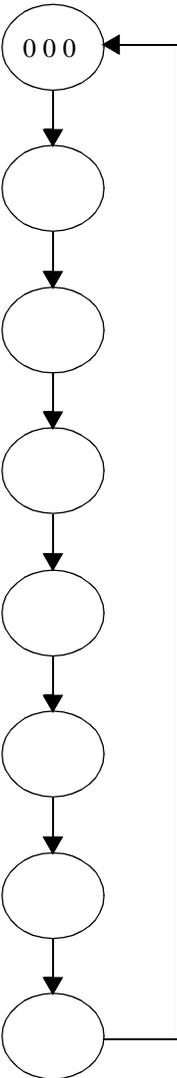
Consider the following state transition table for a counter. Q2, Q1 and Q0 represent the current state of the counter and N2, N1 and N0 represent the next counter state.

Q2	Q1	Q0	N2	N1	N0
0	0	0	0	0	1
0	0	1	0	1	1
0	1	0	1	1	0
0	1	1	0	1	0
1	0	0	0	0	0
1	0	1	1	0	0
1	1	0	1	1	1
1	1	1	1	0	1

(a) Use K-maps to derive the MSP expressions for N2, N1 and N0 as a function of Q2, Q1 and Q0. (12 points)

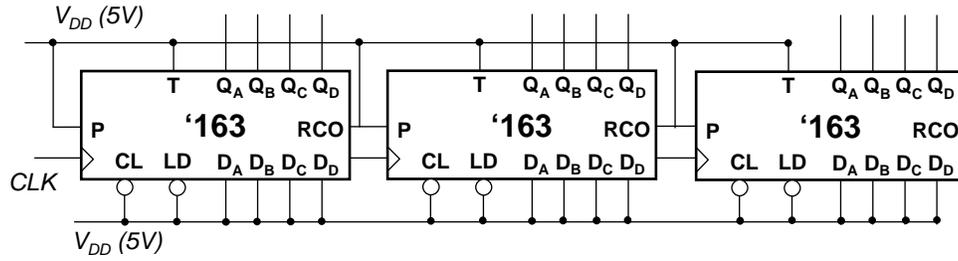


(b) Draw the state transition diagram for the counter in part (a) starting with state 0 (states should be labeled Q2 Q1 Q0). (4 points)



(c) Implement the counter specified in part (a) using three T-Flip Flops (recall that a T-FF has a Toggle input and a Q output). Represent the functions T2, T1 and T0 as a function of Q2, Q1 and Q0 in a standard sum-of-products expression (but do not minimize). **(12 points)**

(d) Consider the following 12-bit counter implementation using three 74163 counters. Describe the key problem with this implementation and propose a fix. (6 points)



(e) Briefly explain three major differences between a 74163 and a 74393 counter. (6 points)

- 1.
- 2.
- 3.

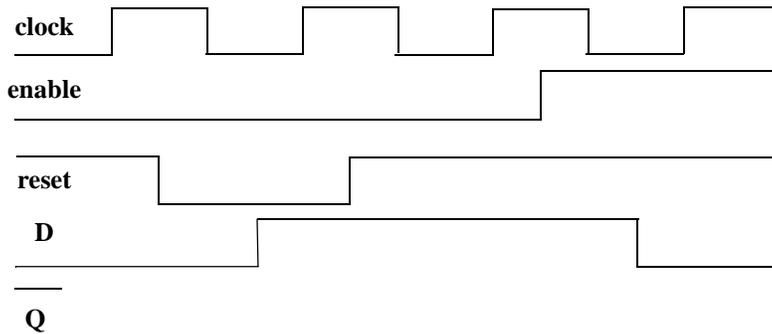
**Problem 2: VHDL of Sequential Circuits**

(a) Complete the timing diagram for the following piece of code. Assume Q starts at 1 and that Q is a signal. Assume that all delays are negligible. (8 points)

```

process (reset, enable, clock, D)
  if (reset = '0') then
    Q <='0';
  elsif (enable = '1' and clock = '1') then
    Q <=D;
  else
    Q <=Q;
  end if;
end process;

```

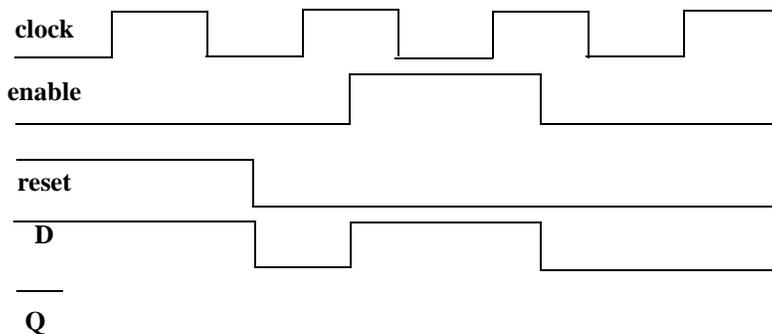


(b) Complete the timing diagram for the following piece of code. Assume Q starts at 1 and that Q is a signal. Assume that all delays are negligible. (8 points)

```

process (reset, clock)
  if (clock'event and clk = '0') then
    if (reset = '1') then
      Q <=0;
    elsif (enable = '1')
      Q<=D;
    end if;
  end if;
end process;

```



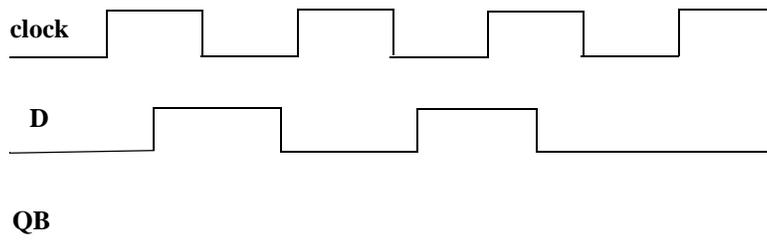
(c) Show the circuit diagram for the following piece of code. Assume that QA and QB are signals. (6 points)

```
process (clock)
if (clock'event and clock = '1')
    QA <=D;
    QB <=QA;
end if;
end process;
```

(d) Complete the timing diagram for the following piece of code. Assume QA and QB are signals. Assume QB is initially 0. Assume that all delays are negligible. (8 points)

```
process (clock, D)
if (clock = '0')
    QA <= D;
else
    QA <=QA;
end if;

if (clock = '1')
    QB<=QA;
else
    QB <=QB;
end if;
end process;
```



- (e) Complete the behavioral description in VHDL for a 74163 counter. The basic template is shown below -- fill in the necessary code to complete the description. Points won't be taken off for minor syntax errors (e.g., missing semicolon, misspelling, etc.) (12 points)

```
library ieee;  
use ieee.std_logic_1164.all;  
use ieee.std_logic_unsigned.all;
```

```
entity c74163 is  
  port (LDN, CLRN, P, T, CLK: in std_logic;  
        D : in std_logic_vector (3 downto 0);  
        count : out std_logic_vector (3 downto 0);  
        RCO : out std_logic);  
end c74163;
```

```
architecture behavior of c74163 is
```

```
  signal count_internal : std_logic_vector (3 downto 0);
```

```
begin
```

```
  RCO <=
```

```
  count <= count_internal;
```

```
  process (CLK)
```

```
    if (CLK'event and CLK = '1')
```

```
      if (CLRN =
```

```
        elsif (LDN =
```

```
          elsif (
```

```
            end if;
```

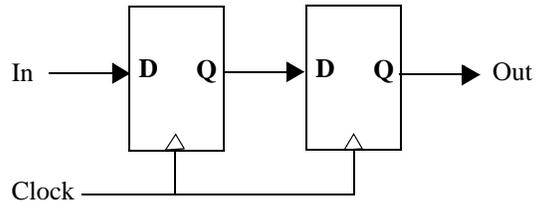
```
          end if;
```

```
        end process;
```

```
      end architecture behavior;
```

**Problem 3: Timing and Memory**

(a) Consider the following sequential circuit. Assume that the setup time for the edge-triggered register is 4ns, hold time is 3ns, the contamination delay is 1ns and propagation delay is 4ns. Identify the key problem with this circuit and propose a solution to fix it without modifying the clock. Assume that  $In$  is properly setup and held around the clock edge. **(8 points)**



(b) Consider the memory chip below (identical to the '6264, except for simplicity, the second enable pin is ignored and assumed to be always asserted). The chip is enabled when  $\overline{E}$  is low. Assume that both the minimum delay and propagation ( $t_{c-q}$ ) delay for the registers is 1ns. Assume that the time from the transition of the tri-state control input to output being driven to 0 or 1 or Z is 2ns. If either output\_enable\_b ( $\overline{G}$ ) or  $\overline{E}$  is pulled high, the memory chip tri-states the data bus after 4ns. **What is the minimum delay before the tristate control that must be added to avoid bus contention?** Hint: consider the simple timing shown below where interface transitions from a read access to a write access. (10 points)

