[SQUEAKING]

[RUSTLING]

[CLICKING]

PROFESSOR: So what I'd like to do today is talk about an entirely different class of switching power converter than we've talked about before. And we are going to-- we are going to look at-- for this class and next class, we're going to talk about switched capacitor converters. And that's *Principles of Power Electronics* chapter six.

Most converters introduce magnetics in them. They have some magnetic component in them. Why do you want it? Why do you want, say, an inductor or an inductive energy storage element in your converter? That's because if I put a voltage difference across it, from, say, an input voltage or an output voltage or two voltages, the inductor can instantaneously take that energy difference, absorb the voltage difference, absorb energy, then we can recover later. And that's the principle we operate on. And that's why almost all of these converters use magnetics or something that acts like a magnetic component.

On the other hand, sometimes, you can get away without any magnetic components, without any inductors in your circuit. And why might you want to do that? Well, because if you look at things that are on the scale of my thumb or something, some small element, the energy density you can achieve with a capacitor is orders of magnitude higher than the energy density you can achieve with a magnetic component at similar efficiencies and energy storage levels.

So capacitors are just extremely highly energy dense. So if I happen to have an application where I can get away with only capacitive energy storage, you can build a much smaller, more efficient converter. But that application space is limited. And we're going to get into why.

So switch capacitor converters are essentially-- to come back to their definition-- are essentially converters where I process all my energy using capacitors. And so I have capacitors and switches to do the energy throughput. I've brought a couple of examples with these. These are both kind of prototype designs. This one is a very small power, low power one. You'll see much of it on the front, and it has some energy storage capacitors on the back. This is another overall circuit, and this part over here is a switch capacitor converter of a certain type. So just to illustrate what we're talking about, you can take a look at these.

And so in order to illustrate their strengths and weaknesses, let's look at the simplest switch capacitor converter I can think of. And this is sometimes known as a 2-to-1 step-down converter, although we'll come back to why people call it that, but what its tradeoffs are.

So here's the idea. Suppose I had some input voltage from which I'm going to draw power, and I'm going to have a capacitor here. And this capacitor is my energy transfer capacitor. So here c, ic, and vc.

So, in this example I'm going to do, this element is where I'm storing the energy in the intermediate form to do this energy processing. So I'll have switches. And then I will have delivered to some output. And I'm going to call this c big-- this is like my filter capacitor. And then, here, I have some output current. This is the load current. And this is v out. So I'm going to have these two capacitors, these two switches, and these are phase one switches. Then I'm going to put two more switches in. I'm going to call these phase two switches. So here's one, one, and two, two.

And the idea here is that we're going to alternately take the switches that are labeled 1 and close them together. And then, at some other point in the cycle, we're going to open those switches and close the switches that are labeled 2 together. And what you're going to see-- one of the characteristics of switched capacitor converters, they tend to have a lot of switches. And, in fact, if you want high conversion ratios, they have lots of switches and lots of capacitors. We'll talk about that a little bit more.

So this beast in the box here, if you will-- I don't know, you can include the output capacitor, I suppose-- is the simplest switch capacitor or converter I can think of.

To analyze it, let me just simplify it. I'm going to think about this as a really big output capacitor. So for the moment, let me just replace them with a voltage source v out. So for my analysis, I'm going to simplify this just a little, and I'll say we have an input voltage v in. Here's my capacitor vc, ic, c, my two switches. I'm just going to replace this with an output voltage, v out. And then I'm going to have this is switch 1, switch 1, switch 2, and switch 2. And this is the circuit we're going to analyze.

So in state 1, I basically have these two switches closed. So in state 1, the converter looks like this-- v in. Our first switch is going to be on. I'll call that R switch. Then I'm going to have my capacitor. And then I'm going to have my second switch. And then that's going to go to the output. And in my second state, state 2-- the input's now going to be disconnected. But I am going to connect my capacitor through a resistor to the output, like this. Any questions about the two switch configurations?

Let's just, for simplicity, assume I'm going to flop back and forth at 50% duty cycle between these two states, although we'll see, in some cases, the duty cycle matters. In some cases it doesn't. All right, any questions? Yeah?

AUDIENCE: So in this case, we can't deal with [INAUDIBLE] switches. We have to think about the [INAUDIBLE].

PROFESSOR: It helps to think about the parasitic resistance because we were going to worry about how much energy we dissipate in the switches. But if I let the switch resistances go to 0, the answer doesn't change, actually. So, yeah, we'll come back to that point.

So let's think about this now in order to analyze this. What I'd like to do is focus on-- here, I have v in. Here's v in. Let me talk about the current i in going into v in. And here, I have v out. And here's i out. And then I have vc and ic. I guess I should have drawn this on the main circuit. So this is v in, i in, v out, i out, and vc, ic.

And what I would like to do is track the charge flowing through this converter. which is going to let me understand what its conversion ratio is. And analyzing any switch capacitor converter more or less comes down to the process I'm following. There are ways that we can organize it to do the general case.

But let's just think about this case. And what I'm going to think about is let's suppose that when I close the switches and I have some switch resistances, the values don't matter. But let's ask what does the final voltage of the capacitor end up at? So at the end of state 1, what I'm going to assume for my first analysis-- and this is what's known as the slow switching limit-- is that I close my switches, and this capacitor charges to some final value and then stops charging.

So what would be the final value of the capacitor in this state 1? So vc at the-- and state 1 at the end. What voltage would vc charge to? Has to be v in minus v out. And in state 2, at the end, correspondingly, vc has to go to v out. So the idea is if I looked at what vc was going to do, it's going to start off when I enter state 1-- or [INAUDIBLE] state 2 I'm going to be at v out. I'm going to flip my switches, and then vc is going to charge to v in minus v out. And I'm going to switch my switches. Then, vc is going to discharge in this case back to v out and it's going to repeat. That makes sense to everybody?

So I'm assuming-- and this is the slow switching limit-- that what my capacitor voltage is going to do versus time-- if this is state 1 and this is state 2, I'm going to basically-- my capacitor is going to charge from v out up to v in minus v out. And then it's going to charge from v in minus v out, down to v out, and it's going to do something like this with some Rc time constant.

And so I'm just assuming-- so this is going to-- at the end of state 1, it's going to v in minus v out. And then, in the next state, in state 2, it's going to charge to v out. So my only assumption is I'm going to-- each cycle, I'm going to charge up, I'm going to charge down, and I'm going to finish the charging. I'm going to let this Rc time constant go to where he's fully charged.

So let's think about how much charge I transfer in each component. In state 1, what do I have? Delta qc in state 1-- the amount of charge that gets put onto the capacitor in state 1. Well, what's that going to be? That's going to be equal to-- delta q is c delta v, which is going to be c times the change in voltage across state 1. He's starting at v out, and he's going up to v in minus v out. So it's going to be v in minus v out minus v out is going to be c times v in minus 2 v out.

So that's how much charge gets put on to this capacitor during state 1 in periodic steady state. Any questions about that? Because the rest of the analysis proceeds just like this. So I want to make sure people get what I'm calculating. NPSS-- I charge and discharge between two points. And I'm just saying how much charge went on to the capacitor in state 1, and that's it.

Well, how much charge went into the input in state 1? Well, the way I've defined it here, the input-- and I've defined here because the general analysis tend to do it this way-- is the current going in the capacitor is exactly the opposite of the current going into the input in state 1. So the current-- the charge into the input just has to be the opposite. This is going to be minus c v in minus 2 v out. And likewise, the charge that got transferred into the output during state 1 is exactly equal to the charge in the capacity that transferred onto the capacitor. And I get delta q out in state 1 is equal to c v in minus 2 v out. Does that make sense to everybody? Any questions?

Let's think about state 2. Delta q c-- how much charge goes on the capacitor in state 2 is equal to c delta v? Well, in state 2, I started at v in minus v out, and I ended at v out. So it's going to be v in minus v out, minus v out is what I'm going to get. But keep in mind that I could write this-- the charge that's going to-- he's going to end up at v out minus v in minus v out. So it's v out minus v in minus v out. It's 2 v out minus v in times c.

But I could write that as minus c times v in minus 2 v out. And the reason I'm going to write-- first of all, does everybody get what I just did? All I did was I just expressed it as a with a minus sign out here. I pulled the minus sign out here. Why did I pull the minus sign out here? Because I want to emphasize that this is going to be a negative net charge. Or another way I ought to think about it is, look, I'm running this converter back and forth between state 1 and state 2 in periodic steady state. What is the net charge that I'm going to transfer through the capacitor in periodic steady state? 0.

So that means that delta q c 1 is a charge transferred onto the capacitor in state 1 plus delta q, c 2, the charge transfer onto the capacitor in state 2-- better add to 0. And you can see that it does if I write it this way. It's c v in minus 2 v out plus minus c v in minus 2 v out. So they add to 0. So indeed, if I made the assumption that it's charged to its initial and final states, this does satisfy the periodic steady state requirements on the capacitor. Any questions about that? So let's just say-- what happens-- what's delta q in in state 2? Anybody tell me that? This is v in. This is i in. How much charge is transferred into the input in state 2?

AUDIENCE: None.

PROFESSOR: 0-- no charge transferred in the input. How much charge is transferred to the output in state 2? Well, this is-- let's be careful about signs here-- here's v out. Here's i out. The negative of the capacitor current is going into the output. So whatever charge went into the capacitor, the negative of that charge went into the output. So delta q out 2 must be positive c v in minus 2 v out. Does that make sense to everybody?

So what is the-- we know that the net total charge transferred on this energy storage capacitor in periodic steady state better be 0. But that's not true of the input or the output. So why don't we just find out what that is? We could then write delta q in is equal to q in state 1 plus delta q in in state 2 And if I just add those up, that's going to be 2 c v in minus 2 v out. And delta q out is going to be equal to delta q out in state 1 and delta q out in state 2. And if I add those up, it's going to be minus c v in minus 2 v out.

Now what's the current at the input on average? Yeah?

AUDIENCE: Are these flipped, [INAUDIBLE]?

PROFESSOR: Yes, thank you. How did I do that? Well, it's easier to do it this way. Thank you. Somebody's watching. So we have our input and output net charge. If I wanted to talk about the average current going to the input or the output averaged over a cycle, really, it's the charge divided by the period, or equivalently the charge times the switching frequency. So the local average or the average in periodic steady state, I could infer from this is that i in is equal to c times the switching frequency-- that's 1 over the period-- times v in minus 2 v out. And I should put my minus sign here. And that's this is the current going into the input. And likewise, i out is equal to 2 c f switch times v in minus 2 v out.

So if you look at this, the magnitude of i out is equal to 2 times the magnitude of i in. Why? Because what happens is, essentially-- and what's the deal with the minus sign? The minus sign is because I chose to define i in going this way. Had I defined it going this way, I'd have i out is equal to twice i in. But let's just worry about the magnitudes here.

So what's going on? In the first part of the cycle, I dump a certain amount of charge from the input to the output through the capacitor. I charge the capacitor up. So that's some amount of charge. In the second part of the cycle, this capacitor then dumps that same amount of charge into the output again. So the output gets twice the amount of charge as the input over the cycle. And then I go back to the next cycle and I repeat. So whatever the current coming in from-- coming into the converter from the input is exactly half the current going to the output by periodic steady state and charge balance on the capacitor. Any questions about that?

I should say that this is the defining feature of a switch capacitor converter. You will always have some rational relationship-- "rational" meaning an actual fraction-- relating the current from the input to the current on the output. Why? Because this is a very simple converter. We've got one capacitor that we're flipping around, but generally, you're going to be taking energy, storing charge from the input, doing something, and throwing it to the output. And those are always going to be related in some rational way. So that's what the core thing that a switch capacitor converter do-- is by charge balance is going to give you some concurrent conversion ratio between the input and the output that's fixed by the topology and the switching sequence.

What else can we say about this? Well, look at this relationship here. First of all, any questions about what got me to that? Yeah?

AUDIENCE: Is this assuming a 50% duty cycle?

PROFESSOR: That's a good question. So long as the intervals are such that I fully charge and fully discharge in each subinterval, in state 1 and state 2, the actual duty ratio doesn't matter in this mode of operation. So the only thing I've assumed is that I'm waiting long enough or in state 1 for the capacitor to get to its final voltage. And I'm waiting long enough in state 2 for the pastor to get to its final voltage. And as long as I've waited long enough in both states, what the actual fraction of bond times are doesn't matter. We'll come back to that shortly. Yeah?

AUDIENCE: I've got a question. This mode is called the slow switching [INAUDIBLE], right?

PROFESSOR: Yes.

AUDIENCE: And is that why we didn't include the [INAUDIBLE], like effect-- or those switches there are represented as resistors, so like the charge doesn't [INAUDIBLE]?

PROFESSOR: Well, no, it does. We've included the resistance. All I've said is the only thing you really need to know in this is where did the capacitor start in terms of its voltage and where did it end? And if you know that, then how much charge went into it. So we have actually included the effect of the resistances. It's those Rc charging things. If the resistances get small, I just make those Rc charging shorter.

AUDIENCE: I see, thanks. But wouldn't on-state and off-state voltages change, like wouldn't there be potential differences across the resistors?

PROFESSOR: Well, if I've assumed that the capacitor is fully charged, the voltage across this resistor went to 0 by the end. So the only assumption I've made is this capacitor charges. Once the capacitor current goes to 0, these voltage drops go to 0. We'll relax that assumption shortly.

So let me start from this relationship, and let me see if I can give you what the voltage relationship is. I've told you here, this is the current relationship of the converter. That's the fundamental thing that this converter does. Well, how are the input and output voltage related? Well, that's by this guy here. And I can rearrange this. So all I could do is maybe solve for v out. And if I solve this equation for v out, what I'm going to get is v out is equal to 1/2 of v in minus 1 over 4 f switch c times i out. This is an equivalent statement as this.

So what does that mean as in a practical matter? Well, let me create for you an equivalent circuit which does this same thing, So I told you, this is my converter. If I wanted a periodic steady state model for what this thing does, I have some input voltage. And then I have some load current connected to it that I'm going to call i out. What is the relationship between what's in there? It's defined by this. Well, here's a circuit that gives you this same relationship.

If I had an ideal 2-to-1 transformer, if this is v in, this voltage would be half v in because that's what the transformer does. And then I would have an equivalent resistance that would give me a voltage drop that was i out times 1 over 4 f switch. So I'd have an equivalent resistance of 1 over 4 f switch c. And I could put this whole thing in a box. And this is a DC equivalent model for how this thing behaves. In other words, this is v out. So this gives me the right relationships between v and v out. v out is half v in minus the voltage drop across this which is i out over 4 c f switch.

Likewise, if I have a current coming i out this way, the current this way through the ideal transformer is going to be exactly half of that. And that means the current this way is minus 1/2 i out. So this model in yellow here precisely captures the average circuit behavior of this system. Does that make sense to everybody?

Now this is this converter. Any other switch capacitor converter I want to model, you can model likewise as some ideal transformer relationship. This gives me my current conversion ratio. The input and the output current are related by the ideal transformer and then a voltage drop that's related by some equivalent resistance that's related to the energy transfer capacitors and the switching frequency. So the details will vary, but this model really captures what's going on.

Now if I said, well, what's a what's an-- if I wanted to just look back from the output and get Thevenin equivalent looking backwards, all I would see is-- another way to think about this is one half v in as a Thevenin voltage. And a Thevenin resistance would be Req is equal to 1 over 4 f switch c. This is a Thevenin equivalent model looking back into the switch capacitor converter from at least a DC. This is legitimate. Does that make sense to everybody?

Now we could say, what's the efficiency of the converter? Well, the efficiency is equal to v out i out divided by v in or minus v in i in. And since i out is twice minus i in, this would be equal to 2 times v out over v in. And we have an expression for v out right here. I could write this as also equal to v out over 1/2 v in. So to the extent that v out is smaller than half v in, the efficiency is less than 1.

Well, we can see that the output is smaller than half v in by whatever drop is across this resistor. So this model is actually useful for calculating-- this model is actually useful for calculating efficiency as well. And I could rewrite that. If I plug that in, what I would get is-- I could rewrite this as the efficiency simply is equal to 1 minus i out times Req over 1/2 v in. This is just illustrating if my load current goes to 0, the efficiency then goes to 1. If my load current gets really big, the output droops down. As my output gets really big, I get a bigger and bigger drop across this equivalent resistor, and my efficiency starts to decline. Does that make sense, everybody?

Now, when I'm saying this, what losses am I counting when I'm calculating this efficiency? The losses I'm counting are essentially the resistor losses, the losses in the switch resistances and in the capacitor, like any parasitics in the capacitor. It's what we would call capacitor charging loss. So the only loss I'm not counting-- if these switch have gate drives and the gate drive-- gate capacitance [INAUDIBLE] charge and discharge or other losses like that are internal to the switches, but the loss associated with the switches delivering current through to charge the capacitor and discharge the capacitor.

Now it doesn't matter-- you notice the switch resistance isn't even in here anywhere. It doesn't really matter what the switch resistance is. The only constraint I have is that I have to finish charging and discharging. And that's just because of-- you can do this by basically charging methods to find out the efficiency.

AUDIENCE: Could you say it again, where the power is being dissipated?

PROFESSOR: The power is being dissipated in-- if the only elements-- I mean, the power is being dissipated in any parasitic resistance in the charge and discharge path. So if I turn the switch on, it has some voltage drop across it, or if the capacitor has some parasitic resistance, it loses some energy in that. You say, well, what happens if I make my switch resistance go to 0? Well, all that happens is that the peak charging current gets higher. And it goes for a shorter time. And the total loss is the same thing.

So mathematically, it works out. The actual value of the resistance doesn't matter. It doesn't even matter if the resistance is linear or nonlinear, but you get the same net loss. So it's basically the loss that I incur in putting the charge on the capacitor and then taking the charge back off to the capacitor to the output-- that's the loss that's included. Yeah?

AUDIENCE: So if you use a smaller capacitor, which takes less time to charge your charge, can you see smaller losses?

PROFESSOR: Ah, so if I wanted to reduce my losses, let's go back and look at my efficiency characteristic. If I want smaller losses, I should make Req small. To make R equivalent small, I should make either c big or switching frequency big. And the notion is-- and we'll come back to this and we'll look at this next class-- it comes down to the amount I'm charging and discharging the parser. When I charge the capacitor over a small, tiny delta voltage, I don't lose much energy in doing it. And so if I want lower loss, it's a very great insight on your part. But if I want lower loss, I want to make the capacitor bigger, not smaller for a given load current.

So this model-- in fact, if I wanted, if I put a resistive load on here, the efficiency is exactly just the efficiency of a voltage divider. So this is a very good model. And the only thing that would vary if I model any other switch capacitor converter would be this transformer ratio, which relates to that perfect current conversion ratio we calculated, and what the exact value of this output resistance would look like, which is, again dictated by the losses. Questions?

So let's think about what other case I might consider. We said, OK, suppose I want to-- and by the way, why do we like these converters? Because they can be hyperefficient. If I go buy a really big capacitor here or I switch really fast, this equivalent resistance can be very small. And I can get an almost perfect 2-to-1 voltage conversion. And, in fact, people would call this thing a 2-to-1 step-down switch capacitor converter. Why? Because they're thinking of the voltage. Ideally speaking, if I make this resistance really small, I'm really just doing like an ideal transformer 2-to-1. And so people would call that a 2-to-1.

On the other hand, it's only approximately 2-to-1 because this is not 0. This is some finite value of resistance. What it is, is a 1-to-2 current converter-- switch capacitor or converter. And that relationship is precise. So what should people call this? They should call this a 1-to-2 current conversion-- switch capacitor converter. But that's not what they call it. They call it a 2-to-1 voltage converter because everybody likes to think about voltages. So it's just you're stuck with the-- you're stuck with what people call things, but maybe it's not fair.

So what do I get if I wanted to go up in performance? Suppose I want-- I should say, when would I want to use a switch capacitor converter? I'd want to use a switch capacitor converter-- for example, I have 5 volts and I need 2.5 volts. I want exactly half the voltage. Then, to the extent that I can make this equivalent resistance small, this is a great converter.

On the other hand, I wouldn't want to use this converter when my input voltage was 5 volts and my output voltage was 2 volts, because then my efficiency would be 2 over 2.5, which isn't that high. So switch capacitors or converters are very efficient when your voltage conversion ratio is very close to the inverse of your intrinsic current conversion ratio. And then their efficiency droops down outside of that range. Sometimes, actually, people use this and vary this equivalent resistor to give yourself a linear regulator kind of action too. So instead of linear regulating down from v in, you linear regulate down from half v in, so you get an advantage that way. But if you want to talk about pure switch mode operation, you're usually trying to make this very small.

How do I make that small? I either get big capacitors or I switch fast. Now there's an exception to what I said or a limit to what I said. This operation is all in what I've been calling the slow switching limit. This limit right here, where I'm fully charging and fully discharging, suppose I want to get higher efficiency. And I'm forgetting about gate losses and capacitor discharge losses and stuff inside the switches. I'm just talking about the charge transfer losses. I can switch faster and faster and faster.

That output resistance keeps drooping, keeps getting smaller, and that's better. But eventually, I get to the point where if I increase my switching frequency-- suppose I just keep each time period half, that this time period is going to get so short that my capacitor doesn't fully charge up. And he doesn't fully charge down. If I keep pushing my switching frequency up enough, I'm going to violate the assumption under which I did this analysis. The extreme limit of that is the capacitor sitting close to some voltage, and he only charges up and down a little.

So, in other words, suppose I made my time scale really short, and I will have-- here's state 1 and here's state 2. And, in state 1, he just does this. He charges a tiny bit, which is part of a much bigger charge. And then to state 2, he discharges just a tiny bit, which is part of a much longer time charge, So I can almost think in the fast-switching limit-- vc is almost constant. I don't have enough time to charge up or down substantially. The delta voltage I get is nowhere near the full swing.

And I can just start to think about the capacitor as being a constant voltage. But it's a special constant voltage because, nonetheless, if I'm going to be in periodic steady state, however much he charges in the first state must balance the amount of discharges in the second state that I haven't gotten around that kind of rule. But nonetheless, we can think about this fast switching limit as the capacitor voltage almost becoming constant.

So let's think about what would a converter do in the fast switching limit in the FSL in state-- so let me just think about-- I'm going to now mentally replace this capacitor with just a fixed voltage, vc. And in this other state, he's also going to be a fixed voltage vc. And the only thing I need is the net charge that goes into vc over a cycle to be 0.

So how much charge do I transfer in state 1? And I'm going to do FSL with 50% duty ratio. In other words, I'm going to assume that in state 1, I spend half a period. In state 2, I'm going to spend half a period because in the FSL, the fast switching limit, how much time I spend in the two adjacent states matters. But let's just assume I'm going to spend half in each state for purposes of this analysis.

So in state 1, what do I get for delta qc 1? Well, delta qc 1 is going to be what? I'm going to say, all right, if he's a constant voltage, I'm going to get a current that's going to be v in minus vc minus v out divided by 2 R switch. That's the current in state 1. So that's going to be v in minus vc minus v out divided by 2 R switch. And that's going to happen for how long? That's going to happen for one half t. Or I could write that as 1 over 2 f switch, This is times half a period.

What is delta q in 1 look like? That's just going to be minus delta qc 1. And what's delta q in 2 look like? That's just going to be equal to delta qc 1. In other words, all I'm saying is that here, the input got the negative of the charge of the capacitor, and the output got the charge that went through the capacitor. Makes sense to everybody?

If I do this for state 2, what I'm going to get is delta qc 2 is simply going to be what? It's going to be v out minus vc over 2 R switch. Or it's going to be v out minus vc over 2 R switch is going to be minus vc minus v out over 2 R switch times 1 over 2 f switch. Delta q in 2 is going to be 0. And delta q out 2 is going to be equal to the negative of this, which is going to be minus delta qc 1. Does that make sense, everybody?

AUDIENCE: [INAUDIBLE]

PROFESSOR: Yes. That's what happens when I rush. Thank you. What constraint do I get off of this? Well, what I need is delta qc of 1 plus delta qc of 2 have to add up to 0. I mean, that's a constraint for periodic steady state. So what I get is for PSS, what I get is delta qc of 1 plus delta qc 2 is equal to 0, which gives me-- I can ignore the 1 over 4 f switch R switch.

That gives me v in minus vc minus v out plus v out minus vc plus v out minus vc is equal to 0. And what this gives me is that vc is going to be half v in. So in periodic steady state, I'm going to be charging discharging the capacitor, but he's going to sit at an average value of half v in.

I can then go and plug this value back in-- and I'm kind of running out of time here. I can go plug this back in and find q out 1 and q in 1. I can do the same game I do over here. And if you do that calculation, it's pretty easy. I can calculate i out as being the sum of q 1 and q in and q out. And what I get is v out is equal to 1/2 v in minus 2 R switch i out. So it's of the exact same format that I had up here.

So here, I get this in the SSL. And in the FSL-- I think should use a different color-- in the FSL. Req is simply equal to 2 R switch. Well, that actually kind of feels good in some sense because if you think about it, in either of these two states, I'm always dumping current through two switches. So half the time I'm doing in this configuration, half the time in that configuration, but if I think of a capacitor current as being of a plus and minus square wave of current, the input current is constant coming here, and the output current-- I'm sorry, the input current is a pulse square root. The output current is kind of constant. But the point is I'm always putting my charging and discharging current through two switch resistances, so it's not maybe surprising that I get down to this equivalent resistance being two switch resistances.

So what happens in the real world is if I have a switch capacitor converter and I say I'm going to have this model for its behavior, all I'm going to get is if I plotted R equivalent on a log scale versus switching frequency on a log scale, what I'm going to get is something that falls linearly. This is 1 over 4 c f switch. And then he's going to have some minimum value, which is 2 R switch. And the actual value you're going to get is going to do something like this.

So there's kind of some limiting efficiency you can get to. Well, if I'm charging through two switches all the time, I got to eat the on-state loss of those switches. I mean, I can't have 100% efficiency. But if I'm using 10 milliohm switches, maybe that's pretty damn low. So essentially, what I would tend to do is keep turning up the switching frequency until I get down to this regime where turning it up any more doesn't reduce my output resistance because, at that point, there are other losses, like gate drive losses and stuff, which get worse with frequency. So I ought to just go high enough that I can get to very high efficiencies.

And the result of this is if what I want is a fixed conversion ratio close to this, I can get extraordinarily high efficiencies in power densities. If I deviate the voltage conversion ratio away from that, then the efficiency starts to droop. But for what they're good at, switch capacitor converters are very hard to beat. And if I was to come back and analyze any other switch capacitor converter, it's the same deal. It's some charge transfer analysis through the different capacitors. And I use charge balance, and you can work that out to being a current conversion ratio and then some equivalent resistance with a slow switching limit and a fast switching limit.

We'll take this up again next class. But are there any final questions? Yeah?

AUDIENCE: Now that you're switching quickly, can the duty ratio change the conversion ratio?

PROFESSOR: Well, yes, but only through the action of essentially what this resistance is. So you can make the-- for any given converter, there's a duty ratio that will give you the lowest output resistance. Even in slow switching limit, you can change the conversion ratio, but you're doing it through a resistive drop. It's sort of like you have an ideal transformer and then a linear regulator kind of thing. So you can always use switching frequency and fast switching limit duty ratio to change the conversion ratio, but not in a perfectly efficient sense-- for the voltage conversion ratio. All right, great. We'll pick this up next class.