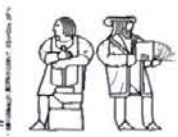

MASSACHUSETTS INSTITUTE OF TECHNOLOGY

DEPARTMENT OF ELECTRICAL ENGINEERING AND COMPUTER SCIENCE

6.622 Power Electronics Assessment #2

Due: Thursday March 9, 2023 at 11:00 pm (Cambridge time)

YOUR NAME Solutions

YOUR KERBEROS ID

General Instructions:

1. You must complete this assessment on your own with no consultation or discussion with any other person, excepting 6.622 staff, of whom you may ask clarifying questions. Do not discuss your solutions with anyone until the solutions have been released.

2. You may use a calculator and review the course lectures, notes and textbook (Principles of Power Electronics) when completing this assessment. Please do not use other computational tools or reference materials.

3. Please do all of your work in the space provided. In particular, try to do your work for each question within the boundaries of the question, or on the additional pages at the end of the uploaded document, clearly marking those pages to indicate what problem they relate to. Place the answer to each question within the appropriate answer box.

4. The assessment must be completed and uploaded by the indicated date/time to receive credit.

5. Please make sure to show all of your work. This is important both for you to receive credit for a correct answer and to receive partial credit when an answer is wrong or incomplete.

 Name:_____

Problem 1

Figure 1 shows a type of PWM dc-dc converter. The switch is turned on with duty ratio *D*. You may assume that it operates in continuous conduction mode, and that the capacitor voltages and inductor currents have small ripple.

a. Please find the steady-state voltage V_{C1} on capacitor C_1 in terms of one or more of V_1, V_2, and *D*.

b. What is the steady-state voltage conversion ratio V_2/V_1 of this topology as a function of switch duty ratio *D*?

c. What polarities of voltage V_1 are permissible in this particular implementation (i.e, $V_1 > 0$ only, $V_1 < 0$ only, or either polarity)? Why?

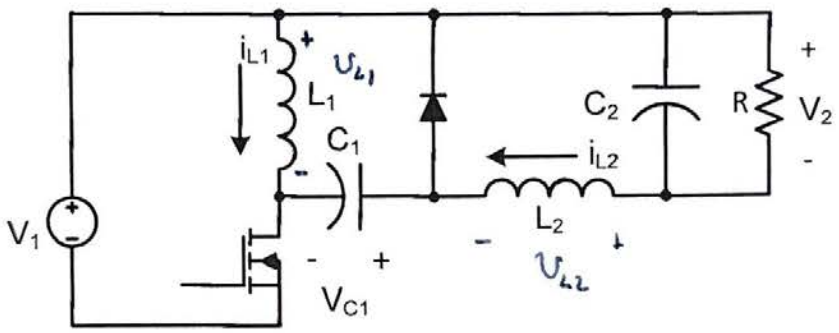

Figure 1 A PWM dc-dc converter.

(a) avg. KVL $\quad \langle v_{C1}\rangle + \langle v_{L2}\rangle + \langle v_2\rangle - \langle v_{L1}\rangle = 0 \quad$ where $\langle v_{L1}\rangle = \langle v_{L2}\rangle = 0$ in PSS

($\langle v_{L2}\rangle \to 0$, $\langle v_{L1}\rangle \to 0$)

$\therefore \boxed{V_{C1} = -V_2}$

(b) $\quad \langle v_{L2}\rangle = DT(V_1 - V_2 - V_{C1}) + (1-D)T(-V_2) = 0$ in PSS

$\therefore \; DV_1 = (1-D)V_2 \quad \Rightarrow \boxed{\frac{V_2}{V_1} = \frac{D}{1-D}}$

(c) Because of body diode of MOSFET and $\langle v_{L1}\rangle = 0$, only $V_1 > 0$ is allowed

Note: This is the "common-positives" version of the "zeta" or "inverse sepic" converter

 Name:_____

(a) $V_{C1} = -V_2$ or $-\frac{D}{1-D}V_1$

(b) $V_2/V_1 = \frac{D}{1-D}$

(c) circle one: ($V_1 > 0$ only) $V_1 < 0$ only either polarity
Explanation:
Power mosfet can only support +ve V_1

6.622 Power Electronics

Spring 2023