6.622 Power Electronics Assessment #2

Due: Thursday March 9, 2023 at 11:00 pm (Cambridge time)

YOUR NAME

Solutions

YOUR KERBEROS ID

General Instructions:

1. You must complete this assessment on your own with no consultation or discussion with any other person, excepting 6.622 staff, of whom you may ask clarifying questions. Do not discuss your solutions with anyone until the solutions have been released.

2. You may use a calculator and review the course lectures, notes and textbook (Principles of Power Electronics) when completing this assessment. Please do not use other computational tools or reference materials.

3. Please do all of your work in the space provided. In particular, try to do your work for each question within the boundaries of the question, or on the additional pages at the end of the uploaded document, clearly marking those pages to indicate what problem they relate to. Place the answer to each question within the appropriate answer box.

4. The assessment must be completed and uploaded by the indicated date/time to receive credit.

5. Please make sure to show all of your work. This is important both for you to receive credit for a correct answer and to receive partial credit when an answer is wrong or incomplete.
Problem 1

Figure 1 shows a type of PWM dc-dc converter. The switch is turned on with duty ratio $D$. You may assume that it operates in continuous conduction mode, and that the capacitor voltages and inductor currents have small ripple.

a. Please find the steady-state voltage $V_{C1}$ on capacitor $C_1$ in terms of one or more of $V_1, V_2$, and $D$.

b. What is the steady-state voltage conversion ratio $V_2/V_1$ of this topology as a function of switch duty ratio $D$?

c. What polarities of voltage $V_1$ are permissible in this particular implementation (i.e., $V_1 > 0$ only, $V_1 < 0$ only, or either polarity)? Why?

![PWM dc-dc converter circuit](image)

**Figure 1** A PWM dc-dc converter.

(a) avg. KVL \[ <V_{C1}> + <V_{L2}> + <V_2> - <V_1> = 0 \]

\[ \therefore <V_{C1}> = -<V_2> \]

(b) \[ <V_{L2}> = DT(V_1 - V_2 - V_{C1}) + (1-D)0-V_2 = 0 \] in PSS

\[ \therefore DV_1 = (1-D)V_2 \]

\[ \frac{V_2}{V_1} = \frac{D}{1-D} \]

(c) Because of body diode of MOSFET and $<V_{Li}> = 0$, only $V_1 > 0$ is allowed.

Note: This is the "common-positives" version of the "Beta" or "inversesepic" converter.
(a) \[ V_{C1} = -V_2 \quad \text{or} \quad -\frac{D}{1-D}V_1 \]

(b) \[ \frac{V_2}{V_1} = \frac{D}{1-D} \]

(c) circle one: \( V_1 > 0 \) only \( V_1 < 0 \) only either polarity

Explanation:
Power mosfet can only support +ve \( V_1 \)
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