

DEPARTMENT OF ELECTRICAL ENGINEERING AND COMPUTER SCIENCE

6.622 Power Electronics Assessment #6

Due: Thursday April 13, 2023 at 11:00 pm (Cambridge time)

YOUR NAME

YOUR KERBEROS ID

General Instructions:

- 1. You must complete this assessment on your own with no consultation or discussion with any other person, excepting 6.622 staff, of whom you may ask clarifying questions. Do not discuss your solutions with anyone until the solutions have been released.
- 2. You may use a calculator and review the course lectures, handouts, notes, textbook (Principles of Power Electronics) and other materials provided for the course on Canvas when completing this assessment. Please do not use other computational tools or reference materials.
- 3. Please do all of your work in the space provided. In particular, try to do your work for each question within the boundaries of the question, or on the additional pages at the end of the uploaded document, clearly marking those pages to indicate what problem they relate to. Place the answer to each question within the appropriate answer box.
- 4. The assessment must be completed and uploaded by the indicated date/time to receive credit.
- 5. Please make sure to show all of your work. This is important both for you to receive credit for a correct answer and to receive partial credit when an answer is wrong or incomplete.

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Problem 1

Figure 1 shows a simplified model of a current-source inverter. The current source is usually realized as a large inductor in series with a voltage source. You may treat the transformer as ideal.

(a) How would one control the switches of the inverter such that the ac current i_L into the transformer is *half-wave symmetric, odd in time and has no third harmonic* while operating each of the switches once per ac cycle? Sketch the current iL into the transformer primary (including switching angles) over a cycle for $-\pi < \omega t < \pi$ and indicate the switch states on your sketch.





i_L and switch states

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(b) Considering the case $I_{dc} > 0$, propose a switch implementation for switches S_1 to S_4 .

Inverter with switches S₁-S₄ implemented

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(Additional Work)

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