6.622 Power Electronics

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Lecture 15 - Switching losses and snubbers

1 Review



Practical switches Finite time for turn on and turn off

On-state: a voltage drop of a resistor

Off-state: leakage current

Parasitics: include a parallel capacitor, may include an anti-parallel diode \Rightarrow non-zero loss including conduction loss, switching loss (snubbers), gating loss, other losses On-state: a voltage drop

incontrolled half-controlled controller Disde read SCR 16B DCIDC leture Min : can block can block +2 carr +1 certr GAN HEMT on-state Mastel resistor a an.

2 Semiconductor losses (back of the envelope)

Example buck converter:



Device conduction losses:

 $\overline{\text{MOSFETS look resistor } P_{FET,cond} \approx i_{sw,rms}^2 R_{dson} = (I_L^2 D) R_{ds,on}}$ diodes look const drop $P_{d,cond} \approx \langle i_d \rangle V_{d,on} = (I_L D') V_{d,on}$ Device switching losses: occur as switches turn on and off

(Back of envelope: linear v,i transitions)





Turn on of MOSFET

Current in mosfet must rise to full value (diode current goes to 0) before diode turns off + block voltage

 t_f, t_r governed by devices and drivers

$$P_{sw,fet} \approx \left[\frac{1}{2}t_f I_L V_{in} + \frac{1}{2}t_r I_L V_{in}\right] f_{sw}$$

(Based on approximate linear transitions. Other losses and diode losses exist) Note: major loss component $\approx f_{sw}$. We want $f_{sw} \uparrow$ to make L, C \downarrow but losses ultimately limit us. We would like $t_r, t_f \downarrow$ to reduce switching loss, but other factor come into play:

1. Parasitics and overshoot

Lose capacitor energy $W = \frac{1}{2}C_p V_{in}^2$ on switch turn on



2. EMI

High $\frac{di}{dt}$, $\frac{dv}{dt}$ lead to EMI, may affect control circuits.

 $\begin{array}{l} \frac{di}{dt} \rightarrow \text{magnetic coupling } v = L_{\mu} \frac{di}{dt} \\ \frac{dv}{dt} \rightarrow \text{capacitive coupling } i = C \frac{dv}{dt} \end{array}$

3. Rate limits

Some devices (BJT, GTO, MCT, MOSFETS are immune to these effects) have limits on allowed $\frac{dv}{dt}, \frac{di}{dt}$ high $\frac{di}{dt} \rightarrow$ destory device on turn on high $\frac{dv}{dt} \rightarrow$ can trigger device back on

4. Safe operations area (SOA)

Limit maybe instantaneous power, "second breakdown", etc.



Some devices cannot sustain high <u>simultaneous</u> v,i.

3 Snubbers

- 1. Control switching losses
- 2. Reduce internal device dissipation

Suppose we placed a capacitor across the device during turn off:



 ${\cal I}_L$ diverted through C_s while switch turns off:

$$\begin{split} i_s w &= I_L (1 - \frac{t}{t_f}), 0 < t < t_f \\ i_c &= I_L \frac{t}{t_f}, 0 < t < t_f \\ v_c &= \frac{1}{C} \int_0^t i_c dt = \frac{I_L t^2}{2t_f C}, 0 < t < t_f \\ P_{diss,sw} &= i_{sw} \cdot v_c = I_L (1 - \frac{t}{t_f}) \cdot \frac{I_L T^2}{2t_f C}, 0 < t < t_f \end{split}$$

$$E_{diss} = \int_0^{t_f} i_{sw} \cdot v_c dt = \frac{I_L^2}{2t_f C} \int_0^{t_f} (t^2 - \frac{t^3}{t_f}) dt$$
$$E_{diss} = \frac{I_L^2}{2t_f C} (\frac{1}{3}t_f^3 - \frac{1}{4}t_f^3) = \frac{I_L^2 t_f^2}{24C}$$

We reduce device turn-off loss with the capacitor!

We also <u>store</u> energy in the capacitor $E_{stored} = \frac{1}{2}CV_{in}^2$

This is $\geq \frac{1}{2}C\frac{I_L^2 t_f^4}{4t_f^2 C^2} = \frac{I_L^2 t_f^2}{8C}$

So: we reduce device loss @ turn off as C \uparrow loss \downarrow

But: @ switch turn on, E_{stored} on cap gets dumped into switch!

- Could destroy switch!
- $\bullet\,$ dumped energy increases as C^

To build effective snubbers, we remove or recover the stored energy in some other fasion! e.g. RCD turn-off snubber



- During turn off, C_s is effectively in parallel w/ the switch
- when switch is on, capacitor stored energy is <u>slowly</u> dissipated in R (we need some on-time to complete the discharge)
- Snubber only operates during switching transitions
 - \Rightarrow switching locus improved (SOA, lower $\frac{dv}{dt}$)
 - \Rightarrow <u>device</u> loss reduced (but total device and resistor loss is typically higher!)

We can do similar things at device turn on!



Reduces <u>switch</u> turn on losses

- Total switch and resistor losses maybe higher with snubber
- does not reduce loss assocaited with parasitic capacitance across the switch
- controls switching locus (SOA, $\frac{di}{dt} \downarrow$)
- results in slightly increased switch voltage
- \rightarrow Could also describe gate drive techniques to get differential on/off transitions

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