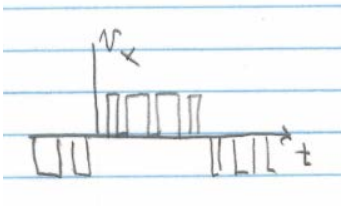
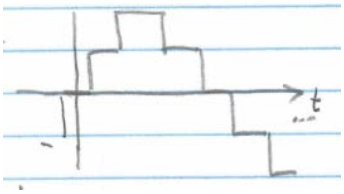
6.622 Power Electronics *Prof. David Perreault*

Lecture 19 - Inverters 3

We have seen that we can use harmonic elimination to eliminate low-frequency harmonic content at the expense of high switching frequency (with resulting undesired content at high frequency where it is easily filtered.



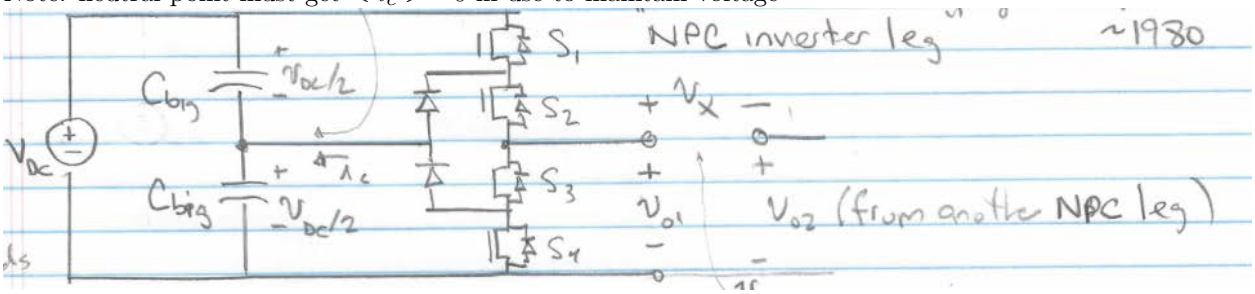
If we can add waveforms, we can also realize harmonic cancellation which cancels out some harmonic content, resulting in stepped waveforms looking closer to the target.



We can realize more sophisticated multi-level inverters that can directly synthesize more intermediate levels in an output waveform, facilitating nice harmonic cancelled output content.

Example: Neutral-point clamped inverters (also called "diode clamped" multi-level inverters). Active switches are sometimes used instead of diodes (Active Clamp NPC inverter, developed by Nabae 1980)

Note: neutral point must get $< i_c >= 0$ in use to maintain voltage



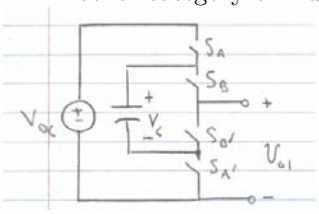
Note: ideally, each of $S_1 - S_4$ only needs block $\frac{1}{2}V_{DC}$ so we can have lower switch rating

Switch states	V_{01}
$S_1 S_2$	V_{DC}
$S_2 S_3$	$\frac{1}{2}V_{DC}$
$S_3 S_4$	0

We can synthesize 3 levels (0, $\frac{1}{2}V_{dc}, V_{dc}$) instead of 2 for a half-bridge (0, V_{dc}). So converters built with this kind of structure are called "3 level inverters", a subclass of "Multilevel inverters".

This is sometimes called a "3 level waveform" as each of V_{01}, V_{02} can take on 3 levels. We can do both elimination + cancellation with this capability!

Another category of multi-level inverters is the so-called "flying capacitor" approach:



"Flying capacitor multi-leveled inverter" or FCML inverter (Meynard 1992)

$S_A + S_{A'}$ switched oppositely
$S_B + S_{B'}$ switched oppositely
Control V_c to $\approx V_{DC}/2$

Switch state on	V_{01}
$S_A S_B$	V_{DC}
$S_A S_{B'}$	$V_{DC} - V_C \approx \frac{V_{DC}}{2}$
$S_{A'} S_B$	$V_C \approx \frac{V_{DC}}{2}$
$S_{A'} S_{B'}$	(1)

Notes:

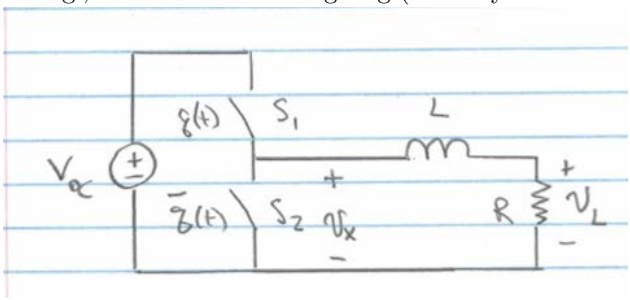
- If $V_C \approx V_{dc}/2$ each switch sees max $V_{dc}/2$
- we can charge or discharge C by which combination we choose for $V_{01} \approx V_{DC}/2 =¿$ can "balance" V_C
  - unlike the diode clamped approach, we can deliver dc current at V_{01} (can make dc-dc FCML converters)"
- Flying Capacitor + diode clamped converters are examples of "multilevel" Converters. This approach has become very common @ high power (and sometimes in low-voltage CMOS design!)
- Balancing of the intermediate voltage levels is always an issue.
- Each of these approaches can be extended to more intermediate levels ($\geq$7 levels used.)
- Device voltages are reduced compared to the full bus voltage but by how much depends upon balancing, startup, # of levels,...

1 "Sine Triangle PWM"

Suppose we can switch many times per cycle and/or would like the ability to synthesize an arbitrary waveform in real time.

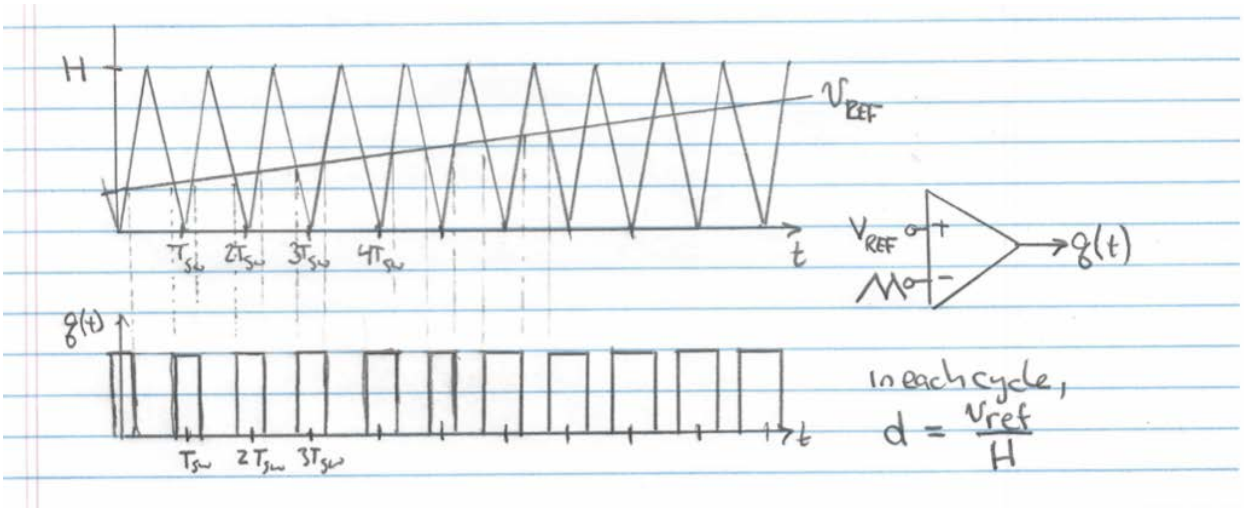
We can do such a synthesis using similar techniques as with PWM dc-dc converters, but with a varying reference command.

e.g., consider a half-bridge leg (like a synchronous buck converter):

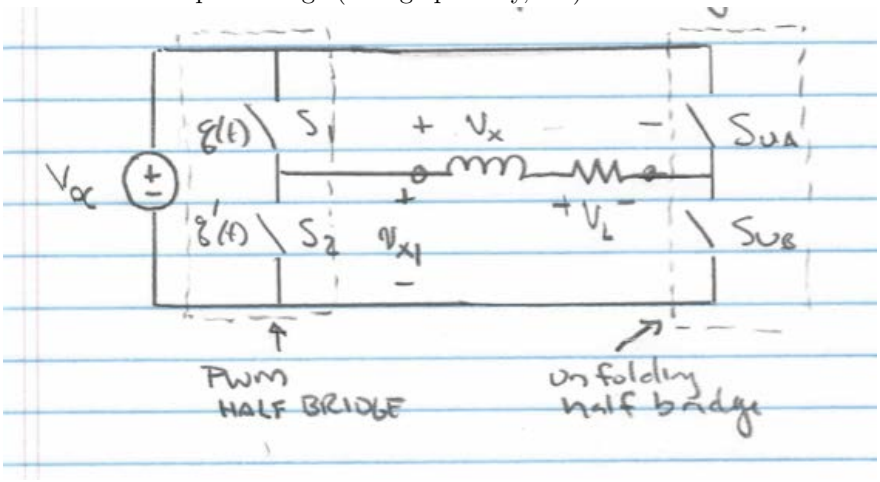


- If q(t) has duty cycle d $< V_x >= d \cdot V_{dc} =< V_L >$
- $w_{sw} = 2\pi f_{sw} = \frac{2\pi}{T_{sw}} >> \frac{R}{L}$
- If we vary d slowly wrt $w_c = \frac{R}{L}$ then v_L will track d(t) $\cdot V_{DC}$

We often implement such PWM based on a comparison between a triangle wave and a reference voltage. (We can use any Δ wave, e.g. a sawtooth, but the harmonic content is best with a balance Δ wave):



To get a bipolar output we could use one bridge leg to PWM synthesise $|V_{ref}|$ and another bridge leg to "unfold" the output voltage (change polarity, etc).



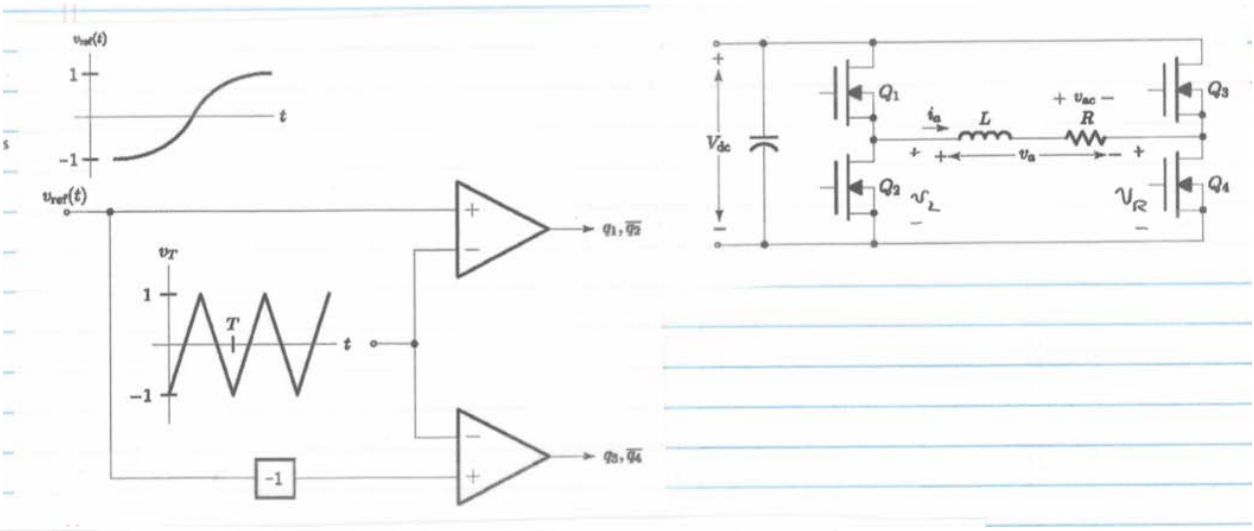
If $V_{ref} > 0$:

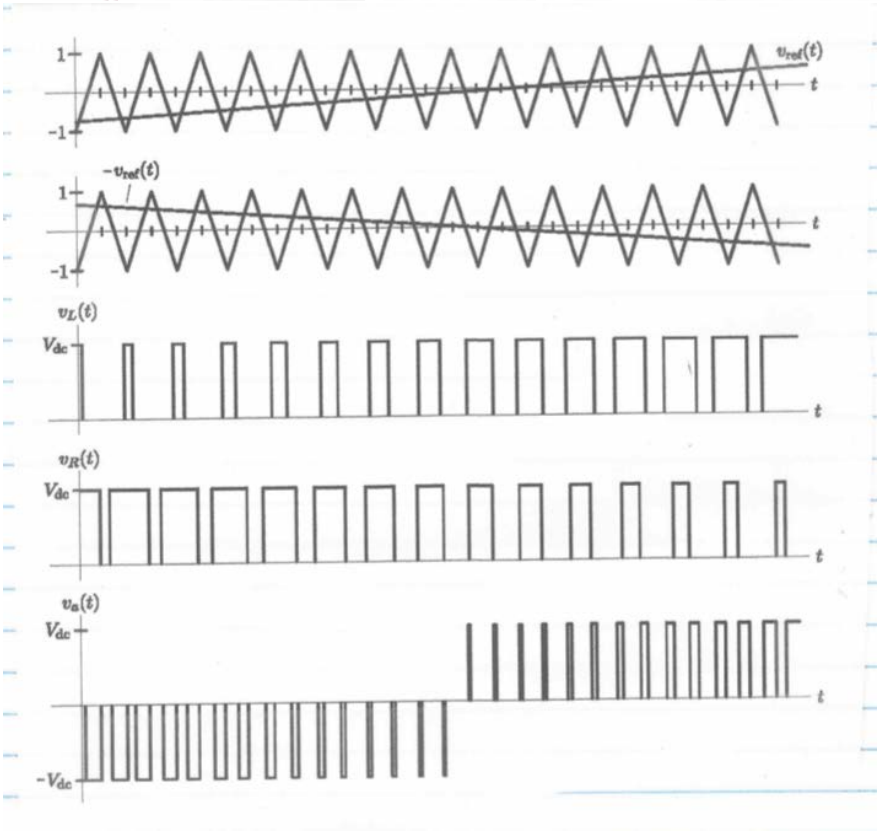
- S_{UB} on
- q(t): d(t) = $\frac{|V_{ref}|}{V_{oc}}$

If $V_{ref} < 0$:

- S_{UA} on
- q(t): d(t) = $1 - \frac{|V_{ref}|}{V_{dc}}$
  or q'(t): $d(t) = \frac{|V_{ref}|}{V_{dc}}$

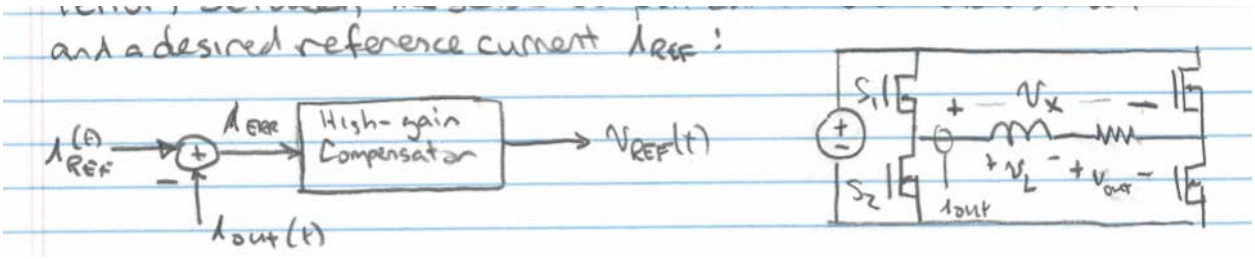
- We change the PWM control + which unfolding switch is on based on the polarity of the reference voltage, with PWM related to $|V_{ref}|$ for a bipolar V_{ref} signal.
- This gives an output pwm ripple in V_L with frequency content centered at f_{sw} of the PWM half bridge + harmonics, with sum and difference frequencies around f_{sw} and its harmonics based on the frequency content of V_{ref} - ie. @ $n \cdot f_{sw} \pm m \cdot f_{ref}$ for a reference voltage that is sinusoidal @ f_{ref}
- The PWM half-bridge switches at f_{sw} (high frequency) while the unfolding half-bridge switches at (e.g.) f_{ref} (low frequency). So, in this case, it is desirable to optimize the switch designs for S_1, S_2 differently than S_{UA}, S_{UB}.
- We can instead have a PWM scheme that treats each half-bridge equally, operating at a frequency f_{sw} with output voltage V_x and V_L seeing ripple centered near $Z \cdot f_{sw}$ and its harmonics.
- =¿ This is like having two buck converters with their outputs connected differentially, and switching them 180° out of phase!





Left HB switching @ $f_{sw} = \frac{1}{T}$ based on V_{ref}
Right HB switches @ $f_{sw} = \frac{1}{T}$ offset by $\frac{1}{2}$ cycle based on -V_{REF}
Output is difference of the 2 HB PWM pulses, has switching @ 2 f_{sw}

In many cases (e.g., motor drives) we're actually interested in controlling output current. One way to do this is to generate the voltage reference $V_{ref}(t)$ based on the difference (error) between the sensed output current (to the load) i_{out} and a desired reference current i_{ref}:

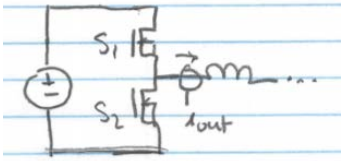


- This approach exactly uses the PWM techniques shown so far and yields devices in the inverter switching with the constant specified switching frequency.
- However, the ripple current amplitude in the output will necessarily vary over a cycle (e.g., $\Delta i_L = \frac{1}{L} v_L \Delta t$ and V_l varies with output).

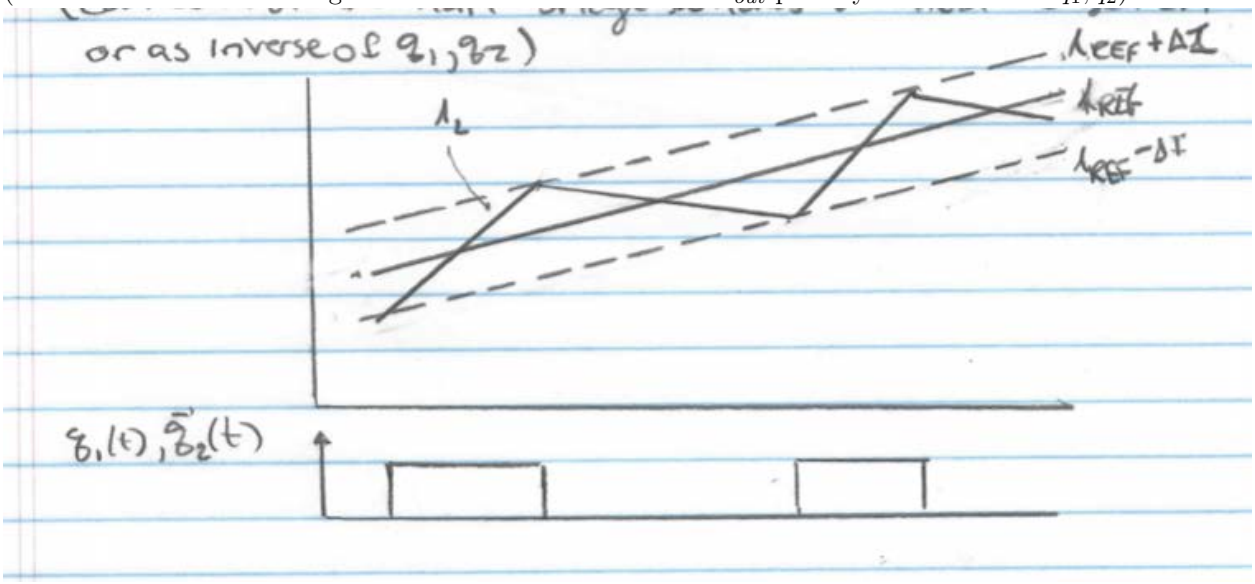
Current control (Hysteretic current control)

An alternative scheme is to switch the inverter switches to directly command the output current to closely track a current reference

Control law: compare i_{out} to i_{ref}
If $i_{out} < i_{ref}$ - Δ I turn S_1 on S_2 off
If $i_{out} > i_{ref} + \Delta$ I turn S_2 on S_1 off



(Can control other half-bridge switches to "unfold" based on V_{out} polarity or as inverse of q_1, q_2)



- In hysteretic current control, we get precise control over the instantaneous ripple current (error current always $\leq \Delta I$), but the switching frequency (and frequency content of the ripple) varies over time (sometimes not desirable).
- If we control the right-hand half-bridge as complement of the left-hand half bridge we get no "zero state". So switching frequency is higher than it needs to be. This problem is mitigated if we use the rh half bridge as an "unfolder" based on the polarity of V_{out} (more sophisticated schemes for full bridge control are also available that do not require knowledge of V_{out}).
- Both fixed-frequency PWM current control and hysteretic current control are used in practice, and there are variants that try to bridge their differences as well.

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