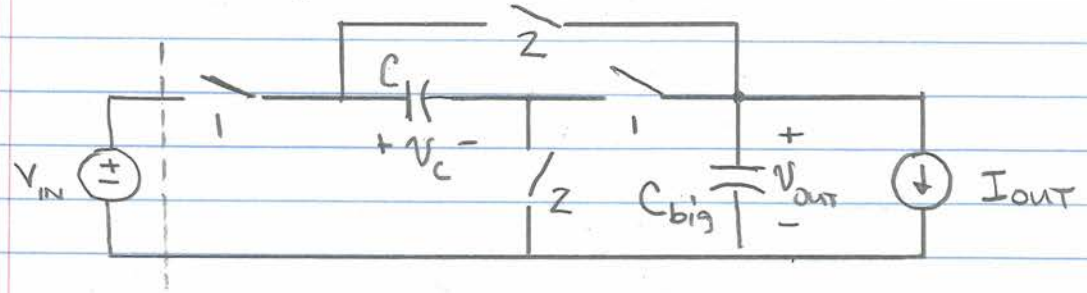
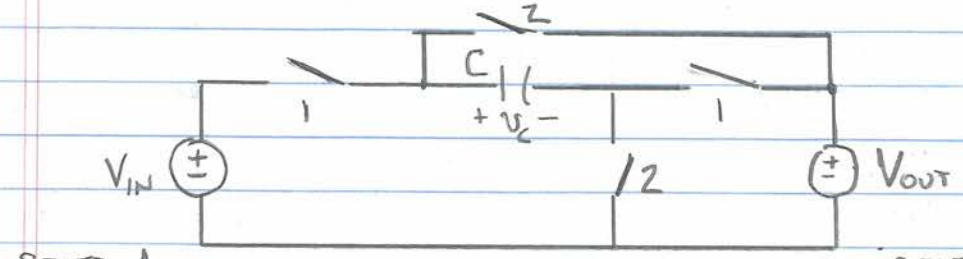
6.334 Lecture Notes — Switched-Capacitor Converters 1

Switched-Capacitor Converters are a class of switching power converter that use only switches and capacitors to provide energy and charge transfer from one voltage level to another.

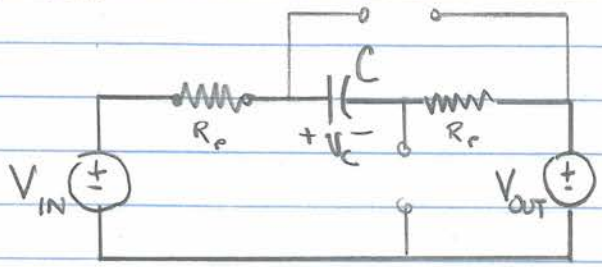
To understand "SC" converters and their characteristics, it is useful to start from an example. Consider a classic "2:1" SC step-down converter:



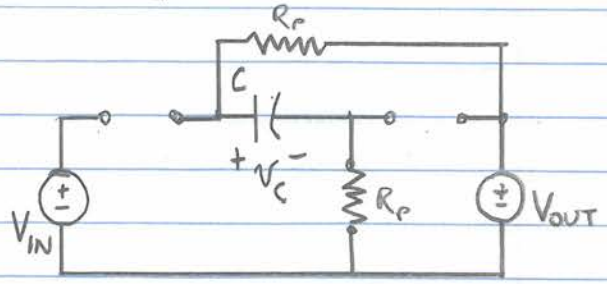
The switch sets "1" and "2" are operated in a complementary fashion (typically at ~50% duty ratio). To understand operation, assume that C_{big} is so large that its voltage variation in a switching cycle is negligible:



STATE 1 (switches "1" closed)



STATE 2 (switches "2" closed)



"Slow-switching Limit"

We first consider operation of the circuit in the "slow switching limit" (SSL), in which the energy transfer capacitor C fully charges/discharges to its limiting voltages in the circuit:

- During State 1 V_C charges to $V_{IN}-V_{OUT}$
- During State 2 V_C discharges to V_{OUT}

We can model the charge transfers in SSL as follows:

State 1:
$$\begin{cases} \Delta q_{bc(1)} = C\Delta V_C = C(V_{IN}-2V_{OUT}) = \text{charge into cap} \\ \Delta q_{bIN(1)} = -C\Delta V_C = -C(V_{IN}-2V_{OUT}) = -\Delta q_{bc(1)} = \text{charge into input} \\ \Delta q_{bOUT(1)} = C\Delta V_C = C(V_{IN}-2V_{OUT}) = q_{c(1)} = \text{charge into output} \end{cases}$$

State 2
$$\begin{cases} \Delta q_{bc(2)} = C\Delta V_C = C(2V_{OUT}-V_{IN}) \\ \Delta q_{bIN(2)} = 0 \\ \Delta q_{bOUT(2)} = -C\Delta V_C = C(V_{IN}-2V_{OUT}) \end{cases}$$

over a cycle: $\Delta q_{bC} = \Delta q_{bc(1)} + \Delta q_{bc(2)} = 0$ {in P.S.S.}

$$\Delta q_{bIN} = \Delta q_{bIN(1)} + \Delta q_{bIN(2)} = -C(V_{IN}-2V_{OUT})$$

$$\Delta q_{bOUT} = \Delta q_{bOUT(1)} + \Delta q_{bOUT(2)} = 2C(V_{IN}-2V_{OUT}) = -2\Delta q_{bIN}$$

By charge balance: $\boxed{|I_{OUT}| = 2|I_{IN}|}$ ★

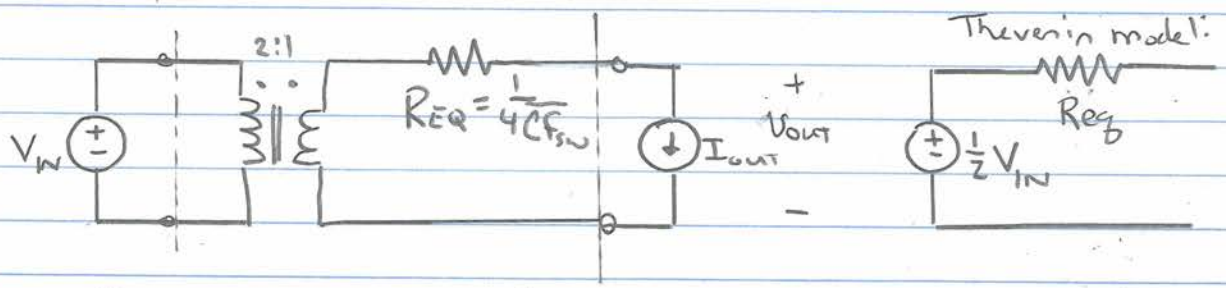
SC converters preserve current conversion ratios precisely by charge balance!

We can compute: $\boxed{I_{OUT} = \Delta q_{bOUT} f_{sw} = 2C(V_{IN}-2V_{OUT}) f_{sw}}$

we can rearrange this to show the voltage conversion relation:

$$V_{out} = \frac{1}{2} V_{IN} - \frac{1}{4Cf_{sw}} \cdot I_{OUT} \quad \star$$

A dc equivalent circuit model for this SC converter in SSL is:



The efficiency of the converter (considering only charge transfer loss) is

$$\eta = \frac{W_{OUT}}{W_{IN}} = \frac{V_{OUT}\,\Delta q_{OUT}}{-V_{IN}\,\Delta q_{IN}} = 2\frac{V_{OUT}}{V_{IN}} = \frac{V_{OUT}}{\frac{1}{2}V_{IN}} \quad \star\star$$

which is equivalent to our dc model efficiency.

from $\star$, $\star\star$

$$\eta = 1 - 2\frac{I_{OUT}}{4Cf_{sw}} \cdot \frac{1}{V_{IN}} \qquad \left\{ \text{since } R_{eq} = \frac{1}{4Cf_{sw}} \right\}$$

$$\boxed{\eta = 1 - \frac{I_{OUT} R_{eq}}{\frac{1}{2}V_{IN}}}$$

Efficiency depends upon R_{eq}, V_{OUT}

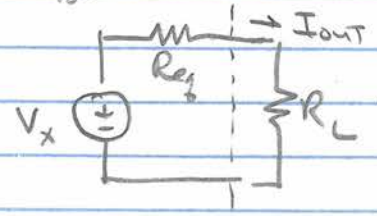
- We thus get a perfect current conversion ratio $I_{OUT} = 2 I_{IN}$ as determined by the charge balance on the energy transfer capacitor(s).

- The voltage conversion ratio depends upon the load current I_{OUT} and is near perfect $V_{out} \approx \frac{1}{2}V_{IN}$ at low load current and/or high switching frequency, but droops from this unloaded conversion ratio with higher load current. We can reduce the droop with higher energy transfer capacitance and/or switching frequency
  ⇒ more generally for a particular SC topology and operation we get an exact rational current conversion ratio A/B $A, B \in \mathbb{I}$ + approx. voltage ratio

6.334 Lecture Notes — Switched-Capacitor Converters 1

- When the converter is unloaded we get an "open circuit" voltage conversion ratio that is the inverse of the current conversion ratio. As current increases, the output voltage drops and efficiency declines.
  - ⇒ Efficiency + loss behavior is just that of a series output resistance [in this case of $R_{eq} = \frac{1}{4Cf_{sw}}$ in SSL]

$$\eta = \frac{V_{OUT}}{V_x} = \frac{R_L}{R_L + R_{eq}}$$



  - ⇒ In other topologies both the open circuit voltage (ratio from V_{in}) and R_{eq} are different
  - ⇒ This only accounts for capacitor charge/discharge loss (switching, gating loss etc are additional loss mechanisms)
  - ⇒ one can use the R_{eq} to provide regulation (like a linear regulator) but only at the efficiency penalty described above
  - ⇒ SC converters are excellent for voltage transformation but terrible for efficient regulation.

Fast Switching Limit (FSL)

- The above analysis (particularly for the R_{eq} value) assumed the slow switching limit where the energy transfer capacitor charges/discharges to its limits

- As we increase f_{sw} or C (e.g. to reduce R_{eq} and increase efficiency), we eventually reach a regime where the charge/discharge of the energy transfer capacitance is limited by circuit resistances {and we can neglect ripple voltage on C}. This is the "Fast Switching Limit" FSL

Lets analyze the FSL for our "2:1" SC, assuming 50% switch duty ratios (for sets 1,2) and ignoring ripple in V_c : (R_p is parasitic resistance)

STATE 1:
$$\begin{cases} \Delta q_{c,1} = \dfrac{V_{IN} - V_{OUT} - V_c}{2R_p}(0.5T) \\ \Delta q_{IN} = -\Delta q_{c1} \\ \Delta q_{OUT,1} = \Delta q_{c1} \end{cases}$$

(D for sw. set 1 — switching period)

STATE 2:
$$\begin{cases} \Delta q_{c2} = -\dfrac{V_c - V_{OUT}}{2R_p}(0.5T) \\ \Delta q_{IN,(2)} = 0 \\ \Delta q_{OUT}(2) = \Delta q_{c2} \end{cases}$$

By charge balance on C : $\Delta q_{c1} = -\Delta q_{c2}$

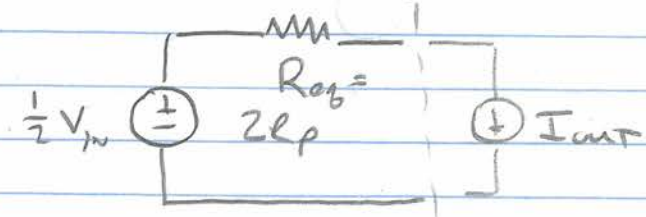
$$\frac{V_{IN} - V_{OUT} - V_c}{2R_p} \cdot (0.5T) = \frac{V_c - V_{OUT}}{2R_p}(0.5T)$$

$$\therefore \boxed{V_c = \tfrac{1}{2} V_{IN}}$$

Also, by charge flow (as with SSL) $\boxed{|I_{OUT}| = 2|I_{IN}|}$

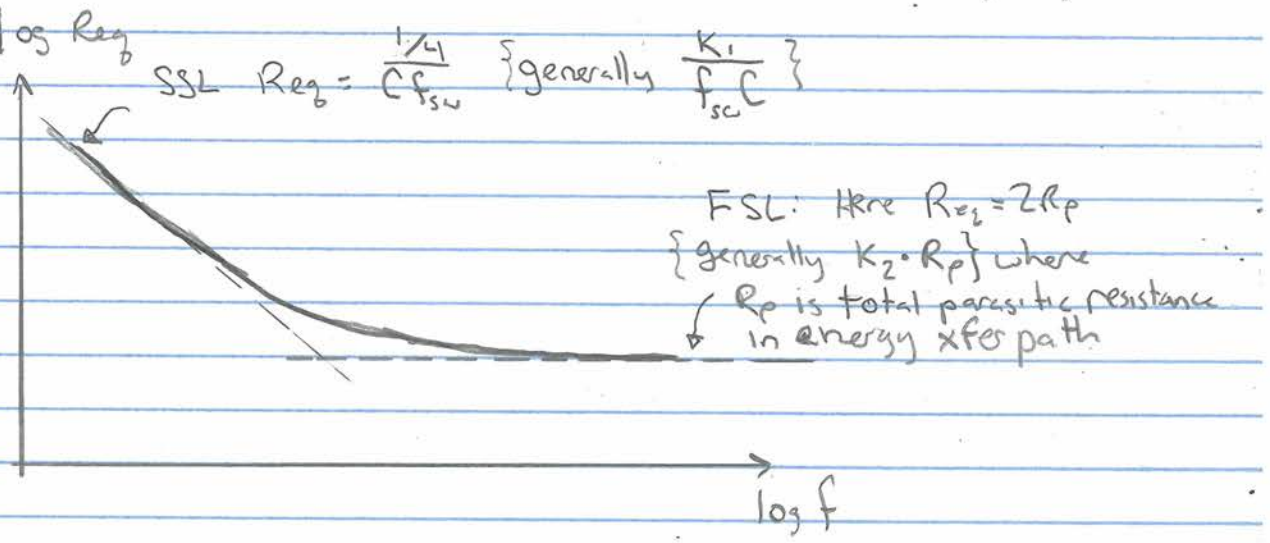
$$I_{OUT} = \frac{V_{IN} - V_c - V_{OUT}}{2R_p} = \frac{\frac{1}{2}V_{IN} - V_{OUT}}{2R_p} \Rightarrow \boxed{V_{OUT} = \tfrac{1}{2}V_{IN} - 2R_p I_{OUT}}$$

In FSL, we get a similar model to SSL, but with a different R_{eq} {$R_{eq} = 2R_p$, where R_p is parasitic resistance}
(we could also include capacitor Esr → $R_{eq} = 2R_p + R_{ESR}$)



- The open-circuit voltage is the same in FSL, SSL and is proportional to V_{in} by a rational factor $\frac{A}{B}$ that depends on topology

- The equivalent output resistance is a function of frequency



- At full load we often operate near the intersection of SSL, FSL as we want to switch fast enough to get low R_{eq}, but continuing to increase frequency much past the SSL/FSL boundary doesn't reduce R_{eq} but incurs increased loss (e.g. capacitive switching loss, gating loss, etc.)

6.622 Power Electronics

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