6.622 Power Electronics *Prof. David Perreault*

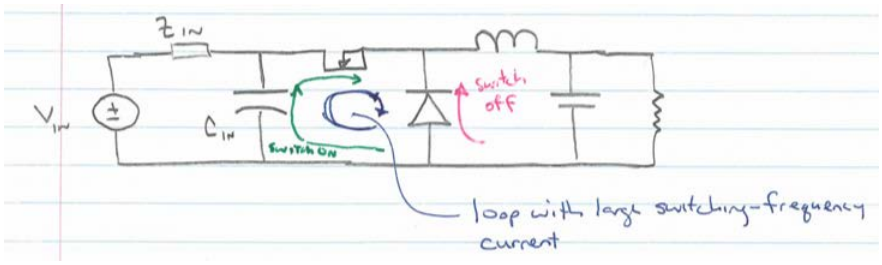
Lecture 38 - Gate Drive, Level Shift, Layout

1 Layout

Layout is a critical aspect of a power electronics design. Positioning of components has a huge impact on performance. Here we introduce a few ideas about layout.

1. Certain loops must be kept very "tight" and have low inductance ⇒ important for loops around which large, high freq currents commutate

   e.g. buck converter



   - The loop formed by the switch, diode, and input capacitor should be kept very "tight" and low inductance to prevent:
     - big voltage transients and ringing at switch transitions (inductance will "ring" with device + parasitic capacitance)
     - EMI from being coupled and interfering with other circuits
   - Loops that do not contain pulsating current (e.g., branch in series with an inductor) are not typically critical.

   How do we minimize inductance? ⇒ Next page

2. We may also choose to reduce capacitance where possible

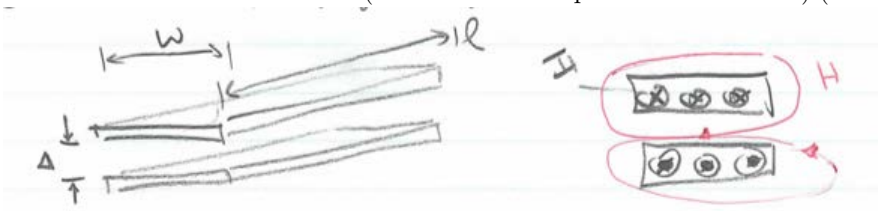
   (a) Across inductances (e.g. for filters) ⇒ by layout

   (b) At nodes with large pulsating voltages! → e.g. @ node w/ diode cathode, fet source, inductor

   ⇒ Can also do a faraday shield

   ⋆ Show switching layout demo cicuitry

Consider a trace and its return (connected to components at each end) (underneath it, e.g. ground plane)



$\int H \cdot d\ell = \int I \cdot dA$. If most field between line and return:

$$H_x \cdot w = I \Rightarrow H_x = \frac{I}{w}$$

Stored magnetic energy $w_m \quad \frac{1}{2}\int\int\int B \cdot H dv = \frac{\mu_0}{2} H^2 \cdot V$

$$w_m = \frac{\mu_0 I^2}{2w^2} \cdot \Delta w l = \frac{1}{2}\mu_0 \frac{\Delta \cdot l}{w} I^2$$

Now $w_m = \frac{1}{2} L I^2 \therefore L\ \mu_0 \frac{\Delta \cdot \ell}{w}$

So inductance ↑ with length ℓ

↑ spacing between conductors Δ

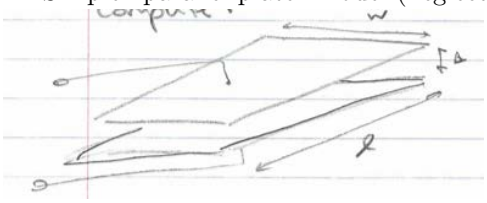
↓ width of conductor.

So to minimize inductance (e.g., in gate drive loop):

1. put drive and return traces close (one underneath another on PCB board)
2. make as short as possible
3. make wide trace width, (especially if cannot make short)

Excess capacitance at a node also injects additional charge from one conductor to another.

Simple "parallel plate" model (neglecting fringing) is easy to compute:

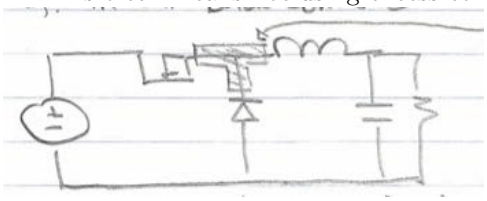


$$C_{p\rho} = \frac{\epsilon A}{d} = \frac{\epsilon W \cdot \ell}{\Delta}$$

So to minimize charge injected from one conductor to another

- Maximize seperation Δ
- Minimize area $A = w \cdot \ell$

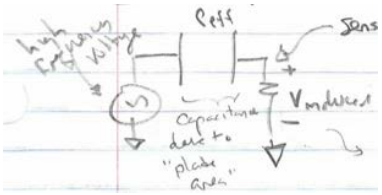
This often means not using excess conductor area at "flying nodes" e.g. in our buck converter



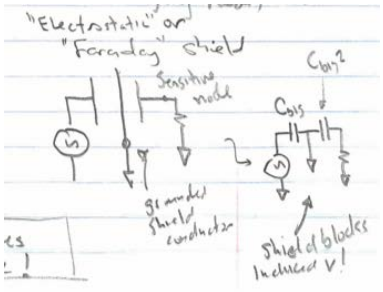
- Keep this area small!
- One could make sure that distances to sensitive (e.g. high impedance) nodes (e.g. comparator inputs) is significant

2 Electrostatic or "Faraday" shield

Note that one can also "shield" sensitive nodes from a flying potential using an electrostatic shield (e.g., a grounded "blocking" conductor). This increases total capacitance to the flying node but reduces capacitance to a sensitive node.



Sensitive "high impedance" node will see induced voltage due to capacitance



shielding increase total capacitance, but improves injection to a specific node!

Note that Faraday shields reduce the capacitance between specific nodes, while increasing total capacitance. This is often acceptable (shields are often used in transformers, for example).

It is also useful to note that there is a direct trade-off between inductance and capacitance of a structure. Consider our parallel-plate interconnect (and its inductance and capacitance).

$$L \approx \frac{\mu_0 \Delta \ell}{w} \quad C \approx \frac{\epsilon w \cdot \ell}{\Delta}$$

For one unit length:

$$L' = \frac{\mu_0 \Delta}{w}, \quad C' = \frac{\epsilon w}{\Delta} \Rightarrow L'C' = \epsilon_0 \mu_0$$

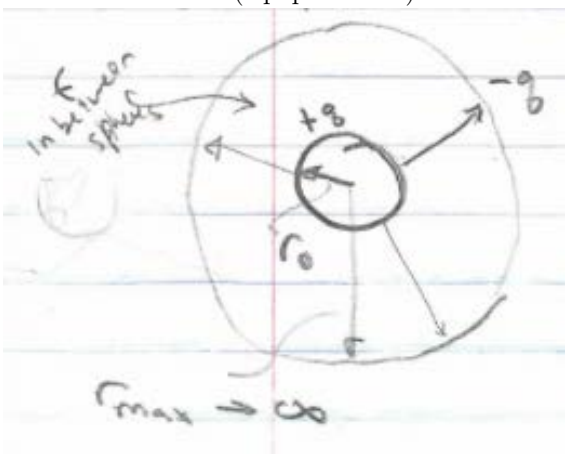
and we know

$$\sqrt{\frac{1}{L'C'}} = \frac{1}{\sqrt{\epsilon_0 \mu_0}} = c \quad \text{(the speed of light!)}$$

So we can only trade inductance for capacitance in this structure.

Also, note that for capacitance, once our "plates" move apart, fringing fields dominate capacitance, and so capacitance does not fall quickly with distance (e.g., $\propto \frac{1}{d}$ for large distances). In fact, a body of a certain size has a finite (nonzero) capacitance to a conductor at infinity!

Consider capacitance of a sphere of radius r_0 to a surface @ $r \to \infty$ (equipotentials)



We know $\int \epsilon E \cdot dA = q$ fo ra charge q balanced @ ∞, E is radial

$$E = \frac{1}{\epsilon(4\pi r^2)}$$

What is the voltage (potential) at the sphere wrt ∞?

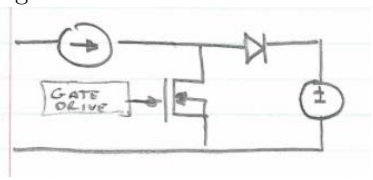
$$V = \int_{\infty}^{r_0} E dr = \frac{q}{\epsilon \cdot 4\pi r}|_{\infty}^{r_0} = \frac{q}{\epsilon 4\pi r_0}$$

$$\therefore C = \frac{q}{V} = \epsilon \cdot 4\pi r_0 \to \text{ a finite capacitance!}$$

(We reduce capacitance only be reducing radius / surface area!)

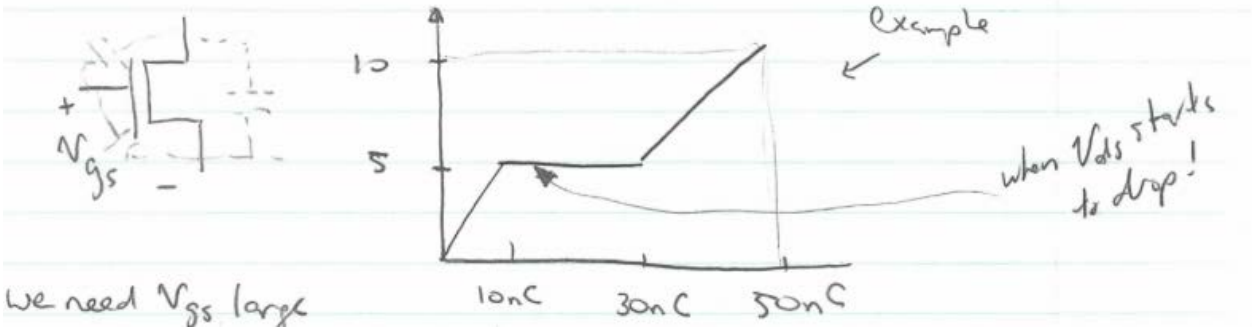
Consider the problem of turning on and off the power device(s) in a converter

e.g. boost converter:



We need to switch on and off quickly to minimize the switching losses

MOSFET gates look capacitive (nonlinear)

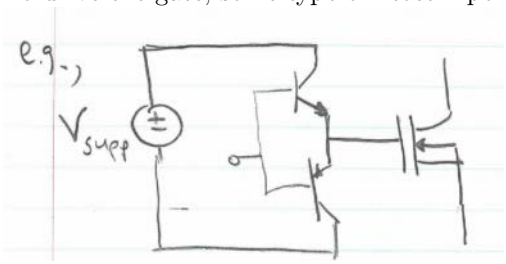


We need V_{gs} large
So MOSFET looks like a resistor!

$$\text{for } V_{gs} > V_T, V_{ds} < V_{gs} - V_T \quad i_d = K[(V_{gs} - V_T)V_{ds} - \frac{1}{2}V_{ds}^2]$$

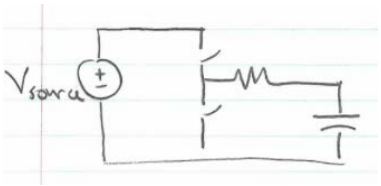
$$\text{if } V_{gs} - V_T >> V_{ds} \therefore i_d \approx K(V_{gs} - V_T)V_{ds}$$

To drive the gate, some type of "totem pole" buffer is used

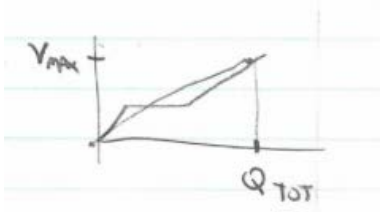


Could use DSODZG line driver, for example, or available MOS gate drivers such as 3907?
Some PWM IC's put gate drivers inside

Note that the gate driver dissipates energy in switching. How much?



$$C_{eq} = \frac{Q_{tot}}{V_{max}}$$



The supply must source Q_{Tot} charge to charge gate capacitance.
$\therefore \text{Energy}_{\text{in}} = Q_{\text{Tot}} \cdot V_{\text{Source}}$.
Some of this is stored. For a linear capacitor,

$$E_{\text{stored}} = \frac{1}{2} C_{\text{eq}} V_{\text{Source}}^2 = \frac{1}{2} Q_{\text{Tot}} V_{\text{Source}}.$$

and the rest is dissipated as heat. {Note, resistor value doesn't matter!}
When gate is discharged at end of cycle, that energy is **lost**!

So, the total energy per cycle from the gate driver is

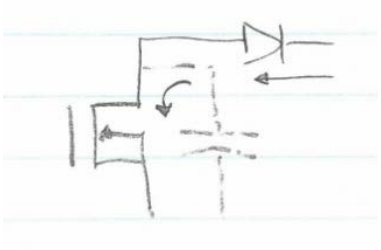
$$E_{\text{Tot}} = V_{\text{Supply}} \cdot Q_{\text{Tot}}$$

The power will be the energy per cycle × cycles/sec,

$$P_{\text{Drive}} = E_{\text{Tot}} \cdot f = V_{\text{Supply}} \cdot Q_{\text{Tot}} \cdot f_{\text{SW}}$$

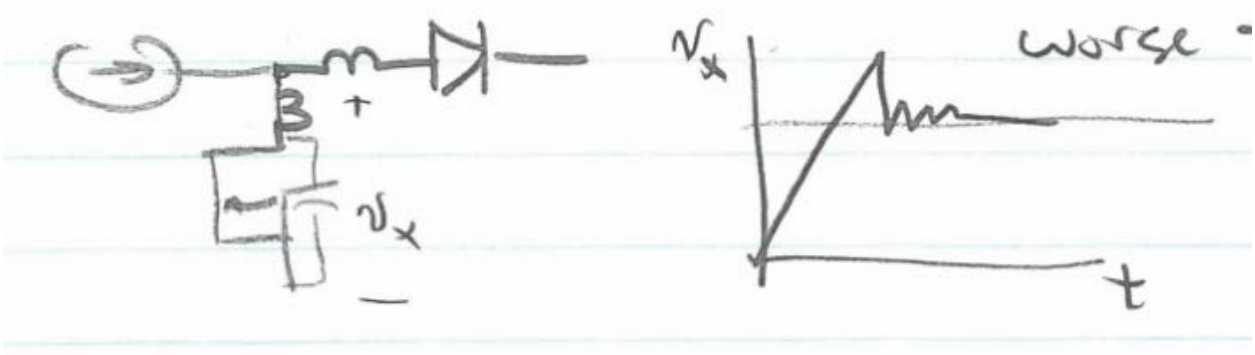
This is (largely) dissipated in the driver (plus some in the internal gate resistance and any external resistors).
⇒ Driver must be properly rated.

From a loss standpoint, one would like to switch as fast as possible. However, faster switching increases EMI.



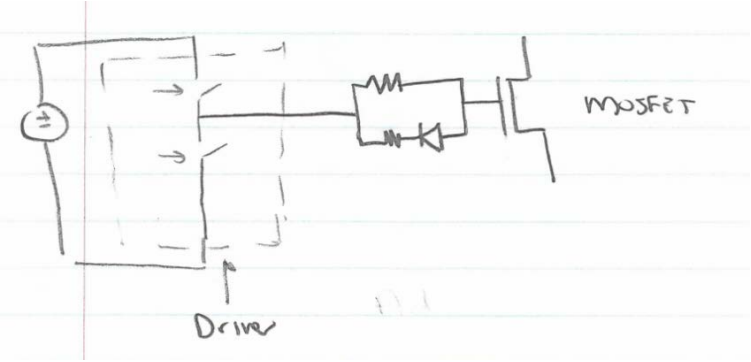
On Turn on, the switch capacitance charge is dumped, and the diode reverse recovery charge is dumped into the device turning on. A fast transition increases the emitted noise ($dV/dt \uparrow$)

On turn off, the switch and diode path inductance can cause overshoot (+ ringing w capacitance), which gets worse as $\frac{di}{dt} \uparrow \therefore$ EMI gets worse



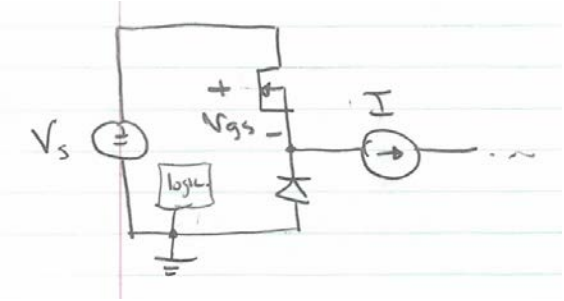
So for EMI reasons, we may want to limit our turn on and turn off rates, perhaps to different values.

One way to do this



- Adding a gate resistor slows switching down.
- Using resistor/diode combinations, we can control turn on and turn off separately, to balance switching loss and EMI as desired.
- Some "fancy" designs actually feedback drain voltage to control switching in a closed-loop fashion.

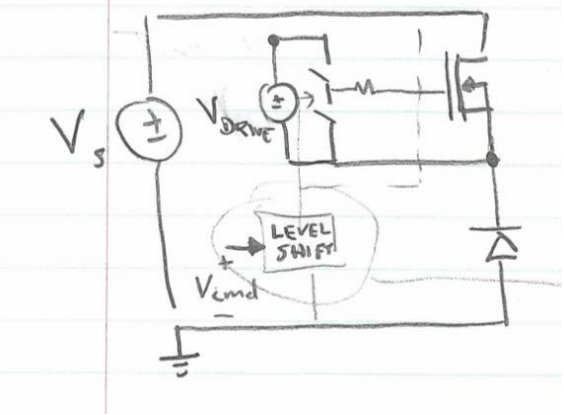
Suppose we have a "high-side" device (e.g., buck converter), with control referenced to ground.



We need to "level shift" the control command to the high side, and generate a V_{gs} voltage such that

$$V_{g,\text{gnd}} > V_s$$

For some cases, one can purchase a level-shifting driver (e.g., IR2125). One must still supply a floating power supply to drive the high-side gate.

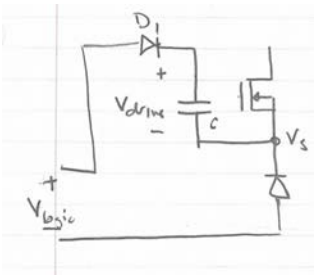


When top switch is on the gate, voltage $> V_s$ $\approx V_s + V_{drive}$

Can do discrete, on in some IC's

Building a floating supply can be tricky.

- Use isolated dc/dc to generate (e.g., 1Wconverters like NME1212)
  $\Rightarrow$ Simple but expensive
- Use "Bootstrap" charging of capacitor



- When diode on, bootstrap capacitor charges up from "low-side" supply.
- Charging diode D_1 turns off when V_s starts to rise.
- Capacitor voltage serves as "floating supply."

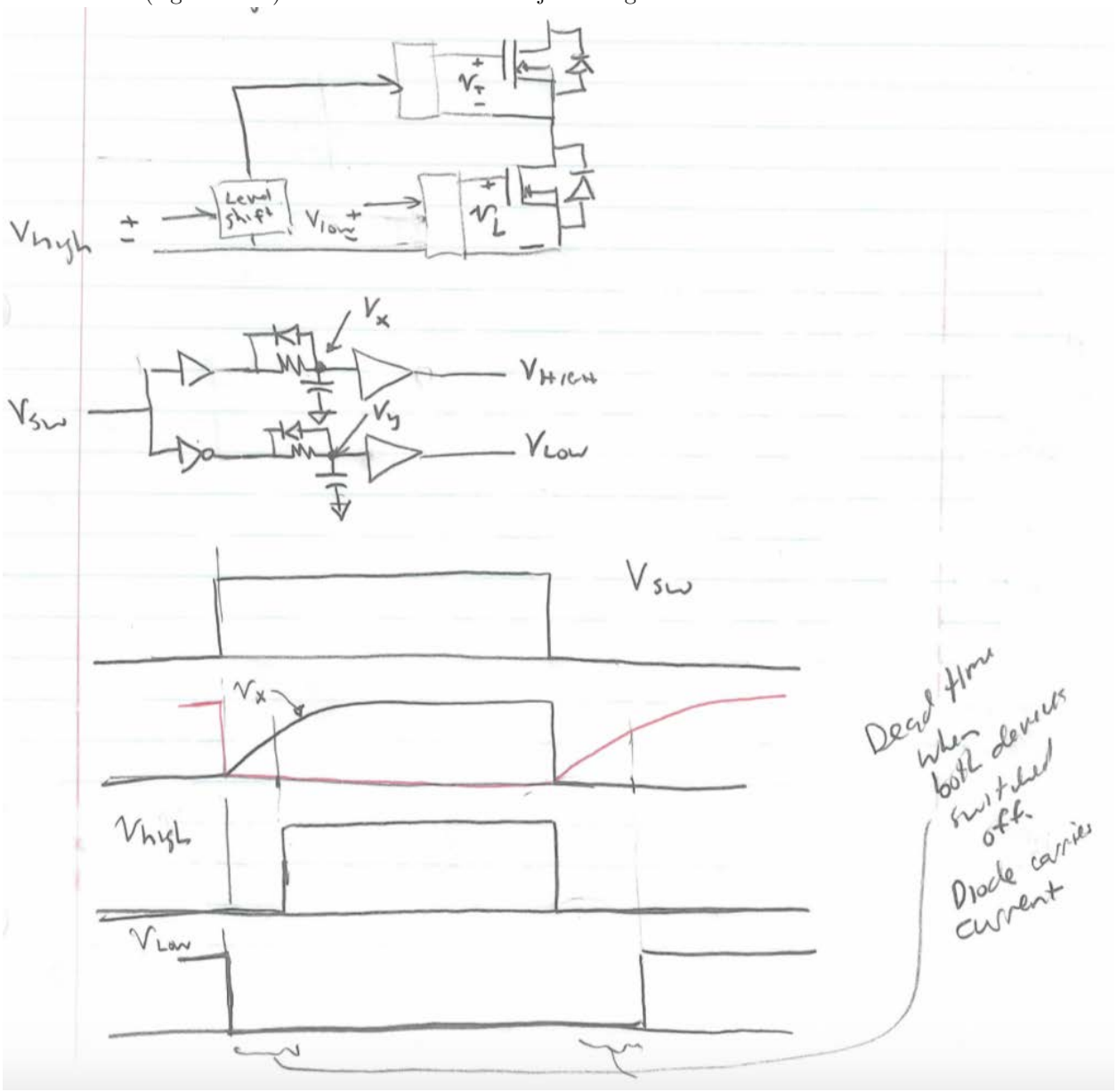
$\Rightarrow$ Inexpensive, but $D \equiv 1$ not possible (must recharge capacitor periodically).

Other methods also possible:

e.g., Transformer-coupled (not covered here).

If one has both high and low-side devices, one must ensurer that they both are not on at the same time! (Shoot-through protection)

Some drivers (e.g. IR2110) build this in sometimes just design it.



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