6.6220 HW2 Solution*

2.1 Source Resistance Boost Converter

If we look at the capacitor voltage v_c as the input of the boost converter, then we know from previous analysis that $v_{out}/\langle v_c \rangle = 1/(1-D)$.

Looking at the first loop, KVL tells us that $\langle v_c \rangle = V_{in} - R_{in} I_{in} = V_{in} - R_{in} I_{out}/(1-D)$. Noting that $I_{out} = V_{out}/R_{out}$ we can plug in and rearrange to get:

$$D^2 + \left(\frac{V_{in}}{V_{out}} - 2\right) D + \left(\frac{R_{in}}{R_{out}} + 1 - \frac{V_{in}}{V_{out}}\right) = 0$$

Before even calculating a numerical solution, we notice this equation is quadratic in D and should yield two solutions. If the solutions are complex conjugates, it means we can no longer achieve the voltage ratio we thought we could. If the solutions are real, then we may settle around two different duty cycles for the same step-up ratio (this could be bad for control). For this problem, plugging in our numbers gives us $D = 0.733$ or $D = 0.85$.

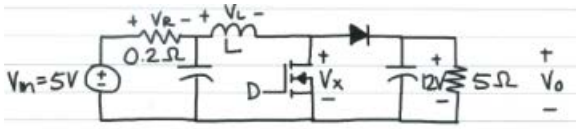

Figure 1: Circuit for the problem

Notice that in the ideal case, $R_{in} \to 0$ and the solutions are 1 and $1 - V_{in}/V_{out}$. Since the ideal boost converter solution doesn't actually include $D = 1$ (as it implies infinite output voltage), we can consider this the same as the ideal boost analysis, with only one actual solution. For small R_{in} we get split real solutions, and large R_{in} prevents us from achieving the desired boost ratio (yielding complex D).

Another interesting perspective on this solution is that you can write the output voltage as

$$V_{out} = \left[\frac{V_{in}}{1-D}\right]\left[\frac{1}{1 + \frac{R_{in}}{R_{out}(1-D)^2}}\right]$$

Noting that the average input-output current relationship in this circuit is the same as in the ideal case, $I_{out} = (1-D) I_{in}$, we can write the output power of the converter as

$$P_{out} = P_{in}\left[\frac{1}{1 + \frac{R_{in}}{R_{out}(1-D)^2}}\right]$$

The term in square brackets is the efficiency of the converter!

2.2 SEPIC Converter Switch Implementation

For the following analysis, we will denote the direction from left to right as "positive" for the sign of voltages and currents.

In SEPIC converter, where the input voltage has positive polarity, the left switch must block positive voltage and carry positive current, and the right switch must block negative voltage and carry positive current. When you flip the input voltage to negative polarity, the SEPIC converter essentially must run in a "flipped" orientation, where the left switch must block negative voltage and carry negative current, while the right switch must block positive voltage and carry negative current. So, for the converter to work with either input voltage polarity, both switches must block positive and negative voltages and carry positive and negative currents. You can replace each switch using any of the switches pictured in Fig. 2.

2.3 5.18

(a) Consider the loop containing L_m, the diode, L_s and R_L. By average KVL, the average

*K. Rafa Islam, Mansi Joisher 2023 (adapted from Yang 2022, Boles 2021, Ranjram 2020, Zhang 2019, and He 2017)

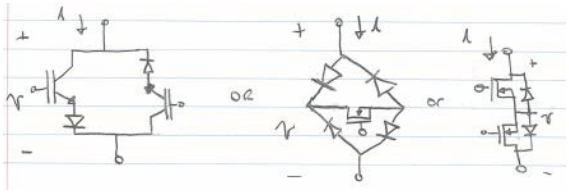

Figure 2: Possible switch implementations for the SEPIC converter to work with any input voltage polarity

diode voltage is equal to the average output voltage. Because the diode can only block a negative voltage from its anode to its cathode, only a negative output voltage polarity is possible.

(b) Similarly, the MOSFET blocks V_g on average between its drain and source terminals. Because a MOSFET can only block a positive voltage between its drain and source terminals, only a positive V_g is possible.

(c) Reducing the connection between the three inductors to a supernode, we find $i_P + i_S = i_m$. Thus, $\langle i_m \rangle = \langle i_P \rangle + \langle i_S \rangle$.

(d) When the switch is on and the diode is off, $i_c = -i_S$. Conversely, when the switch is off and the diode is on, $i_c = i_P$. Enforcing zero average current in the capacitor, $-Di_s + (1-D)i_p = 0$. Thus, $i_s/i_p = (1-D)/D$.

(e) Apply conservation of power, $V_g i_P = -V_o i_S$. Thus, $V_o/V_g = -D/(1-D)$.

(f) When the switch is off, it blocks v_C. We get v_C directly from average KVL: $V_C = V_g - V_o = V_g/(1+D)/(1-D) = V_g/(1-D)$.

2.4 Buck Converter L & C Design

2.4.1 Part A

The output of the buck converter has a capacitor in parallel with the load resistor and these components are fed by the inductor. The inductor current will have an average (dc) component and a ripple (ac) component. The capacitor cannot have average current through it in periodic steady state, so the most current that can flow through the capacitor is the ripple current of the inductor (and ideally it would all flow through the capacitor to ensure a steady dc output voltage). Thus, ensuring less than 5A rms ripple flows through the capacitor is equivalent to ensuring less than that ripple flows through the inductor.

We can find the ripple current in the inductor based on the voltages that are dropped across it in the two switching stages. We know in part (b) that we are going to design the capacitor to have a ripple ratio of less than $(1.2/2)/48 = 1.25\%$, so it is a great approximation to treat the capacitor voltage as dc (V_{out}).

When the switch is on and the diode is off, the inductor sees a positive constant voltage ($V_{in} - V_{out}$). Then, when the switch is off and the diode is on, the inductor sees a negative constant voltage $-V_{out}$. So, we expect the inductor ripple current to be a triangular waveform.

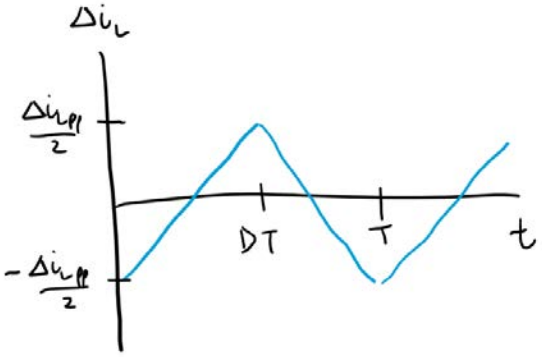

Figure 3: Inductor ripple current (same as capacitor ripple current)

We can solve for what Δi_{Lpp} is by integrating the inductor voltage from time 0 to DT.

$$\Delta i_{Lpp} = \frac{V_{in}(1-D)DT}{L}$$

Now, we need to figure out what inductance values allow us to meet the requirement that the rms

ripple current $\Delta i_{L,rms} = 4\,\mathrm{A_{rms}}$. Since the ripple current is a triangular wave, we know that $\Delta i_{L,rms} = \Delta i_{Lpp}/(2\sqrt{3})$. So, to meet the ripple current requirement, we need

$$L \geq \frac{V_{in}(1-D)D}{f\Delta i_{L,rms}2\sqrt{3}} = 3.46\,\mu\mathrm{H}$$

An example inductance that would meet our requirement is $L = 4\,\mu\mathrm{H}$. This value would give a ripple current with $\Delta i_{cpp} = 12.0\,\mathrm{A_{pp}}$ and an rms capacitor current $\Delta i_{c,rms} = 3.46\,\mathrm{A_{rms}}$.

2.4.2 Part B

The output ripple voltage is the same as the capacitor ripple voltage, which can be derived from integrating the capacitor ripple current. Since the current ripple is a triangular wave, the voltage ripple should look like the following:

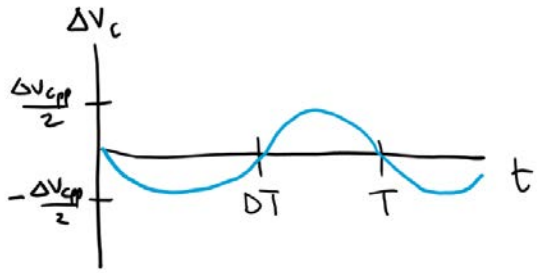

Figure 4: Capacitor ripple voltage (same as output ripple voltage)

To solve for $\Delta v_{cpp}/2$, we can integrate Δi_{Lpp} from time 0 to $\frac{1}{2}DT$.

$$\frac{\Delta v_{cpp}}{2} = \frac{1}{8}\frac{\Delta i_{Lpp}D}{Cf}$$

So, to satisfy the output ripple voltage, we need a capacitor value such that

$$C \geq \frac{1}{4}\frac{D\Delta i_{Lpp}}{f\Delta v_{cpp}}$$

Using the example inductance value from Part A ($L = 4\,\mu\mathrm{H}$), which gives $\Delta i_{cpp} = 12.0\,\mathrm{A_{pp}}$, we need $C \geq 5.0\,\mu\mathrm{F}$. Let's pick an example capacitor value of $C = 6\,\mu\mathrm{F}$, which would give a ripple voltage of $\Delta v_{cpp} = 1.0\,\mathrm{V}$.

2.4.3 Part C

We'll simulate the converter using the example values of $L = 4\,\mu\mathrm{H}$ and $C = 6\,\mu\mathrm{F}$ (Fig. 5).

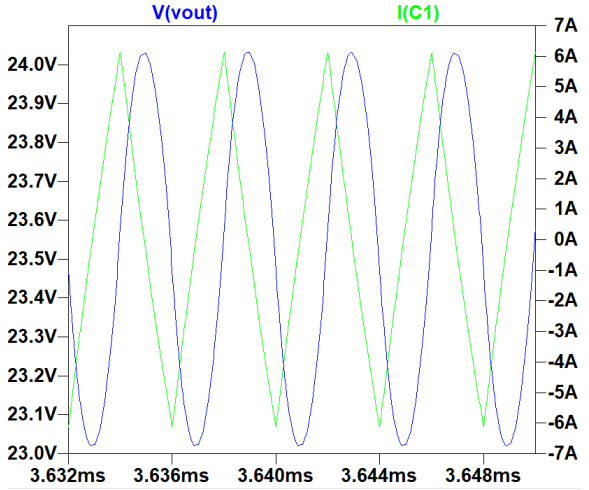

Figure 5: Buck converter simulation using the $L = 4\,\mu\mathrm{H}$ and $C = 6\,\mu\mathrm{F}$

The capacitor ripple current has a peak-to-peak value of $12.2\,\mathrm{A_{pp}}$, which gives an rms current of $3.5\,\mathrm{A_{rms}}$. The output ripple voltage has a peak-to-peak value of 1.0 V. So both ripple requirements are met.

2.4.4 Part D

While using $L = 4\,\mu\mathrm{H}$ and $C = 6\,\mu\mathrm{F}$ satisfies the ripple requirements, it does not satisfy the transient requirement. Instead, a much bigger capacitor is needed to suppress the transient. (So, sizing components to satisfy ripple requirements does not necessarily mean that other requirements, such as transient requirements, are met.)

Here, we bump up the capacitance to $20\,\mu\mathrm{F}$ and simulate (Fig. 6 and 7). The two load step tran-

sients now satify the transient requirement while also meeting the ripple requirements.

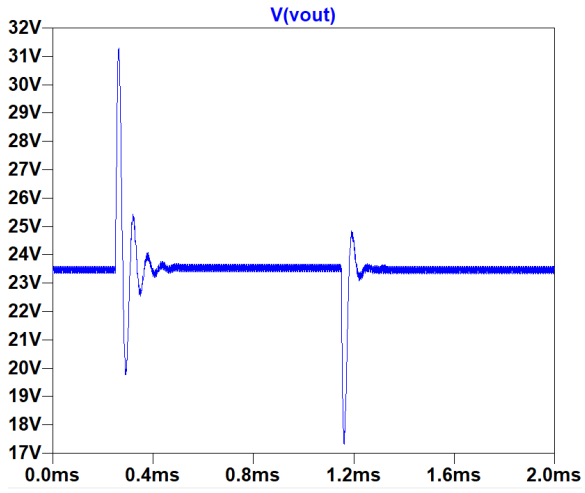

Figure 6: Simulated output voltage transient response

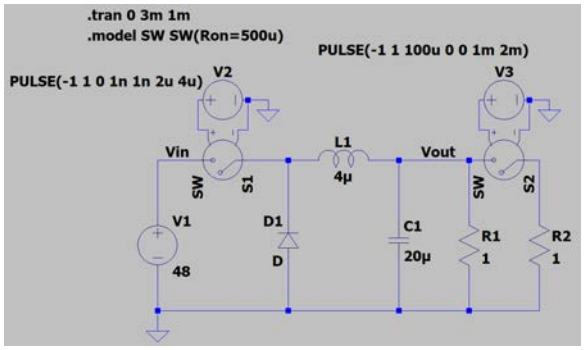

Figure 7: Simulated buck converter for the load step transients

2.5 Battery-Interface Circuit

We might draw the power converter in a more enlightening way as follows: where we can immediately see that this is an inverted buck-boost converter.

In CCM, by volt-second balance, we know that

$$+V_1 DT - V_2(1-D)T = 0 \qquad (1)$$

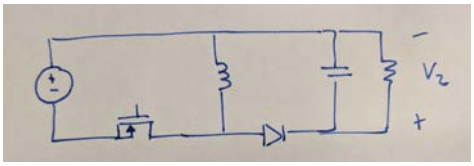

Figure 8: Re-drawing the battery-interface circuit as an inverted buck-boost converter.

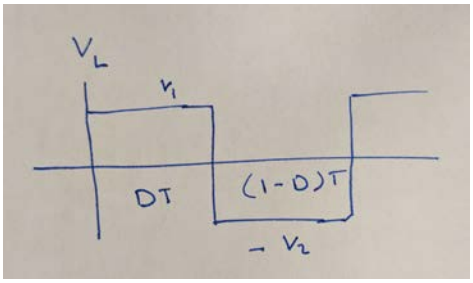

Figure 9: Analyzing the inductor voltage to ensure volt-second balance.

and therefore

$$V_2/V_1 = D/(1-D) \qquad (2)$$

as expected for a buck-boost converter. Note that, with the way V_2 is defined, the resulting conversion ratio is positive.

To analyze the circuit in DCM, focus on the energy storage variabel i_L,

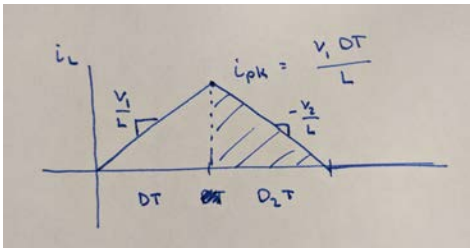

Figure 10: Analyzing the inductor current in DCM to determine $\langle i_D \rangle$.

We can calculate the average output current:

$$Q_{out} = \frac{1}{2}\,\text{Base} \times \text{Height} \tag{3}$$

$$= \frac{1}{2}(D\frac{V_1}{V_2}T)(\frac{V_1 DT}{L}) \tag{4}$$

$$\langle i_{out} \rangle = \frac{1}{2}\frac{V_1^2 D^2 T}{V_2 L} \tag{5}$$

Now, we know that $\langle i_{out} \rangle = V_2/R$ and, at the boundary of CCM and DCM, $D_2 = 1 - D \implies V_2 = V_1 \times D/(1-D)$. Plugging these results into our expression for $\langle i_{out} \rangle$ and rearranging gives us D:

$$D_{crit} = 1 - \sqrt{\frac{2L}{RT}} \tag{6}$$

For the given values of 9 µH, 8 Ω, and 500 kHz, the critical duty cycle is $D = -0.0606$.

In other words, for these specifications, the converter never enters DCM. You can test this result in SPICE by setting up the converter and running it at a very low duty cycle ($D \approx 0.01$) and checking that the inductor current is still in CCM.

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