# 6.6220 HW4 Solution* 

## 1 KPVS 7.1

The conversion ratio for the single-ended forward converter with leakage inductances neglected is

$$
V_{2}=D \frac{V_{1}}{N}
$$

The value of $V_{c}$ must be chosen on the basis of a Volt-second balance on the primary. This balance gives

$$
V_{1} D T \leq\left(V_{c}\right)(1-D) T
$$

Substituting in $D=N V_{2} / V_{1}$ gives

$$
N V_{2} \leq\left(V_{c}\right)\left(1-\frac{N V_{2}}{V_{1}}\right)
$$

Solving for $V_{c}$ gives

$$
V_{c} \geq \frac{N V_{2} V_{1}}{V_{1}-N V_{2}}
$$

We have $V_{2}=5 \mathrm{~V}$ and $N=2$. For $V_{1}=$ $100 \mathrm{~V}, V_{c}=11.1 \mathrm{~V}$. If $V_{1}=50 \mathrm{~V}, V_{c}=12.5 \mathrm{~V}$. It follows that the minimum value of $V_{c}$ that will work for the entire input voltage range is $V_{c} \geq 12.5 \mathrm{~V}$.

## 2 KPVS 7.24

(a) First, applying average KVL, we find: $\left\langle V_{1}\right\rangle=$ $\left\langle v_{L 1}\right\rangle+\left\langle v_{C 1}\right\rangle+\left\langle v_{L_{\mu}}\right\rangle=0$. Thus $V_{1}=v_{C 1}$. We know that the key to finding voltage conversion ratios is to apply volt-second balance to the inductors, so let's do that. When the switch is on we have $v_{L 1}=V_{1}$ and $v_{L \mu}=v_{C 1}$ (where we have assumed inductor voltage polarity according to passive sign convention). When the switch is off we have $v_{L 1}=$ $V_{1}-v_{C 1}-N_{1} V_{2} / N_{2}$ and $v_{L \mu}=-N_{1} V_{2} / N_{2}$. Thus,

$$
\begin{align*}
D\left(V_{1}\right)+(1-D)\left(V_{1}-v_{C 1}-\frac{N_{1}}{N_{2}} V_{2}\right) & =0  \tag{1}\\
D\left(v_{C 1}\right)+(1-D)\left(-\frac{N_{1}}{N_{2}} V_{2}\right) & =0 \tag{2}
\end{align*}
$$

[^0]Since we've already worked out that $V_{1}=v_{C 1}$, these equations are telling us the same thing (if we hadn't worked that out by inspection, we could solve these two equations to determine that). The conversion ratio is therefore

$$
\begin{equation*}
\frac{V_{2}}{V_{1}}=\frac{N_{2}}{N_{1}} \frac{D}{1-D} \tag{3}
\end{equation*}
$$

(b) Recall that device stress is the product of the peak voltage the device must block and the peak current it must carry. In "heavy" continuous conduction mode (meaning we are very far from discontinuous conduction mode operation), we expect relatively small ripple current, so it's reasonable to assume that the inductor currents are dc. We aren't explicitly told anything about the ripple voltage, so we'll assume that they're small. Ripple voltages are usually small since we generally want input and output voltage ripple to be small. If they weren't small, then that's important and against our expectation, and we would expect to be told about that.

When the switch is on, the diode is off. The peak switch current $\left(I_{q}\right)$ and diode voltage $\left(V_{d}\right)$ are:

$$
\begin{array}{r}
I_{q, p k}=I_{L 1}+I_{L \mu} \\
V_{d, p k}=-\frac{N_{2}}{N_{1}} V_{C 1}-V_{2} \tag{5}
\end{array}
$$

We haven't worked out what the average values of the inductor currents are, so let's do that. Inductor $L 1$ is in series with the input, so its average current is the same as the average input current $I_{1}$. Inductor $L_{\mu}$ is a little bit more complicated, but we can figure out its average current by applying capacitor charge balance to $C_{1}$ (i.e. enforce $I_{C 1}=0$ ). When the switch is on, the capacitor carries $-I_{L \mu}$. When the switch is off, the capacitor carries $I_{L 1}=I_{1}$. Thus we have $-D I_{L \mu}+(1-D) I_{1}=0$ and $I_{L \mu}=(1-D / D) I_{1}$.

We can now simplify the peak switch current and peak diode voltage expressions:

$$
\begin{array}{r}
I_{q, p k}=I_{1}\left(1+\frac{1-D}{D}\right)=\frac{I_{1}}{D} \\
V_{d, p k}=-\frac{N_{2}}{N_{1}} V_{1}-V_{2}=-\frac{N_{2}}{N_{1}} \frac{V_{1}}{1-D} \tag{7}
\end{array}
$$

When the switch is off, the diode is on, and we have:

$$
\begin{gather*}
V_{q, p k}=\frac{N_{1}}{N_{2}} V_{2}+V_{C 1}=\frac{V_{1}}{1-D}  \tag{8}\\
I_{d, p k}=\frac{N_{1}}{N_{2}}\left(I_{L 1}+I_{L \mu}\right)=\frac{N_{1}}{N_{2}} \frac{I_{1}}{D} \tag{9}
\end{gather*}
$$

Thus, the device stresses are

$$
\begin{align*}
\left|I_{q, p k} V_{q, p k}\right| & =\frac{I_{1}}{D} \frac{V_{1}}{1-D}=\frac{P_{1}}{D(1-D)}  \tag{11}\\
\left|I_{d, p k} V_{d, p k}\right| & =\frac{I_{1}}{D} \frac{V_{1}}{1-D}=\frac{P_{1}}{D(1-D)} \tag{12}
\end{align*}
$$

Does this mean that the switch stress is independent of the transformer turns ratio? Technically, yes! The device stresses only depend on the power throughput of the converter and the duty ratio we operate at, and it's minimized for operating at $\mathrm{D}=0.5$. You could build this converter with a transformer that has a 100:1 or 1:1 turns ratio and in either case $\mathrm{D}=0.5$ would be the condition that minimizes switch stress (assuming $P_{1}$ is independent of D...).

The critical caveat is that we usually have an input/output voltage specification. In this problem, it's $V_{1}=12 \mathrm{~V}$ and $V_{2}=60 \mathrm{~V}$. The benefit of the transformer is that it lets us set $\mathrm{D}=0.5$ while satisfying this voltage gain by the appropriate choice of $N_{1}: N_{2}$. Here, to get our optimal $\mathrm{D}=0.5$, we'd set $N_{2}: N_{1}=5: 1$.
(c) For a non-isolated indirect converter, the stress parameter is

$$
\left(\left|V_{1}\right|+\left|V_{2}\right|\right)\left(\left|I_{1}\right|+\left|I_{2}\right|\right)=\frac{P}{D(1-D)}
$$

While the voltage conversion ratio is

$$
\left|\frac{V_{2}}{V_{1}}\right|=\frac{D}{1-D}
$$

. Given the same input and output voltage, the duty ratio of the non-isolated converter is $D=$ $5 / 6$, hence the stress parameter for both devices is $7.2 P_{1}$, while the isolated SEPIC converter with $D=0.5$, has a stress parameter of $4 P$. We can see that the non-isolated indirect converter has higher stress than its isolated counterpart, in particular because it does not have the freedom to choose an optimal duty ratio.
(d) Note that even though we have small current ripple in this converter, the magnetizing inductor still carries average current and this current is comparable to the input current $\left(I_{L \mu}=(1-D / D) I_{1}\right)$. This average magnetizing current is associated with energy storage in the magnetizing inductance in our model $\left(E_{\text {stored }}=L I_{\mu}^{2} / 2\right)$, which physically represents the energy stored in the magnetic path that couples the primary and the secondary. This means that we are using the transformer as an energy storage element and we should the gap the core.

Why is gapping better for energy storage? The energy density (in $\mathrm{J} / \mathrm{m}^{3}$ ) of a magnetic field having flux density $B$ in a material with permeability $\mu$ is $B^{2} /(2 \mu)$. Thus, the lower the permeability is, the better your energy density is for the same flux density (i.e. you can store more energy in a given volume, or the same energy in a smaller volume). In a gapped or ungapped core there is a practical limit on flux density, $B_{s a t}$, associated with avoiding saturation of the core material. In this limit, a gapped core will have a region where $B_{\text {sat }}$ flows through air with permeability $\mu_{0}$ while an ungapped core has $B_{\text {sat }}$ only flowing through the core which has a much larger permeability than air. This means the ungapped core has a much lower maximum energy density and you'd need a much larger core to store the same energy that you could store if you used a smaller core with a gap!


Figure 1: The current waveforms associated with the double-ended full-bridge converter of problem 7.3 when $I_{\mu p}>I_{2} / N$. D5 and D8 or D6 and D7 remaining off from DT to T

## 3 KPVS 7.3

Assume the circuit operates with the same switching sequence as given in Example 7.3 of the text. At the start of the period $D T$ at $t=0$, we assume $i_{\mu}(0)=-I_{\mu p}$. During $D T, S_{1}, S_{4}, D_{5}$ and $D_{8}$ are conducting, and the primary current is

$$
i_{P}=\frac{1}{N} I_{2}+\frac{1}{L_{\mu}} \int_{0}^{t} V_{1} d t-I_{\mu p}
$$

Note that $i_{P}$ starts negative because $I_{\mu p}>I_{2} / N$. At $t=D T, i_{\mu}=I_{\mu p}$ (assuming operation in periodic steady state), and $S_{1}$ turns off and $S_{3}$ turns on, maintaining a path for $i_{\mu}$. With $v_{P}=0$ during $(1-D) T, i_{\mu}=I_{\mu p}$ until $S_{4}$ turns off and $S_{2}$ turns on at $t=T$. Figures 1 and 2 shows the resulting waveforms depending on the operation of the diodes.


Figure 2: The current waveforms associated with the double-ended full-bridge converter of problem 7.3 when $I_{\mu p}>I_{2} / N$. Freewheeling through the diodes from DT to T

## 4200 W off-line converter

(a) The provided schematic is a a little dense, but a lot of what's making it dense isn't the main power con- verter, it's the control and sensing. Starting from the ground of C 3 and C 4 we run into a transformer TR2, this transformer has its secondary connected to the control chip so we know it's being used for control rather than being fundamental to the main power transfer mechanism of the converter (it looks like it's used for sensing input current). From there we go to transformer TR1 which has a single pri- mary and multiple identical secondaries, and we can recognize the secondaries as each being the secondary of a forward (also known as an isolated buck) converter. The forward converter must have a switch in series with the transformer and indeed we see Q1 doing that. So, a forward converter is at the core of this converter.
(b)The conversion ratio of an isolated buck converter is $V_{o} / V_{i n}=\frac{N_{s}}{N_{p}} D$. For $V_{o}=5 V, V_{i n}=$ $340 V, N_{s}=1, N_{p}=16$ we have $D=0.235$.


Figure 3: Equivalent circuit of the tapped-inductor boost converter in problem 7.25.
(c)The different secondaries have a ratiometric voltage relationship $(+5 \mathrm{~V},+15 \mathrm{~V},-15 \mathrm{~V})$. This is a textbook situation for a series transformer since we can simply achieve the different voltage scalings by the appropriate selection of secondary turns. Note that we also assumed in Part B that $V_{o}$ and $V_{i n}$ are proportional to $\frac{N_{s}}{N_{p}}$, and a series wound transformer is consistent with that assumption.

## 5 KPVS 7.25

(a) The two segments in the tapped inductor can be viewed as the two windings of a transformer. First, we'll place a magnetizing inductance $L_{\mu}$ in parallel with the $N_{1}$ segment, then we'll redraw the tapped inductor in the more familiar transformer form shown in Fig. 3.

We are told that the inductance of the entire $N_{1}+N_{2}$ turn winding is $L$.

$$
L=\frac{\left(N_{1}+N_{2}\right)^{2}}{\mathcal{R}}
$$

The inductance associated with $N_{1}$ turns in this winding is $L_{\mu}$,

$$
L_{\mu}=\frac{N_{1}^{2}}{\mathcal{R}}
$$

Thus, we can express $L_{\mu}$ in terms of $L$ as

$$
L_{\mu}=\left(\frac{N_{1}}{N_{1}+N_{2}}\right)^{2} L
$$

(b) To determine the voltage conversion ratio, we can enforce inductor volt-second balance. When
the switch is on, $V_{\mu}=V_{1}$. When the switch is off, we have

$$
V_{1}-V_{\mu}-V_{x}-V_{2}=0
$$

where

$$
V_{x}=\frac{N_{2}}{N_{1}} V_{\mu}
$$

Thus, when the switch is off

$$
V_{\mu}=\frac{V_{1}-V_{2}}{1+\frac{N_{2}}{N_{1}}}
$$

Applying volt-second balance,
$D V_{1}+(1-D) \frac{V_{1}-V_{2}}{1+\frac{N_{2}}{N_{1}}}=0 \Rightarrow \frac{V_{2}}{V_{1}}=\frac{D \frac{N_{2}}{N_{1}}+1}{1-D}$
(c) When $N_{1}=N_{2}$ we have

$$
\frac{V_{2}}{V_{1}}=\frac{D+1}{1-D}
$$

When $N_{2}=0$, we have

$$
\frac{V_{2}}{V_{1}}=\frac{1}{1-D}
$$

which is the conversion ratio for a conventional boost converter. These conversion ratios are plotted in Fig. 4.


Figure 4: Conversion ratios for the tapped-inductor boost converter in problem 7.25.

## 6 KPVS 24.2-Switching Loss with R Load

The switching transitions studied in class assumed a constant current load demanding a certain total current supplied either by the switch or the diode, and the diode can only turn on once voltage across the device has risen to $V_{d c}$. In this problem, we study a transition where the load is purely resistive, as shown in Fig. 5.


Figure 5: A switching scenario with resistive "load"

As the switch turns on, $I_{s w}$ rises, with a resistive load the $V_{s w}$ has to fall at the same time. (Compare this to the inductive case, where $V_{s w}$ is kept at $V_{d c}$ until $I_{s w}$ reaches load current.)

Similarly at turn off, $V_{s w}$ rises at the same time as $I_{s w}$ falls. ( $V_{d c}-V_{s w}=I_{s w} \cdot R$ always holds.) The time-domain plot and switching locus are given in Fig. 6 and Fig. 7 respectively.


Figure 6: Switch Waveforms for both Transitions with Resistive Load


Figure 7: Switching locus. As $V_{s w}$ and $I_{s w}$ transitions simultaneously, the locus is friendlier than the constant I load case

The energy dissipated during turn on is:

$$
\begin{aligned}
W_{o n} & =\int_{0}^{t_{r}} V_{s w} I_{s w} d t \\
& =\int_{0}^{t_{r}}\left(V_{d c}-V_{d c} \frac{t}{t_{r}}\right)\left(\frac{V_{d c}}{R} \frac{t}{t_{r}}\right) d t \\
& =\frac{V_{d c}^{2} t_{r}}{6 R}
\end{aligned}
$$

and by symmetry, the energy dissipated during turn-off is $\frac{V_{d c}^{2} t_{f}}{6 R}$.

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### 6.622 Power Electronics

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[^0]:    *Mansi Joisher 2023 (adapted from Yang 2022, Boles 2021, Ranjram 2020)

