MASSACHUSETTS INSTITUTE OF TECHNOLOGY
Department of Electrical Engineering and Computer Science

6.622 Power Electronics — Issued: March 13, 2023
Problem Set 5 — Due: March 20, 2023

Reading: KPVS Chapter 26 through 26.3; Texas Instruments Application Note AN-2020 "Thermal Design"; KPVS Chapter 8 though 8.2

Problem 5.1 KPVS Problem 25.4

Problem 5.2

Consider the thermal model suggested in Figure 3 and Table 1 of the model in Texas Instruments application note AN-2020 page 4.

We often transfer heat through a printed circuit board mounted to a heat sink mounted on the opposite side of the circuit board, using a "via farm" – a dense collection of vias placed to aid heat transfer vertically through the circuit board. Consider that we would like to transfer heat from the bottom of a device package soldered to the top of a pcb vertically through the pcb to a heatsink attached to the bottom of the pcb.

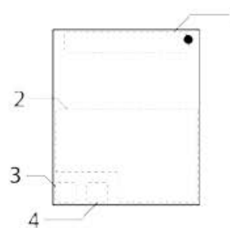
a. Consider vertical heat transfer through 1 cm^2 area of a circuit board. *Without* thermal vias, what would be the thermal resistance of the vertical heat path through a 63 mil (0.063", 1.6 mm) thick FR4 printed circuit board over an area of 1 cm^2 ? How many 12-mil 1-oz plated vias would one seek to place in that 1 cm^2 area to reduce the thermal resistance of the vertical path to below 25 °C/W? (Note that AN-2020 only provides numbers for a 12-mil thick section of printed circuit board.) If the pcb process requires a minimum spacing of 8 mils *between* holes (edge to edge), is this density achievable? (Note, we could also further reduce thermal resistance by using a pcb process that would allow the vias to be completely filled with copper or another thermally-conductive material.)

b. Consider the GaN Systems GS66508B transistor used on a printed circuit board having similar characteristics and constraints as in part a. (a subset of the datasheet for the transistor is shown in Fig. 1.) In the circuit considered in this problem, the transistor is used such that its source is electrically connected to system ground on the printed circuit board, with a thermal via farm placed under the source pad connecting to a water-cooled heatsink mounted on the opposite side of the board. Consider the conservative case of heat transfer *only* to the heatsink and *only* through the portion of the pcb directly under the transistor, and assume that the heatsink is able to maintain the back surface of the board at 85 °C. Propose a via-farm design for the board (indicating how many thermal vias you will utilize), assuming that the thermal vias can only be placed under the source pad. How much power can we dissipate in the transistor if we limit the junction temperature to a conservative value of 125 °C?

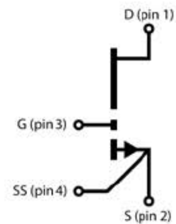
Features

- 650 V enhancement mode power switch
- Bottom-side cooled configuration
- $R_{DS(on)}$ = 50 mΩ
- $I_{DS(max)}$ = 30 A
- Ultra-low FOM Island Technology® die
- Low inductance GaN*PX*® package
- Easy gate drive requirements (0 V to 6 V)
- Transient tolerant gate drive (-20 V / +10 V)
- Very high switching frequency (> 10 MHz)
- Fast and controllable fall and rise times
- Reverse current capability
- Zero reverse recovery loss
- Small 7.1 x 8.5 mm² PCB footprint
- Source Sense (SS) pin for optimized gate drive
- RoHS 6 compliant

Package Outline



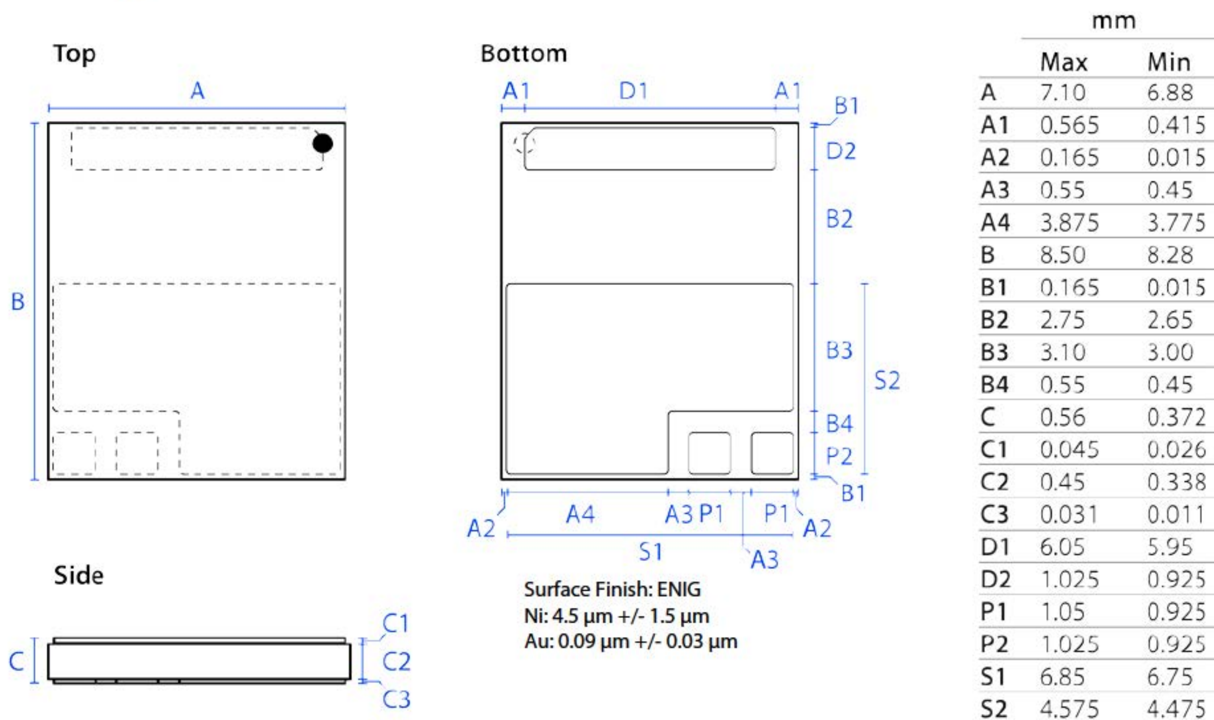
Circuit Symbol



Thermal Characteristics (Typical values unless otherwise noted)

Parameter	Symbol	Value	Units
Thermal Resistance (junction-to-case) – bottom side	$R_{\Theta JC}$	0.5	°C /W

Package Dimensions



	mm	
	Max	Min
A	7.10	6.88
A1	0.565	0.415
A2	0.165	0.015
A3	0.55	0.45
A4	3.875	3.775
B	8.50	8.28
B1	0.165	0.015
B2	2.75	2.65
B3	3.10	3.00
B4	0.55	0.45
C	0.56	0.372
C1	0.045	0.026
C2	0.45	0.338
C3	0.031	0.011
D1	6.05	5.95
D2	1.025	0.925
P1	1.05	0.925
P2	1.025	0.925
S1	6.85	6.75
S2	4.575	4.475

Figure 1 Segments of the datasheet for the GaN Systems GS66508B transistor.

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Problem 5.3

See the data sheet for an International Rectifier power MOSFET IRF620S; pay special attention to the first page and figs. 3, 4, and 7–11. Assume a maximum allowable junction temperature of 150 ˚C and a maximum ambient temperature of 50 ˚C for this problem. (Note that the on-state resistance of the MOSFET varies with junction temperature, as illustrated in datasheet Fig. 4.)

a. Assume that the device must carry a (forward) rms current of 2.5 A, and that switching losses can be ignored. The MOSFET is attached to a heat sink using an insulating pad with a maximum thermal resistance of 0.75 ˚C/W. What is the maximum allowable thermal resistance of the heat sink?

b. Suppose the device is instead operated in a pulsed fashion, carrying large pulses of current 1 ms in duration with 99 ms of off time between pulses. If the device is mounted to an extremely good heat sink that maintains the *case* temperature at 50 ˚C, what is the maximum allowable current pulse magnitude? You may assume that the MOSFET on-state resistance is always at its 150 ˚C value.

Problem 5.4 KPVS Problem 7.3

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