6.6220 HW5 Solutions*

5.1 KPVS 25.4 - Common Heat Sink

5.1.A Thermal Model

With two transistors sharing one heat sink, a thermal circuit analogy can be created as shown in Fig. 1. Where according to the given values, $R_{\theta jC} = 1.2\,^\circ\text{C/W}$, $R_{\theta CS} = 0.2\,^\circ\text{C/W}$ and $R_{\theta SA} = 1.2\,^\circ\text{C/W}$.

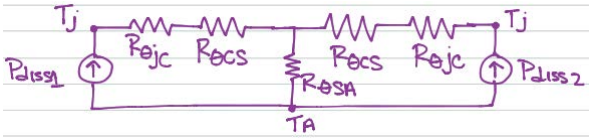

Figure 1: A Thermal Circuit Model with Shared Heat Sink

5.1.B Maximum Power for Two Devices

Applying KCL and KVL in the thermal circuit, denoting the dissipated power of the two devices $P_{diss1} = P_{diss2} = P_{diss}$, we have

$$T_j = T_A + P_{diss}(2R_{\theta SA} + R_{\theta jC} + R_{\theta CS}) \le 150\,^\circ\text{C}$$
$$\implies P_{diss} \le 36.67\,\text{W}$$

The maximum total power is thus $P_{total} = 2P_{diss} \approx 73.34\text{W}$.

5.1.C Maximum Power for One Device

If only one device is operating, we have a reduced circuit as shown in Fig. 2. Here similarly we have

$$T_j = T_A + P_{diss}(R_{\theta SA} + R_{\theta jC} + R_{\theta CS}) \le 150\,^\circ\text{C}$$
$$\implies P_{diss} \le 50\,\text{W}$$

The maximum total power dissipation is thus $P'_{total} = 50\,\text{W}$.

*Updated by Mansi Joisher (adapted from Yang 2022, Ranjram 2020)

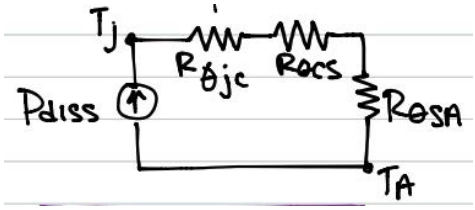

Figure 2: Reduced Thermal Circuit Model

5.2 Thermal Modeling of Vias

5.2.A

FR4 Vertical Thermal Resistance: We can read the thermal resistivity ρ_{FR4} from AN-2020, and the thermal resistance of the vertical heat path through a 1.6 mm thick FR4 PCB is

$$R_{FR4} = \frac{\rho_{FR4} \cdot t}{A} = 435\frac{^\circ\text{Ccm}}{\text{W}} \times \frac{1.6\,\text{mm}}{1\,\text{cm}^2} \approx 69.6\,^\circ\text{C/W}$$

Vertical Thermal Resistance with Vias: For a via, the cross-sectional area can be computed from the total area ($\pi \times (6mil)^2$) minus the inner area for 1 oz plating, which is ($\pi \times (6mil - 35\mu m)^2$). So the vertical thermal resistance of a single via is

$$\begin{aligned} R_{via} &= \frac{\rho_{cu} t}{A} \\ &= 0.25\frac{^\circ\text{Ccm}}{\text{W}} \times \frac{1.6\,\text{mm}}{\pi(6\,\text{mil})^2 - \pi(6\,\text{mil} - 35\,\mu\text{m})^2} \\ &\approx 134.83\,^\circ\text{C/W} \end{aligned}$$

To get the via farm's total thermal resistance down to 25 °C/W, we can neglect the contribution of the FR4 substrate for safety margins and only count the vias, we would need at least $\frac{134.83}{25} \approx 5.39 \approx 6$ vias. Since the vias are only 12 mils (0.03 cm) in diameter and the minimal edge-to-edge clearance is 8mils (0.02 cm), we can easily fit 6 vias in a 1 cm by 1 cm square area.

If we do consider the thermal resistance of FR4, we may assume it's in parallel with the via's thermal resistances, and we would need at least ($\frac{1}{25}$ −

$\frac{1}{69.6}) \times 134.83 \approx 3.43 \approx 4$ vias. Though it is always recommended to leave considerable margins.

Via Placement: One way of placing the vias is as shown in Fig. 3. We used minimum via spacing of 8mils, and it can be shown that the vias take only approx. 0.015 cm^2. If we use hexagonal instead of in-grid placements, we can possibly fit even more. Nevertheless this is just to prove that the $1cm^2$ area we're given is more than enough to fit the vias.

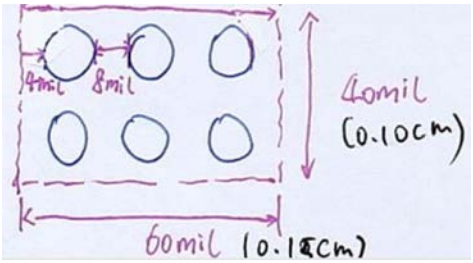

Figure 3: One Way of Placing Vias, in a 2 by 3 Array

5.2.B Max Pdiss for GAN transistor

The equivalent thermal model for the system is shown in Fig. 4. The thermal resistance of the via and FR4 are the same as part a. The vias can be only placed under the source pad. Hence, the maximum number of vias placed under the source pad in a rectangular pattern is 13*5 + 7*2 = 79 as shown in Fig. 4.

$$T_j = T_s + P_{diss}(R_{\theta JC} + \frac{1}{\frac{1}{R_{\theta FR4}} + \frac{number\ of\ vias}{R_{\theta via}}})$$
$$\implies P_{diss}max = 18.46\ \text{W}$$

Maximum power that can be dissipated through the transistor is 18. 46 W,

5.3 IRF620S Thermal Design

From the datasheet we can read the following parameters: standard $R_{DS,on} = 0.8\Omega$, the junction-to-Case thermal resistance $R_{\theta jC} = 2.5°C/W$, and Case-to-Sink $R_{\theta CS} = 0.75°C/W$. Our design choice is to find a suitable Sink-to-Ambient $R_{\theta SA}$.

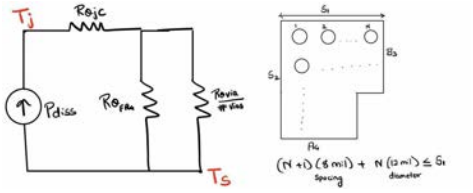

Figure 4: Thermal model and placement of vias under source pad in a rectangular pattern

We can then construct a simple thermal circuit model, with worst-case ambient temperature at $T_A = T_{A,max} = 50°C$.

From the datasheet Fig. 4, we can also find the on-state resistance normalization factor, at the worst case of $T_j = 140°C$, the factor is approx. 2.125. Hence the dissipate power can be estimated as

$$P_{diss} = I_{rms}^2 \cdot R_{on} \cdot 2.25 \approx 11.25\ \text{W}$$

And the maximum allowable heat sink thermal resistance is

$$R_{\theta SA} \leq \frac{T_j - T_A}{P_{diss}} - R_{\theta jC} - R_{\theta CS}$$
$$\leq 5.84°C/W$$

(b) For the 1ms on, 99ms off pulsed operation, and with an assumed constant case temperature at 50°C, we can use the thermal response characteristic to calculate the maximum allowed current.

From the datasheet Fig. 11, we can read the junction-to-case thermal impedance. With an 0.01 duty ratio and 1ms rectangular pulse duration, the junction-to-case thermal impedance $Z_{\theta JC} \approx 0.25°C/W$. With the on-state resistance at its 150°C value, i.e. $R_{DS,on}|_{T_j=150°C} \approx 0.8\Omega \cdot 2.25 \approx 1.8\Omega$, we can write

$$P_{diss,max} = I_{pk}^2 R_{DS,on}|_{T_j=150°C} \leq \frac{T_j - T_C}{Z_{\theta JC}}$$
$$\implies I_{pk} \leq \sqrt{\frac{150°C - 50°C}{0.25°C/W \times 1.8\Omega}}$$
$$\leq 14.89\ \text{A}$$

Note that the thermal response is with reference to instantaneous power dissipation in the pulse and

not the average power, so peak on-stage current instead of rms or average current should be used.

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