December 20, 2002 - Final Exam

Name: _____

General guidelines (please read carefully before starting):

- Make sure to write your name on the space designated above.
- **Open book**: you can use any material you wish.
- All answers should be given in the space provided. Please do not turn in any extra material.
- You have **three hours** to complete your quiz.
- Make reasonable approximations and *state them*, i.e. low-level injection, extrinsic semiconductor, quasi-neutrality, etc.
- Partial credit will be given for setting up problems without calculations. **NO** credit will be given for answers without reasons.
- Use the symbols utilized in class for the various physical parameters, i.e. N_c, τ, $\mathcal{E}$, etc.
- Pay attention to problems in which *numerical answers* are expected. An algebraic answer will not accrue full points. Every numerical answer must have the proper *units* next to it. Points will be subtracted for answers without units or with wrong units. In situations with a defined axis, the *sign* of the result is also part of the answer.
- If needed, use the doping-dependent Si parameters graphed throughout del Alamo's notes.
- If needed, use physical parameters for silicon at room temperature listed in Appendix B of del Alamo's notes.
- If needed, use the values of fundamental constants listed in Appendix A of del Alamo's notes.

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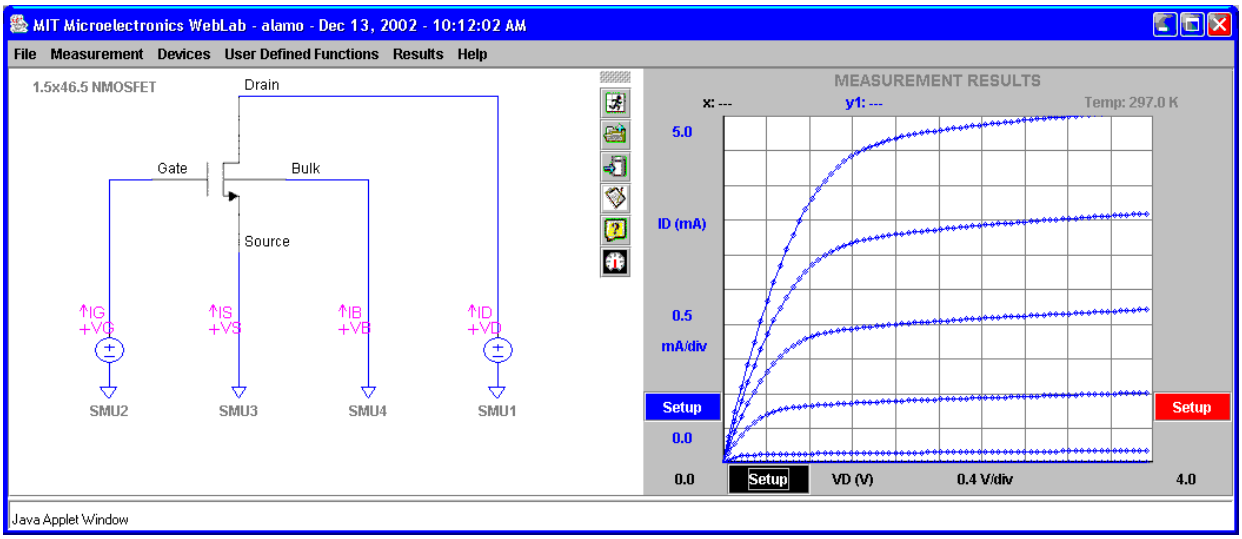
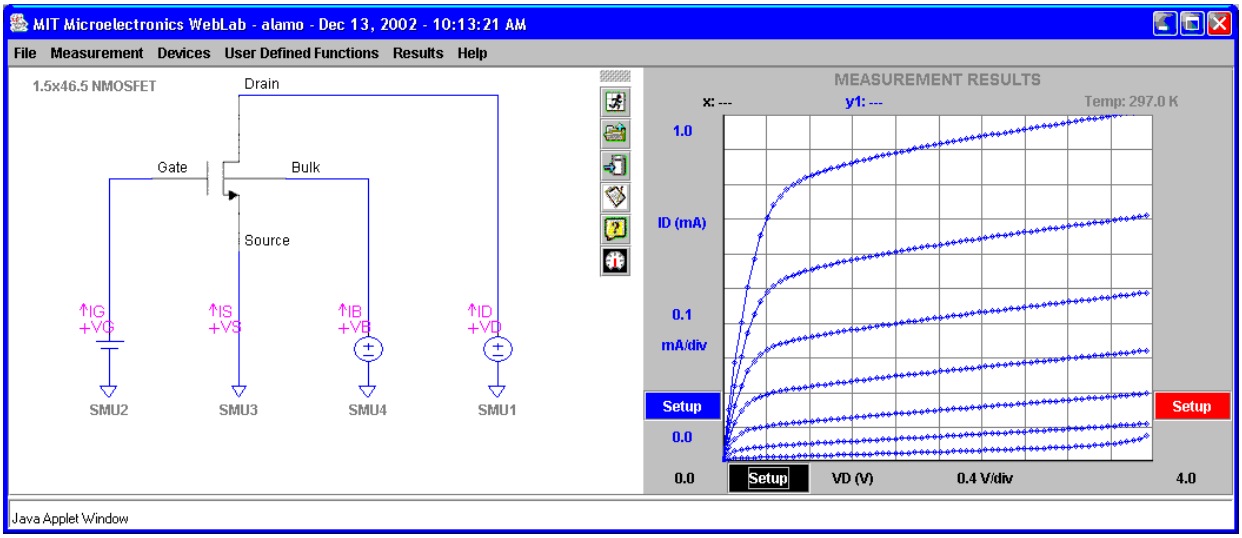
1. *(25 points)* Below are two screen shots of weblab measurements taken on a 1.5x46.5 μm NMOSFET. The first one shows the output characteristics obtained for $V_{SB} = 0\ V$, and V_{GS} from 0 to 3 V, in steps of 0.5 V. The second one shows the output characteristics obtained with the roles of the gate and body reversed. In these, $V_{GS} = 1.5\ V$ and V_{SB} is stepped from 0 V to 3 V, in steps of 0.5 V.





As we discussed in class, the body of the MOSFET behaves as a gate and reasonably looking output characteristics are obtained.

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a) *(10 points)* One of the most striking differences between the two sets of output characteristics is V_{DSsat}. The characteristics obtained with the body operating as the main gate seem to display remarkably smaller values of V_{DSsat} than in the normal mode. This question is about understanding the origin of this.

Derive a simple expression for V_{DSsat} as a function of V_{SB} for an ideal MOSFET. Do not include the "body effect" (but obviously include the "back bias" effect). Is this expression consistent with the data above? Explain.

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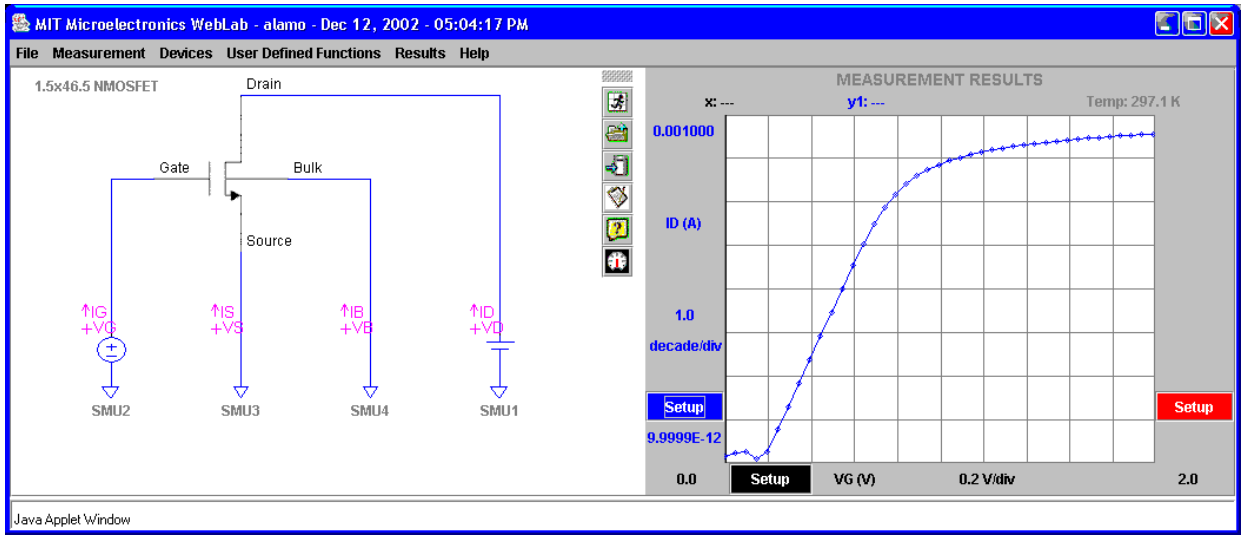
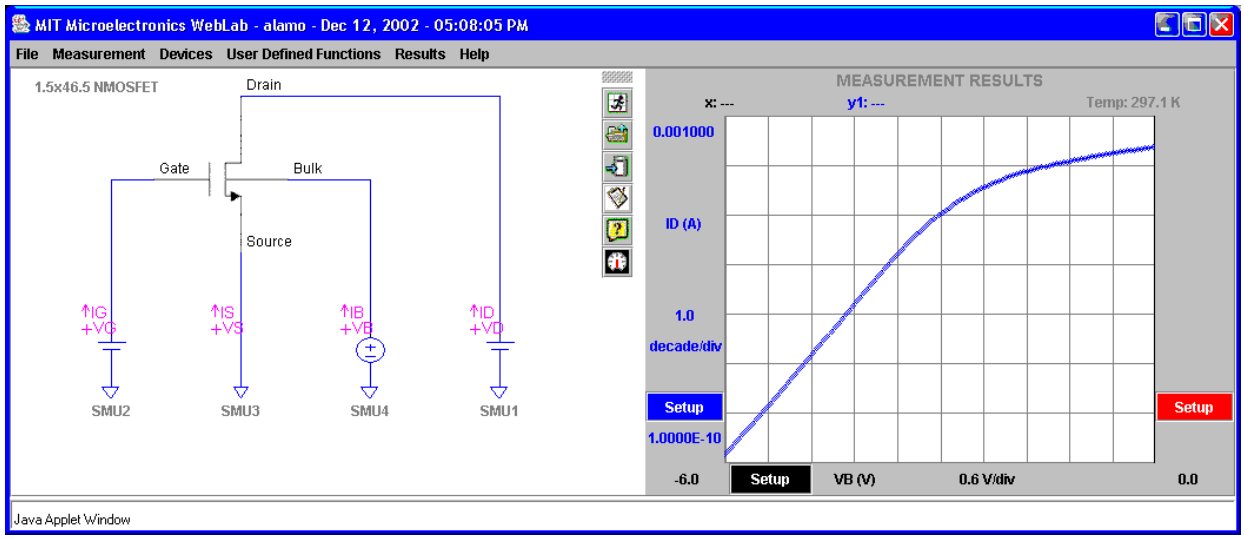
Below are the subthreshold characteristics obtained for this MOSFET for both modes of operation. In the normal mode (top), $V_{SB} = 0$. In the mode in which the body is used as gate (bottom), $V_{GS} = 1.5\ V$. In both cases, $V_{DS} = 0.1\ V$.





A remarkable difference is also observed here: the subthreshold slope of the device in the normal mode is significantly sharper than in the mode in which the body is used as the main gate.

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b) *(10 points)* Derive an expression for the relationship between the inverse subthreshold slope of a MOSFET in the normal mode and in the gate-reversed mode. Explain your result.

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c) *(5 points)* From the experimental characteristics of the previous page, extract the subthreshold slope of this device for both modes of operation. Compare their relationship with that predicted with the equation derived above. Discuss.

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2. *(10 points)* Consider a n-channel MOSFET process from the 0.18 μm-technology generation characterized by $x_{ox} = 4.5\ nm$ and $V_T = 0.3\ V$. Estimate the sheet resistance of the inversion layer for $V_{GS} = 1.8\ V$.

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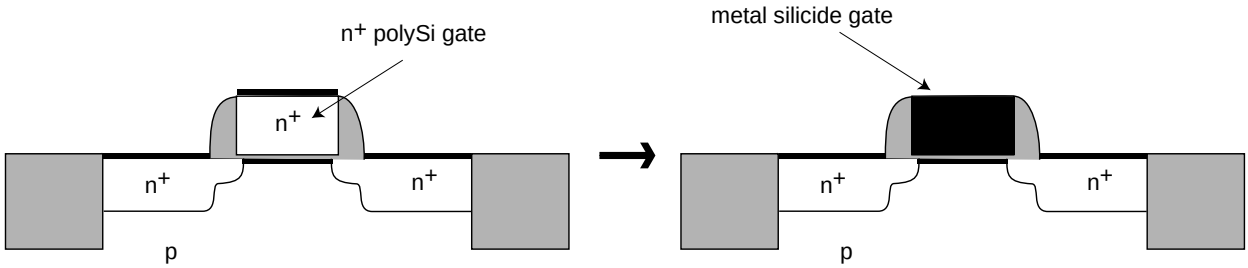
3. *(15 points)* At the 2002 International Electron Devices Meeting last week, there were a number of papers that demonstrated a new technique to fully silicide the gate of MOSFETs. This is done by depositing a suitable metal on top of the polySi gate and then reacting it at high temperature until all the gate polySi is completely consumed. The remaining metal is then removed. This is sketched in the figure below:



This problem is about examining the changes that occur to the MOSFET device characteristics as a result of the complete silicidation of the gate. The key change that complete silicidation introduces in an n-channel MOSFET is an increase in the gate work function. To the first order, nothing else is changed.

Indicate the impact of the *increase* of the gate metal work function on the parameters and figures of merit listed below. Circle one: *increase* $=\uparrow$, *decrease* $=\downarrow$, or *no effect*. For each item, give the reason for your choice *(no reason, no points)*.

-threshold voltage, V_T: $\uparrow \quad \downarrow \quad no\ effect$

-effective inversion layer mobility at a given V_{gs}, μ_{eff}: $\uparrow \quad \downarrow \quad no\ effect$

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-inverse subthreshold slope, S (in units of mV/dec): $\uparrow$ $\downarrow$ $no\ effect$

-off-state current, I_{off}: $\uparrow$ $\downarrow$ $no\ effect$

-minimum achievable gate length for a given $DIBL$ criteria: $\uparrow$ $\downarrow$ $no\ effect$

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4. *(25 points)* At the 2002 IEDM, a world record SiGe HBT (Heterojunction Bipolar Transistor) was presented. The device featured an $f_T = 350\ GHz$, almost twice as high as the best result presented last year at the 2001 IEDM. This problem is about studying in some detail the reported results. To the first order, you can think of this transistor as a regular Si bipolar junction transistor.

The following table gives the value of f_T at two different collector current levels , as reported in the paper ($V_{CB} = 1\ V$):

$I_C\ (mA)$	$f_T\ (GHz)$
0.2	70
6	350

$I_{Cpk} = 6\ mA$ is the collector current at which f_T peaks. In the paper, the emitter-base junction area is listed as $A_E = 0.12 \times 2.5\ \mu m^2$. The current gain is listed as $\beta_F = 2300$.

a) *(5 points)* Estimate the collector doping level *(numerical answer expected).*

b) *(5 points)* Estimate the sum of the emitter-base and base-collector junction capacitances *(numerical answer expected).*

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c) *(5 points)* Estimate the intrinsic delay *(numerical answer expected)*.

d) *(5 points)* Estimate the quasi-neutral base width *(numerical answer expected)*.

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e) *(5 points)* At $I_C = I_{C,pk}$, estimate the total minority carrier charge in the device *(numerical answer expected)*.

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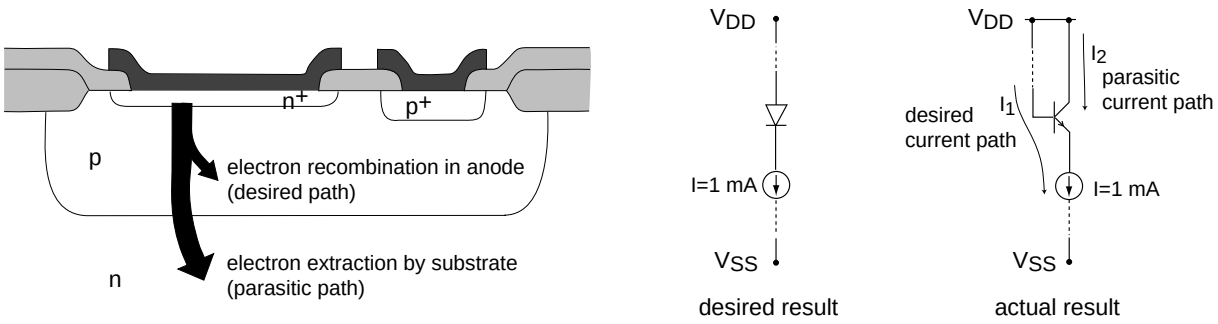
5. *(25 points)* The figure below is a modified version of Fig. 7.26 in the notes. It describes the isolation problem when implementing pn diodes in a CMOS process. Depicted is a n^+-p diode implemented using a n-MOSFET. The source/drain n^+ diffusion is used as the diode cathode. The p-type well is used as the diode anode. The p^+ body contact is used as the anode contact. Surrounding the p-type anode is the n-type substrate which is connected to the most positive voltage of this circuit, V_{DD}.



The problem with this "diode" is that it is actually a parasitic vertical npn bipolar transistor. Depending on the circuit environment, the actual current path can be very different from the desired current path.

An example is shown on the right where this "diode" is connected somewhere half way between V_{DD} and V_{SS}, where V_{DD} is the positive rail of the circuit and V_{SS} is the negative rail. Immediately below the diode is a current source pulling down 1 mA. Ideally, this current should entirely flow from anode to cathode in the diode. Since this is in reality a bipolar transistor, some of this current can be diverted to the substrate through the bipolar effect and flow through a separate path, I_2. As a result, the current through the desired path, I_1, can be less than the intended value of 1 mA. The end result might be circuit misfunction. Computing these currents is the goal of this problem.

Here are specs for the three key regions:

region	type	doping level (cm^{-3})	thickness (μm)
cathode	n^+	10^{19}	0.05
anode	p	10^{17}	0.2
substrate	n	10^{16}	400

The area of the n^+p junction is 100 μm^2.

a) *(5 points)* Under the conditions indicated above, identify the emitter, the base and the collector of this bipolar transistor. In what regime is this bipolar transistor biased?

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b) *(10 points)* Estimate the current gain of the bipolar transistor in the configuration indicated above *(numerical answer expected)*.

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c) *(5 points)* Estimate I_1 and I_2 *(numerical answer expected).*

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d) *(5 points)* Quantitatively sketch the excess minority carrier concentration across the base of the parasitic BJT.

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