JUDY HOYT: In a polycrystalline state, or it can be grown epitaxially, which epitaxially-- "epitaxial" is a Greek word, which means, having the same crystal structure as the substrate. So silicon itself can be deposited. And we'll talk about that in the next couple of lectures. So we're going to talk about the methods, the equipment, and some basic concepts used to deposit or grow the-- these thin films.

So let's just go back to a picture that I think I showed earlier in the course. But it's a cross-section view of, say, devices in a CMOS chip. And we've got our silicon substrate down here at the bottom. We've talked a lot about how to create n-wells and p-wells by ion planting, and diffusing, and the source drains, and all that. But there are a lot of other films here besides silicon substrate. So everything that's in a color, other than white here, is some other film.

For example, here, we might have copper that's used in the interconnect wiring, or aluminum, or tungsten. The-- shown here in this bright magenta. These hatched regions that are blue could be a low temperature oxide. Now, it's a deposited oxide, very different from a grown oxide. So we're going to talk about how we deposit oxides by a process called chemical vapor deposition. Or it might not be oxide. It could be generally referred to as an interlayer dielectric in between some of the metal layers, and that has a low dielectric constant.

And we'll talk about that in a little minute, why we want that. Other films that are absolutely critical for the MOSFET itself. We haven't talked about it. We've been talking about polysilicon gates. So far, I just draw them in in PowerPoint just by slapping them in there. But they don't get slapped in PowerPoint. They have to be deposited. So we'll talk a little bit about the deposition of polycrystalline silicon, which is critical, the deposition of the materials that are going to form the spacers, which is either this bright green silicon nitride, again, deposited, or it could be low-temperature oxide.

So there are a lot of different materials that we want to talk about, and how they go down. Besides how they go down, there are some requirements, or goals, if we go onto slide number three, for thin-film deposition. We need to be able to control the material composition. So either a stoichiometric SiO2, for example, or a silicon 3 N4 for silicon nitride, or it could be a oxynitride, a mixture of silicon, oxygen, and nitrogen.

But we need to be able to have a process that reliably controls the atomic composition. We would like to have low contamination in general to-- in order to control the electrical and optical properties of this material. And good electrical, and mechanical, and optical properties, generally. An obvious-- somewhat obvious thing, but very important, is we need to control the thickness uniformity across the wafer and from wafer to wafer so that when we go to etch it, or whatever, we know what the unit-- we know how-- what the uniformity is, what the thickness is, at any given point on the wafer.

There's something called step coverage, which I'll give you an example in the next couple of slides of what we mean by step coverage. We often want conformal deposition. And we'll give illustrations of that. We want to be able to fill spaces in between lines. We don't want to have voids, usually. And there is a need to planarize films. That is, create-- we have a topography that often has a lot of ups-- hills and valleys. We often need to planarize it to give a smooth, flat, top surface.

It turns out that certain deposition techniques themselves tend to be self planarizing. And we'll talk a little bit about that. So these are some requirements that people worry about when they're talking about coming up with a deposition procedure, or process. Let's give some examples of these issues, some of the ones that may be not so obvious here on slide number four. What is step coverage?

OK, well, step coverage is when we have a step that exists. So let's say, I already have this step here. You see this-- there's maybe a material here, this metal line, and then we have a step going over it. It could be an oxide. And now, I want to put a metal down. So I'm going to either evaporate it, or I'm going to sputter it, or somehow put the metal down. But you can see, here, I'm getting very uniform step coverage. Regardless of when I go over the step, I get the same thickness and conformality of the film.

That's good. That's uniform step coverage. This is what's called poor step coverage. What does that mean? Well, right at the point of the step, you can see that the film thickness is, with respect to the surface here, is actually less. It's thinned down here. So that's poor step coverage. It's not conformal. And so the problem with this, then, is if your step coverage degrades at some point, this can be a weak spot in the metal line. And you could get an open.

So step coverage is an important property of the type of deposition. So this would be considered poor step coverage. How about a filling issue? OK, well, what we mean by this is this is an example of metal that has been-- that shows good filling into a via. So here, I have a flat surface, I have a deposited oxide, and I've etched a hole. And I want to deposit the metal onto the surface and fill the hole. So that's good filling of the via.

Here's an example where we were trying-- we had metal to start with, these two metal lines. They had a certain height, and width, and spacing. And we were trying to deposit oxide over them. And you notice, we did not fill the space completely in between the two metal lines. We end up with a void. So that would be kind of a poor fill. We have voids. So we not only have to fill vias, which where we've etched, this is a via, where I've etched into a film, but we may have etched features that we're trying to cover up. And we want to fill the space in between them uniformly.

And then here's an example of-- here, the third example on the right is showing, trying to etch, or rather fill a via where we have poor bottom filling. Here, we get a nice metal film on top. The metal is not very well uniformly deposited on the edges. And the bottom doesn't fill very well at all. So there's an example of poor bottom filling.

So this particular methodology, we'll talk about how this happened. This probably happened in some kind of evaporation or some type of line of sight type of deposition. So depending on how we do the deposition, we can get different quality of filling. Those were cartoons. Here on slide number five, these are some actual micrographs. These are scanning electron micrographs taking in an SEM microscope. I took these directly out of your text.

The one on the left labeled A here is an example of poor metal step coverage. This is a sandwich layer, where Thai tungsten was put down, aluminum, then aluminum, and then Thai tungsten. So it's a tri-layer stack deposited by sputter deposition over an oxide step. So this is the oxide step here right at this point. And you can see the tri-layer stack here, it's kind of hard to identify the different layers, but it has this sort of-- this sort of thickness over here, and a certain thickness over here. But it did not cover the step. And the PowerPoint, unfortunately, this didn't scan all that well.

But you can see that the layer, the metal layer, is thinned down where it goes over the step. On the right-hand side, these are a series of metal lines. Each one of these is a metal line going into the board. And oxide was deposited over these metal lines by chemical vapor deposition. And there were very narrow spaces between the lines. The spacing is less than a micron, maybe half micron. And you can see in the deposition of the oxide, when it gets-- the spacing gets to be quite narrow, as in the case between these two metal lines. You actually get voids.

So the oxide did not fill in here. When the spacing was wider, as in this case, you didn't get the voiding. So when the net-- we get below a certain spacing. And this is a typical test structure one could use to figure out, what's my critical spacing, below which I start to get voids. And so again, this is a property-- this voiding will be a strong function of the method by which the oxide is deposited.

OK, so those are some practical examples of issues with film deposition. Let's go on to slide number six. There is an important concept when people are doing thin film, describing thin films, deposition. And that is called aspect ratio. We abbreviate that in this class, AR. And the aspect ratio is just simply defined as the height of a feature. So if we have a metal line, it says, height h divided by the width of the feature, w. So a meta line, it looks like this is the aspect ratio, h over w.

For a contact hole, they also speak of an aspect ratio. It's the height, or the depth, of the hole divided by its width. Aspect ratio tells you something about the topography. In general, a high aspect ratio structure is more difficult to fabricate than a low aspect ratio one. For example, it's hard to make a very, very deep-- imagine this being very deep and narrow contact hole. It has a high aspect ratio, say 2 to 1. And it's harder to etch it for one thing, and it's going to be harder to fill it, as you can imagine.

As you go deeper and deeper down, it's going to be harder to access the bottom of the hole. So in one of the requirements people talk about is, what kind of aspect ratio can a given deposition technique fill? And how does it vary with aspect ratio? So that's just a simple definition, h over w.

Slide number seven, I took from the-- your hand-- from the 2003 ITRS, the International Technology Roadmap on Semiconductors. Remember, in the beginning of this course, you read as a homework set, you read a couple of chapters. Well, I took this from the chapter. They have a whole chapter on interconnect. So this is table 81. And these are interconnect-- predicted interconnect technology requirements in the near term, so to speak. Near term being going up to the year 2009 for microprocessor units.

If you're talking about DRAM or other types of devices, the requirements are a little bit different. But this is specifically for microprocessors. And we've seen these type of charts before. Let's just go through it here. The columns are the years. So 2004, where we are right now. Remember, this was written a little over a year ago or so. So this is a prediction going up to 2009. And each row tells us some kind of a characteristic. In this case, for interconnect, I have pointed out with the arrows a couple of key characteristics.

Let's look at the number of metal levels. In 2004, that was expected on average for a microprocessor is 10 levels of circuit wiring of metal. So that's quite a bit. And you notice that number is increasing over time as we go through 2007 going-- five and seven is 11 metal layers and then going up to 12. And it's going to continue on beyond that. So we're getting higher and higher numbers of metal levels. That's one, which means we're going to have more deposition steps basically.

Another characteristic that is quoted here is metal one. The metal layers are numbered, by the way, from 1 up to n. So in 2004, if you had 10 layers, they'd be numbered 1 to 10. So the metal one is the first metal layer.

And you're being told here what the aspect ratio is. They use an A slash R in the ITRS roadmap. We just define the aspect ratio as being the height to the width for the metal line for copper. And its aspect ratio is somewhere around 1.7. And you see the aspect ratio is increasing over time.

And in fact, I didn't show it here, but if you go to the year 2010 and beyond, it goes up to 2, a little over 2. So the aspect ratio, we need to make that an increasing number. And then look at the number-- look at the interlevel metal insulator dielectric constant, the very bottom row of this chart.

I actually truncated the chart. There was a whole bunch of rows in the middle. And you can see right here where this little discontinuity, I took it out. If you want to see the full chart, you can go to the website. So look at the dielectric constant. The bulk dielectric constant of the-- of the insulator is going to between each layer of metals is actually going down. Here it is supposedly in 2003. It was around three. And you notice, we get into the yellow region, which means solutions-- people have some idea of what the solutions are, but they're not ready for manufacturing.

People want to go to less than 2.7 dielectric constant. And in the year 2007, they're looking at-- would like dielectric constants less than 2.4. And that's part of the red region, which means nobody knows exactly how to do that. So just the opposite of the gate insulator. Remember, in the gate insulator, i was trying to get higher capacitance between the gate and the substrate. So I can get better charge control.

So in the gate insulator that dielectric constant, we want to go up. For in the interconnect, we want the dielectric constant to go down. We want it to be lower. And these are the so-called low k dielectrics that are used in the back end. And the reason we want that is just simply if I have a big stack here, if I'm going back a couple of viewgraphs here to, say, page number two, I'm only showing a couple layers. But between this metal layer and this metal layer, I'd like to have minimum capacitance between the different lines because the capacitance leads to RC time delay in the circuit.

And so-- and in fact, the RC delays, the interconnect delays are very rapidly approaching the delays associated with the devices. So making the devices faster doesn't do a whole lot of good if your interconnect limited. So there's a trend to get new dielectrics in here, all these shading here in blue to come up with new materials that have lower and lower dielectric constants. Just the opposite of what we want to do with the gate insulator here. We want to make a higher and higher one.

So we're going to find new materials coming all the time. So let me skip back to that on slide seven. And again, if you want to see more of this, you just go to the ITRS. And you've been there before. And you just pick the chapter on interconnect. So besides interconnect though, I don't want to give you the idea that thin films are only used in the back end. They're actually used in front end. And that's what I'm going to emphasize in this course. So I chopped off-- I took the diagram I just showed you and I chopped off the back end to mean what we're talking about sort of front end.

And there are maybe three different types of critical thin films that we're going to emphasize, because this is a course on front-end processing. So we're going to emphasize the deposition of silicon, either single crystal by epitaxy, or polycrystalline by LPCVD. That's-- and here's the poly gate. Silicon dioxide, which is also called LPCVD oxide, Low-Pressure Chemical Vapor Deposition, or low-temperature oxide, and silicon nitride, which I've shown here in green. The spacers are often made of nitride these days, or combinations of nitride and LTL.

So that's what we'll emphasize in this class. All the rest above this, which I've erased, if you take 6.773, that hasn't been offered recently because Professor Reif is department head of EECS. So he's been kind of busy. But that course deals with all the types of thin films that are kind of above here. I'll talk a little bit about deposition of metals and things like that. But we won't emphasize it as much as that class does.

OK, so let's go on to slide number nine. And we'll just talk a little bit, historically, about how some of these films are deposited. And the films we're going to emphasize initially today will be a deposition of silicon, either polycrystalline or epitaxially. So there's really two main types of methods that are used in CMOS. And you'll hear about them. And one thing I want to apologize for right off the bat is in thin films, one of the things I really dislike is the number of acronyms is really kind of ridiculous.

And you'll see that as we go through, just this first bullet here, number one. So the first type of deposition method, and very common, is called chemical vapor deposition. And it is just like the name sounds. You have a vapor of different gases, and you deposit from the vapor phase a film on the wafer. And there are different types. People call atmospheric pressure, CVD, and that's abbreviated APCVD. Low-pressure CVD, which we'll talk about, abbreviated LPCVD.

Now, we get a little crazy. There's also a plasma-enhanced types of CVD. So PECVD, where we use not only thermal energy, but we use plasma energy to break up the constituents and cause the deposition. And there's also high-density plasma CVD, or HDPCVD. So it goes on and on, the number of acronyms that are all associated with CVD.

PVD, not-- maybe not so many in acronyms, but this stands for-- so the second major method is called physical vapor deposition. This is just as distinguished from chemical. It's primarily a physical process. So there's not as much chemistry involved. And the physical processes that people use, you may be familiar with, is thermal evaporation, which we'll talk about, and sputtering. These are primarily physical, have less chemical sort of-- less chemistry associated with them.

So let's talk about CVD here first. This is a very old-fashioned sort of classic diagram of an example of an atmospheric cold wall, or cool wall system, that might have been used for a number of years to grow epitaxial silicon. And I put it here in quotations, "old fashioned" because it's pretty far from what modern epitaxial reactors look like today. And I have some examples of modern reactors in the next few slides. But just to give you an idea.

The basic idea was this. You had a series of different gas lines. So here is, for example, hydrogen with diborane or phosphine. These could be used for dopants for boron and phosphorus doping. You had carrier gases like argon and hydrogen. Hydrogen chloride could be used to etch a-- etch deposits off the courts. And here's a liquid source for silicon, silicon tetrachloride, $SiCl_4$. Maybe hydrogen was bubbled through that and transported that vapor into the chamber.

The silicon wafers typically used to sit on a big block of graphite. And the graphite was heated not by a nichrome heater, but it was heated by induction heating. So there were RF coils. And this is why it's called cold wall, because these RF coils, the RF energy is not absorbed by the quartz, just by the graphite. So just the graphite gets hot here. And the hot graphite then heats the wafers. The chemical vapor passes over. And there's decomposition on the surfaces we'll talk about. And you grow the epitaxial silicon. That's a-- that's a relatively old-fashioned atmospheric reactor.

Let's go on to slide number 10. Now, this is an example of something that you will find. That old epi reactor, you probably won't find in too many fabs today. Maybe a few of the bipolar-- old bipolar fabs. But this is a reactor that you will find in most fabs, something very much like it. It's called low-pressure hot wall system, or LPCVD. And it's used pretty much every day now for the deposition of polycrystalline silicon that is used to form the gate, or for amorphous silicon. And-- or even the silicon dioxide. This type of setup.

And what it is is a regular furnace that is resistively heated. So it's a hot wall system. So the entire quartz tube comes up to the temperature of deposition. Could be 600-- anywhere from 400 to 700, something in that range. So everything is hot. And you notice what's very different from the previous diagram. I have some kind of a quartz holder here. And the wafers are standing up. They're not sitting flat. And there's a lot of wafers in here. It could be 25. Could be a hundred.

But they're stacked very, very close to each other. And so you can do batch processing. Lots of wafers at once. And the whole reason you can do this, and we'll talk about that, is because it turns out the mean-free path is quite long when the pressure is low. So the gas can get-- effectively, the reactants can be transported in between the wafers very efficiently. So there's no need to spread them out over a large susceptor, as we had to do in the case of an atmospheric process like this, where we can only get two or three wafers in at a time.

In this low-pressure case, you can put in quite a few wafers. The pressure is kept low in this case by a vacuum pump. So the quartz tube has an opening in the front, which is sealed by an O ring seal and a stainless steel plate. So that closes the quartz, and you can suck on it with this pump, and pull a vacuum. And you have a couple of source gases that-- with mass flow controllers that control the flow of whatever it is you're using. Could be silane, could be dichloro, or whatever. Yeah.

AUDIENCE: Why is it that when the mean-free path is long,

do you get the atoms to go [INAUDIBLE]?

JUDY HOYT: We're going to talk about that. But basically, if the mean-free path is sufficiently long, what it means is before-- the atom can go, or the molecule can go, a long distance before it hits a wafer and would stick. The mean-free path is very short. And I would have put it in a reactor like this, you'd get deposition all on the tips of the wafers right on these edges. But it wouldn't get down in between because the mean-free path tells you how often is it that you have a collision.

If that mean-free path is very short, basically, you're going to-- the chance of you having a collision with a wafer is quite high and you'll tend to react.

AUDIENCE: Is it a collision of particles?

JUDY HOYT: It's a collision of particles. Right. But it also relates to the interaction of those particles with whatever you have in the reactor with the geometry.

AUDIENCE: It means [INAUDIBLE] to have more shielding [INAUDIBLE]?

JUDY HOYT: Well, it's not-- this is a chemical process now. Again, when we talk-- when we kind of go through this process, it may become a little obvious. It's not evaporation. You still have the gas flowing and getting in between. So it's still a gas phase type of process. We're not evaporating onto it.

So the gas can still flow here in between each of these wafers. And the pressure is low enough that the reactants can get in between. And you can get nice uniform deposition. That's not the case if you do at atmospheric pressure where you need to have the wafers well separated, because you develop boundary-layer effects and things like that.

OK, hopefully, that'll become a little more obvious as we go on for the rest of this lecture and the next. OK, what else about this reactor you should know? Remember, it's a hot wall. That's-- the problem with that is you get deposition of whatever you're depositing on the wafers also deposits on the walls. That can be a part-- give you particulate problems. Because you can eventually develop so much silicon, develop deposit on the walls, it's-- it'll start to flake. And then you get particles.

So LPCVD is notorious for having particulate issues. So that's kind of a basic characteristics of LPCVD reactor. Let's give an example of two types of deposition. Here's on slide number 11. The first example was epitaxial silicon, single-crystal growth. And I showed you a picture of a cold wall atmospheric pressure system. This particular equation, equation number one, is, again, a little bit old fashioned using silicon tet, silicon tetrachloride. And it reacts at high temperature, and can be decomposed into silicon solid plus HCl gas, which has evolved.

You can also more commonly today, rather than silicon tet, people typically use silane, SiH_4. Again, in the gas phase at high temperature, it can react to form solid silicon and give and evolve off hydrogen. So this might be for epitaxial growth. The second example here, equation number three shows the deposition of amorphous silicon dioxide. So this is that famous LTO that we've been talking about, low-temperature oxide. That is deposited very commonly in a hot-walled low-pressure system, just like what I just showed on page 10.

This is exactly a low-pressure CVD oxide, or LTO furnace. And the way the LTO is made is typically with silane, a gaseous silane combined with oxygen, usually in the temperature range of 400 to 500, something like that. Decomposes on the wafer surface. Both of these decompose. And they react to form SiO_2 in the solid phase, and evolved hydrogen. And notice, because you are putting in silane, you don't have to consume any silicon on the wafer.

So that's the advantage. If you need to put down a film, and there's no silicon exposed, then you use this low-- this LPCVD process to get-- put down an oxide. OK, there's a couple of examples. So let's look at this process now on slide number 12 a little bit more carefully. And here, maybe we'll see how the pressure comes to play in all this.

Slide number 12 talks about atmospheric pressure, APCVD. And what it is is, schematically, this is the top wall of your reactor. Could be quartz. Here's the bottom wall. Here's a graphite susceptor, which is hot. And there's a wafer sitting on it. And there's a gas stream up here above. Some distance is the gas is flowing at a reasonably high velocity. And steps one through seven here are the different steps that people have identified as being involved in chemical vapor deposition.

So notice how it's not evaporation. So the first step, we take the reactants that are-- that have to be transported from the main gas stream into the deposition region. So they're coming in the reactor over here on the left. They have to get over near the wafer. OK, that's obvious. It's not usually rate limiting in any way.

Step number two is the transport from the main gas stream through what's called a boundary layer to the wafer surface. Now, a boundary layer exists whenever you have a static surface and a gas or some fluid flowing above it. And the boundary layer is a layer in which the velocity of the particles actually goes from the velocities in the center of the tube down to 0. Because right at the wafer's surface, the velocity is 0. So you have to somehow get through the stagnant layer.

And so transport through the boundary layer is one of the critical processes. And it will be rate limiting in certain types of reactors. Then there are three surface processes here. You could lump them all together if you want and just call them surface processes. But they are called out individually here. Number three is the adsorption of the reactant onto the wafer surface. Four is the surface reaction itself, including a chemical decomposition, like what I just showed you, a reaction, if we go back to slide 11.

This is what I mean by that step. So it's the actual decomposition of the gas on the surface into to-- to crack the gas, or decompose it. Could also be a surface migration involved in the surface in step four, or attachment to kinks and ledges. So there are a number of surface processes that happen. And then step number five is desorption of the byproducts. And then we have to transport the byproducts through the boundary layer.

And then finally, transport of that out of the reactor, out of the deposition zone. And I've highlighted here in red steps two through five because they're most important in determining the growth rate. In fact, the two rate-limiting steps tend to be step two, which is transport the reactants through the boundary layer, through the-- which is usually typically a diffusion type of process, and a reaction-- the second rate-limiting step is the surface processes themselves, the chemical reactions usually.

OK, so let's go on to slide 13 and talk about a way to quantitatively come up with a very simple quantitative model. Now, I've turned everything by 90 degrees on you because that's what was done in the text. I took this from your text. So now, be a little more careful here. The silicon wafer is now sitting vertically. It doesn't really matter if it's horizontal or vertical. You just have to tilt your head, if you want, from the last picture.

And the gas here, so the gas is flowing vertically. So the gas is going up here the way the laser pointer is. It's flowing by. And it has some concentration here in the main gas stream. And this region that's labeled from here to here by these two arrows from the silicon surface to this point here is called the boundary layer.

So that's the stagnant layer where the gas velocity in the stream direction is actually going down. Eventually, it reaches 0. So within the boundary layer, we typically have a gradient of the concentration of the silane, or whatever it is, the concentration of the reactant. And the gas stream is called c sub g here. When you reach the surface of the silicon, at the very surface, there's a concentration of that species called c sub s at the surface.

And these two-- these two f's here, this flux f1 is a diffusion flux. So that's the flux of the reactant species to the wafer. And it's mass transfer-- it's called a mass transport, or mass transfer flux. And on the previous page, it represented step number two. So that's this flux, f1. Flux f2 is the actual reactant consumed by the surface reaction. So that's the surface reaction rate, or surface reaction flux. And that's what I meant by steps three to five on the previous page. So f2, refer to these surface reactions.

So we have these two fluxes. We got to get through the boundary layer by diffusion, and we've got to react to the surface by some chemical reaction. And so where-- we're just going to write down simple equations for flux one, transport through a boundary layer. We're going to say that flux, the number of particles going through per square centimeter per unit time is going to be just proportional to the concentration gradient, cg minus cs. And the proportionality constant, we're going to call hg, which is the mass transfer coefficient, and typically have units of length per unit time, or centimeters per second.

So that's the first flux. That's just transport through the boundary layer. Flux number two is the reaction at the surface, and is a chemical reaction. So we typically write that with its chemical constant, k sub s, some surface reaction rate in centimeters per second, times the concentration of the species at the surface. So again, this is a little cartoon of what we just saw.

So in steady state, we're going to let this-- the fluxes through the boundary layer and at the surface, be equal. f1 equals f2 so we just equate equations four and five, which we just had. That's pretty simple. We can solve, then, for c sub s, the concentration at the surface, in terms of c sub g, the concentration in the gas. And we get its cg divided by 1 plus k sub s over hg.

Now, we just need to define the growth rate of the film. So the growth rate of the film is this flux, f, which we now know. We can write f as k sub s times c sub s. And I just solve for c sub s in equation seven. So the velocity of the growth rate of the film is a velocity v. It's just the flux divided by n, where n is the number of atoms per cubic centimeter. Just you can just do this dimensionally.

The velocity-- the flux has units of number of atoms per square centimeter per time. And this is number of atoms per cubic centimeter. So I just-- I end up with a velocity of centimeters per second, or centimeters per unit time. So we just divide this flux by the density. In silicon, for example, the density is 510 to the 22nd. Multiplying this out, what we get is we get this quantity, k sub s hg divided by k sub s plus hg. That times the concentration in the gas phase of the reactants divided by the density.

This kind of makes sense if you look at it. Or you can look at it here in terms of this quantity y, where y is the mole fraction of the incorporating species. So it's the partial pressure of silane, for example, divided by the total pressure in the-- of the gas. And it kind of makes sense, as you might imagine, the velocity of growth, or the growth rate, depends on the concentration of the species in the gas phase. That's not too surprising.

And therefore, it depends on the mole fraction, the partial pressure of the silane divided by the total pressure. So that's a very simple model. And the important thing is now to look at the dependency on k sub s and hg and what their temperature dependences are. So let's go on to slide 15 and look at that. So this is the-- equation eight, I just repeated exactly that same equation we just saw for the deposition rate. And you notice what it-- because of the way these add here, the deposition rate is going to-- determined by the smaller of the two of k sub s or hg.

So let's say k sub s is very small. Then I can ignore it here and forget about it in the denominator. Then the hg's go out. And then in that case, if k sub s is very small, the velocity just depends on-- but I'm doing this case. Then it just depends on hg times this concentration. Let's see. k sub s is much, much less than hg. Then I can ignore it here. The hg's go out. Oh, and I end up-- it's the rate-limiting step. And you end up being proportional to k sub s.

So in that case, we have what's called the surface reaction case. So this would be a case where the mass transfer through the boundary layer is very fast. You want to think about that, or you could call it in a case where the surface reaction is very, very slow. And so the growth rate in this case is directly proportional to the reaction rate. The important thing about k sub s is to notice is that it's exponentially dependent on temperature.

So in this regime, we expect to see the growth rate exponentially proportional, or exponentially dependent, on temperature. On the other hand, if k sub s is very-- if the reaction goes very fast compared to the mass transport, or the mass transport here is slow, hg is small, then we have the mass transfer, or gas phase, diffusion control case. So here, the velocity depends on hg, which it turns out, diffusion through the gas is not a very tempered-- unlike reaction at the surface, is not very temperature sensitive.

So we expect in this regime to have a very weak temperature dependence. So just, we can immediately see these two different regimes happening depending on the relative ratio of k sub s to hg, and therefore, depending on the relative temperature.

So if we go to slide 16, what people find experimentally what these rate constants look like. k sub s actually goes like a constant, some number, k naught, whatever it happens to be, times e to the minus e over kt. So the surface reaction rate has a certain temperature dependence, it's exponential, and it has an activation energy of ea.

So if I were to plot that on the growth velocity, or the growth rate, on a log scale, versus 1 over t, what-- the k sub s term is just going to be a straight line because it's just, I'm taking the log of an exponential. And therefore, I just get a straight line directly proportional to 1 over t. So down in this region here, the slope is directly proportional to the activation energy.

Now, what happens is, as I go-- as I change the temperature here, and I go to higher and higher temperature-- so higher temperature means going to the left, right? Going to lower 1 over t. At some point, what we see is we come rate limited by the surface reaction rate by the mass transport rather. The surface reaction is happening so fast at this point that its rate overtakes that. And you-- the growth rate becomes limited by transport through the boundary layer.

And that transport through the boundary layer is pretty much a constant. It doesn't depend much on temperature. It depends on pressure and the design of the reactor. So in this regime, we expect this to be relatively temperature insensitive. And of course, the growth rate is-- the net growth rate is neither one of these dashed lines. It's the solid line, which is the combination of the two, where we combine them just like we did here according to this equation, equation eight. Tells you exactly how to add them up.

For example, if you are growing single crystal silicon, typically, the activation energy, just to give you a rough idea, is typically in the range of 1.6 to 2 EV. So that's what the slope down here will be. And again, hg is relatively constant as a function of temperature. So as an example, let's go to slide number 17, where-- which illustrates some data I took out of your textbook on silicon epitaxial growth.

And this is all at atmospheric pressure. So the data is a little bit older. But what you see here is growth rate. And the units are microns per minute. And again, this is a logarithmic scale versus 1 over t, or actually 1,000 over t. So this is a typical Arrhenius-type plot. If you want to read the temperature, you can conveniently read the temperature right off here, going from say 600 all the way up to 1,200.

And there are a couple different curves here. So here's the curve for silicon tetrachloride. Silicon tet doesn't react very well at low temperatures. So its growth rate is relatively slow compared to trichlorosilane, dichlorosilane, which is SiH2Cl2-- that's dichlorosilane, very commonly used today-- or silane. Silane's the most reactive of all of these. And so at any given temperature, it has a higher growth rate. You can see that.

But look at the shapes of the curves. It's very similar to that previous model. Not exact. But you see for any given reactant, let's say silane, we have a region where the growth rate on Arrhenius plot is a straight line. So it's exponentially activated. This is so its mass-- it's limited here by a surface reaction. Very sensitive to the temperature. And then you finally get up to a high enough temperature and it starts to roll off. It never is completely constant. But it reaches a point where the temperature dependence is very small at high temperatures.

And so and this-- we call this high temperature regime the mass transport limited. So you're talking about diffusion through the boundary layer. And down here, where it's clearly exponential, the surface reaction rate limited. So in the old fashioned silicone epi, people used to do deposition at very high temperatures to get high crystal quality. So in the old days, people typically grew at 1,00 or 1,150. So they were almost always growing with these reactants in the mass transport limited regime. So they were almost always hg controlled.

So the old-fashioned reactors had to have the horizontal reactor configuration because mass transport through the boundary layer depends on exactly how the reactor is designed. Modern epitaxy often operates, however, people growing silicon germanium and other materials need to be grown at lower temperatures, like 800 or so, or 700, often operates in this regime now these days, where you're in the exponential regime. So we're controlling the temperature becomes extremely important because that-- in order to get good growth rate control. Yeah.

AUDIENCE: [INAUDIBLE]

JUDY HOYT: The question on slide 17 is about, what happened to the silane in the nitrogen ambient? You see this dashed line. You notice the growth rate for silicon using a nitrogen ambient instead of a hydrogen. These are all grown in hydrogen, which is typically used for higher purity. The growth rate pops way up at the same temperature. And the reason for that is if you go back and look at a couple of slides, let's see if I can find the chemical decomposition.

On slide number 11, if you look at equation number two for the chemical decomposition of silane, silane and the gas forming silicon, solid silicon, it evolves. The reaction, when you grow epitaxial silicon with silane, it evolves hydrogen. So hydrogen has to come off. Now, this is a chemical reaction. So you know you can push it to the left. You can tend to slow down this reaction if I put a lot of hydrogen in the ambient.

So using the hydrogen carrier gas tends to push this to the left, and tends to cause this surface reaction to be less probable. And the reaction rate goes down. But if you, instead of using hydrogen as the carrier gas, if you use an inert, more inert gas like nitrogen, you won't have that pushing-to-the-left effect. And so the growth rate goes up.

AUDIENCE: [INAUDIBLE]

JUDY HOYT: Well, let's see. In the transport limited regime, you're still going to have-- I mean, you still have-- well, there is a little bit. Yeah. Well, in the transport limited regime, it looks like we never really get there with this dashed data. They sort of petered out a little bit. So it's almost getting to the transport limit regime. But the problem is the surface reaction rate is so fast now, it's hard to see the transport limited regime. But it looks like they're converging. It looks like the two are converging.

Because at that point, the reaction rate really isn't what's controlling it. It's the transport through the boundary layer. So the question is, well, what's the difference in transport between a boundary layer and a nitrogen versus a hydrogen? There's probably some small differences there. OK, so let's go on to slide number 18.

We were just saying how transport through the boundary layer is important when you're in the high temperature regime, or the mass transport limited regime. And therefore, it turns out that the reactor geometry in the high temperature regime is very important, how you build the reactor. And I've taken this on slide 18 here. I've taken this picture from your textbook, figure 9.9. And what it's showing is the velocities in the boundary layer, the velocities are represented by these little arrows along the susceptor and going from left to right.

So the gas is coming in at the left, flowing over the wafers and the susceptor, and going out the right. And according to some gas flow laws, Newton's second law, the boundary layer, the thickness of the stagnant layer, which is represented by the height of this layer above the wafer surface, this delta sub s, you see this height, or the thickness of the stagnant layer, is actually increasing. So and this boundary, this dark region, represents the thickness of the boundary layer.

And you notice beyond the boundary layer, above it, the gas velocity has reached the same as the velocity as it is in the center of the tube. It's only within the boundary layer that the velocity is decreasing. So these arrows, their lengths are decreasing. So as you flow gas through a pipe against the surface, the boundary layer thickness is actually increasing.

Now, this process of diffusion through the boundary layer, this quantity, the hg, the mass transport coefficient, it has to do with diffusion through that delta sub s, that thickness delta sub s. So people write in a crude way that hg is equal to some diffusion coefficient in the gas phase divided by the thickness delta s.

But see, delta is not constant as the gas flows along the surface. So people try to manipulate things to try to make delta s more constant across the reactor surface. Otherwise, what will happen is the growth rate here will be much higher on the first wafer than it would be on the last wafer in the reactor.

So people try to compensate for that. A certain type of reactor geometry is usually required, therefore, to get uniform deposition across a number of different silicon wafers if you're working in this mass transport limited regime. A typical trick is to tilt the susceptor. So take the susceptor and tilt it. And how-- this increases the gas velocity, which keeps delta sub s constant.

So as I'm going, the gas velocity at this point-- so imagine I'm flowing the same volume of gas a certain number of liters per minute through this cross section from here to here. The gas velocity has some value. Now, if I go here, the cross section has decreased. So the velocity-- so again, I'm getting the same volume number of liters per minute. So the velocity of the gas in a smaller cross section tube must therefore go up. So v is increasing. now from left to right, which was not the case when the susceptor is flat.

When the susceptor is flat, the velocity here is called u. And the center is the same from left to right. And so what we're doing is we're-- to compensate for this-- to make the boundary layer thickness perfectly flat, we tilt the susceptor to up that velocity in the center of the tube. So but there's another-- there's another issue, though, with non-uniformity. Not just so that-- and you can take care of the boundary layer effect by designing your reactor appropriately.

The source gases themselves can become depleted along the length of the susceptor. So you have-- maybe have less silane back here than you have here because a lot of it may have reacted. What people sometimes do, then, is they sometimes introduce a temperature gradient along the flow direction. So you might make the temperature here just a little bit hotter than it is here and try to compensate for that, and try to get uniform thickness on the first wafer, and the fifth wafer in such a type of reactor.

So if we go on to slide 20, now, there are some implications of this-- what we know about how CVD works now based on our simple model of surface reaction rate and mass transport late on the reactor design. If we look at a horizontal reactor, and this is what I was just-- this is supposed to represent the tilt susceptor.

If the deposition occurs in the range of, say, one torr to 760 torr, relatively high pressures and relatively high temperatures, then the mass transport to the wafer surface is the most important thing. It's more important than the surface reaction rate. And that places some severe restrictions on the geometry of the reactor, and on the gas flows, and how the wafers are stacked.

So typically in that case, atmospheric pressure, or relatively high pressure, epi, you'll see it in reactors that only have a few wafers in them. And the geometry of the reactor and how you stack them is really critical. So when the deposition occurs primarily at low temperatures, and low pressures-- so we're in the millitorr regime, or hundreds of millitorr, we're surface reaction rate controlled. So it's very sensitive to the temperature. But it's not so sensitive to transport through the gas boundary layer.

And the mean-free path is long enough that the mean-free path is just don't come into effect. In this case, for this type of process, then, where we're working in the hundreds millitorr range, and the temperature is low enough that we're surface reaction rate limited, we can stack the wafers together relatively closely. So you see in an LPCVD process, which LPCVD usually works at around a few hundred millitorr, you can stack a lot of wafers close to each other.

You still have to worry about gas depletion in LPCVD. So what people do is when-- assuming the gases are coming in here and going out, say, they're going out-- going from left to right, people will again tilt the profile of the temperature in the furnace. So typical LPCVD system will have three zones, a front zone, a middle zone, and a back zone. And the back zone is usually kept a little bit hotter than the middle or the front zone. Because again, the silane, or whatever you're depositing, tends to get depleted.

So you make up for that by increasing the surface reaction rate a little bit by increasing the temperature. So you hope you can get the same thickness on the first wafer as you got on the 50th wafer, or whatever. And that needs to be done somewhat empirically. So on slide 21, I'm showing some classical geometries for epitaxial reactors. I took this from Simon Z's book. He has a VLSI technology book that he edited. There's a whole chapter there on epitaxy if you want to hear more-- see more details on it.

These are some schematics of some of the common old-fashioned epi reactors. There was something called a radiant barrel. The barrel reactor was shaped like a barrel. The gaseous-- gas would come in at the top and exit out the bottom. And there would be sort of cylindrically shaped, but with flat surfaces, sort of susceptor. And you see each one of these circles is supposed to represent a wafer sitting on the susceptor. So you could get a fair number of wafers in it at one time.

And notice, the-- they were trying to make to do the equivalent of susceptor tilting by decreasing the cross-section through which the gas flows from the top, which the wafer at the top to the bottom, where the gas exits. There are also vertical reactor geometries where the gas would come in and go out like this. And the horizontal, we've already talked about.

So all of these were in the cases where-- are typically multi-wafer tools where you grow anywhere from five to 20 wafers in a typical epi-- in an epi batch. It's the more classical, or maybe old-fashioned, type of reactor. Slide 22 is a more modern epitaxial system that you will see in fabs today, particularly fabs that are growing silicon germanium for bipolar transistors, or even silicon germanium now used in CMOS in source drain regions of CMOS intel has a commercial process.

In both of those cases, bipolar or CMOS, people have moved to-- away from the old fashioned more to the more modern single-wafer epitaxial, silicon, in order to get the kind of uniformity they would need over a single wafer. As the wafer diameter has increased, people are now at 12-inch wafers. The reactor would become gigantic if you had 12-- 12-inch wafers along a system. It's much more efficient to do a single wafer in a chamber at a time, and get the throughput high enough that you can do that.

So this is an example of a system that's manufactured by Applied Materials. We actually have one here at MIT. This is sort of an overall view of the system. What it has is two different load locks. So the load locks are designed so you can open them up to air without putting air into the reactor-- into the reactor itself. So you can keep the reactor very clean. So you can open this door, put the wafer cassette in, and close it, and pump it down, get most of the air out. So you don't just open up the whole reactor, and get all the air in, and contaminate it.

Because there's a couple of different load locks. There's a transfer-- a chamber in the center called the transfer chamber, which has a robot in it. And here's a picture of the robot. It has two little arms. Looks like a frog arm. The robot will come out, grab a wafer from the cassette, put it into the transfer chamber, and close this door, again, so you don't allow any air to get in. And then it'll take the wafer, according to how it's programmed, and put it in one of these three chambers depending on what is-- how you've programmed it.

And there-- you can have up to three chambers here growing different materials, silicon or silicon germanium. So they increase the throughput by having three chambers instead of having three wafers all along the susceptor in a single chamber. Typical growth pressure in this type of equipment is in the 1 to 100 torr range. So both-- it turns out both surface reactions and mass transport are important. Growth temperatures can be anywhere from 400, very low if you're growing some special material. Typically, silicon germanium is grown between 600 and 800.

And high-temperature silicon can be grown up to 1,100 in this type of system. Just taking a little more zoomed-in look at this more modern reactor on the slide 23, this is that same picture. The only difference is here, we're showing in a single chamber right here, one of the chambers. And this green object is meant to be a wafer that is sitting on a susceptor that's spinning.

So the wafer is spun at high velocity, say 30 revolutions per minute, to try to get good uniformity across the wafer. And the gas comes in here through a series of injectors as a plane flows across the entire wafer. So the inject is over here. And it flows laterally across, and the exit, or the exhaust, would be over here. And the wafer is spinning.

So the chamber is designed with both in mind. Both the control of the boundary layer is important as well as the control of the temperature. There's a lamp bank that sits on top and bottom that tries to uniformly control the temperature from center to edge to get good uniformity of the epi. So that's a more modern single wafer piece of equipment.

So let's just go back one more time to think about slide 24, the basic example of silicon epi. To show the slide before of temperature effects, depending on the relative speed of the surface reaction rate, and the mass transport through the boundary layer, you'll be in one of these two regimes probably.

This curve on the lower right is interesting. It shows the reactant flow, or the partial pressure, effects. So this is-- before, I was showing growth rate versus 1 over t. So these are at fixed temperature. Each curve is for a fixed temperature. And I'm showing growth rate versus the percent of the reactant.

So this is the percent of dichlorosilane that's in the gas stream. Or you could think of it as the dichlorosilane flow. So interesting, if you go here at lower-- with dichlor-- in this particular reactor, again, this will be reactor dependent. At 840 degrees, the growth rate is independent of the flow of the dichlorosilane. So it doesn't matter. You can increase the partial pressure by a factor of 2 or 3. You're not upping the growth rate anymore. You have enough there. And you're really limited by the set of the partial pressure limited by the temperature, the rate at which the reaction can occur.

So at low enough temperatures, it doesn't do you any good to flow more gas. As you get to higher temperatures here, say at a thousand, you can see that the growth rate is pretty much almost linearly proportionate up to a certain flow. It's proportional to the flow, or the-- because basically at this point, the surface reaction is going faster and faster as you give it more reactants than at some point, it saturates out.

So depending on what temperature you're in, increasing the flow may or may not increase your growth rate. So we go to slide 25, there's another process that we want to talk about. We've talked a little bit about design of the reactor for growth rate uniformity and things like that, and epitaxial growth. But the uniformity of the layer thickness is really only one aspect. And these days, it's pretty well nailed. But another aspect that's just as important is called autodoping during epitaxial growth.

And it's sort of unique to epitaxial growth. We don't usually think about it as being an issue in deposition of other types of films. But autodoping, as the name implies, is automatic, or unintentionally-- unintentional introduction of dopants into the epitaxial growing layer. And there's a couple of different regions it can come from.

First, before we look at the reactor at the top, let's just-- look at the-- this diagram at the bottom of slide 25. And it's a plot of the concentration on a log scale of a dopant as a function of your distance into the epi layer. So if you-- it's a little bit backwards, but going from 0 to here is your distance into the epi. So the epi is getting thicker from left to right. And everything to the left of 0 is the substrate. So here, I'm in the substrate. So what we're doing in autodoping, you can imagine, I might have a substrate that's heavily doped, say, for a silicon bipolar process.

So I have a substrate that has some concentration at the surface. And some of that dopant is going to make its way into the epi layer as the epi layer grows. And one process of-- say I'm trying to grow a lightly-doped epi layer on a heavily-doped substrate. One process by which it will get in there, you already know. And that's diffusion. And in fact, we know it's going to be a complementary error function type of profile if it's simply up diffusion from the substrate into the epi layer.

So that's relatively simple. We know how to solve that. And we can limit the temperature and all that. And that will help us limit how far this autodoping goes into the epi layer. But there's another process here, which I'm showing by this sort of exponential dependence, exponentially-decreasing function. It has a certain decay length. And that's called front side, or vertical, autodoping.

And vertical autodoping refers to the fact, not so much up diffusion, but just the fact that as I grow a single layer, if there is a phosphorus atom there on the surface, it tends to want to be up on the surface. So it tends to want to exchange sites instead of being buried with the silicon. And the phosphorus will ride up the surface. Same thing for arsenic. These dopants tend to like to be on a free surface.

So as you're growing the crystal, they will ride themselves not by diffusion, but just by surface exchange at the surface. They'll ride themselves up the epi layer. And it's called vertical autodoping because it happens directly from the buried layer. It just goes vertically straight up. So that surface riding effect is really a function of the nature of the dopant and the temperature to a certain extent.

But the nature of the dopant, it turns out the n-type dopants, arsenic, phosphorus in particular, like to be on the free surface. They're very happy being on a free surface. So they float to the surface. And they make it very hard to make a lightly-doped epi layer because they tend to autodope. They tend to have a long tail.

Boron on, the other hand, doesn't mind being buried in the crystal. So boron doesn't have much autodoping. It does not surface ride very much. So this tail is not a diffusion-limited process. It has to do with the affinity of the dopant for the free surface during the growth process. And then there's this final background that you'll see in an epi layer, which is I'm showing here in green, called-- sometimes called backside, or lateral, autodoping.

And what that refers to is you can get-- say if the back of the wafer is heavily doped, when you heat this thing up, you can actually get dopants coming off the back and finding their way onto the front of the wafer. They could be coming off the susceptor. Let's say you just grew a doped epi layer. The run before this, you're growing doped epi. And you put in some phosphorus. So that phosphorus now can still hang around in the susceptor. And then it can be transported when the susceptor is heated onto the wafer.

So it could be from the back of the wafer, it could be-- from the susceptor, it could be from another wafer that has a heavily-doped region on it. So it's lateral because it's coming from somewhere else. And this is very often a function of what you just grew, maybe a memory effect that was grown in the reactor, and how it's designed, how well the susceptor is sealed, and things like that.

So in the epitaxial growth process, we don't worry just about growth rate and its uniformity. We have to think carefully about temperature, and pressure, and the nature of the reactor design to avoid this type of autodoping effect. Slide 26. Let me-- let's say a little bit about epitaxy has evolved in CMOS and bipolar technology just so you have a view of where it comes from. Originally, in the old days, epi was originally primarily used just to provide a lightly-doped layer on top of a heavily-doped substrate for either bipolar or CMOS device processing.

So epitaxy in the old days, and there is no chalk, because-- we had colored chalk last time. So it was simply a way if you had a heavily-doped wafer, and you needed a lightly-doped layer on top, maybe 10 microns, it was a way to produce that. There really wasn't any other way. And CMOS and bipolar foundries, or companies, didn't do epi. They bought epi wafers from one or two places in the world, half a dozen places where people grew it.

So you would just buy an epi wafer. There's-- that's still a very large market, a very large component of epitaxial technology. It's simply to produce wafers that are heavily-doped substrate, and you need a lightly-doped layer on top. But actually, the last 10 or 15 years, the technique really has evolved. And now, it's used to do much more than that. People grow very complex doping profiles. They grow layers of different materials. Silicon germanium is grown on silicon, for example. It could be grown selectively.

That means in only certain regions of the wafer where there are openings in the oxide, could be-- selective epi can be used for the source drains on top of the source drains to elevate them. It could be used in the active regions of the heterojunction bipolar transistors. So epi has gone from being just a type of wafer you buy to the point where different-- where manufacturers of silicon chips now, a lot of them have epi reactors in their fabs. And they use them. Thanks. And they use those reactors to actively grow structures.

So as these-- as this evolution took place, several things had to happen. And that's why these new single wafer reactors have come out to a certain extent. This-- the cleanliness of the system and the purity of the gases had to be improved. And that's because the epitaxial growth temperatures are going down. And there's a tendency for impurities, like oxygen, to be incorporated much more readily at low temperatures. So in order to deal with that, as we lower the temperature of growth, we need to have a cleaner reactor. Otherwise, you're going to put a lot of oxygen in your epitaxial layer.

Again, and pre-clean temperatures have also lowered. So the reduction in the growth temperature and reduction in the pre-clean temperature means epi now has a lower thermal budget. It used to be 1,150 degrees for an hour. Now, people grow silicon germanium layers at 700 for 10 minutes. Something like that. So it can be a relatively low thermal budget process now. And that's important. Because that means you can have epitaxial-- you can have other dope structures on the wafer, and not have to worry too much about TED, or other things going on.

But in order to have low-temperature growth, you really have to have a clean reactor. So the new paradigms I've already showed you are single-wafer tools. There are rapid thermal epitaxy systems. So just like rapid thermal annealers, but you can grow epi in them. And there's also something that is not used in production very often, but is used in research. It's called molecular beam epitaxy.

It is not a manufacturing process generally because the throughput is horrible. But it's a good-- it's very good for research. It's good for growing new types of materials for the first time. And then people figure out how to grow them by CVD. And they go from there. So that evolution that I just explained in words is shown here pictorially on slide 27 in the 1970s, probably before you guys were born, maybe. Or you were just being born. I don't know. Something like that. No, no. That's before your-- yeah, yeah. That's a long time ago.

This is what epi was, the concentration versus depth in a bipolar transistor. The epi was simply formed-- the whole-- the collector. You just grew a silicon epi layer, you would buy a wafer with 5 microns of epi on it. And on top of that, you would form-- you would diffuse in or ion implant your base, and then you diffuse in your emitter. And you make an NPN bipolar transistor.

And the epi layer was pretty thick, 5 microns. In the 1980s, again, it was silicon, epi, and the epi layer was shrunk by a factor of 10. Bipolar transistors, the total thickness was about half micron. So in those 10 years, the epi layer thickness had to drop by a factor of 10. People had to learn how to do autodoping reduction. They had to change the pressure and the temperature to try to reduce this out diffusion and the autodoping of this n plus buried layer into the active region.

And finally, the 1990s, what people started to do, instead of just growing the collector, people started to grow not only the collector by epi, but the base. Instead of using an ion-implanted, look at this-- you can see this very broad profile with a retrograde. That-- not necessarily what the device designer wanted. That's just what they got when they ion implanted it.

In fact, you can grow a very thin, narrow profile with a very abrupt base doping by epitaxial growth. And so epi transformed from just growing the substrate to being able to grow the base layer. Either a silicon base or people then inserted silicon germanium into it. And IBM and others commercialized the silicon-- silicon germanium, silicon heterojunction bipolar transistor. And that was all based on the development of silicon and silicon germanium epitaxial-- epitaxial growth technology.

So it's really come from tens of microns. Now do people grow typical base today in a heterojunction bipolar transistor is 400 angstroms. So people are growing 400 angstroms in silicon germanium commercially in production, and thousands of transistors on circuits all the time, and selling them.

So what are the most common gases here on page 28 today for epi, silane is quite common. And we saw the decomposition reaction before. Dichlorosilane is also popular, has a lower growth rate, but it gives you a better selectivity if you're trying to deposit the epi in windows. It's not too unusual to have a wafer where you-- in cross-section where you have oxide like this and you've patterned the oxide. And you can grow, it turns out, by a process called selective epi. You can grow it in such a way that the epi only grows in the silicon, where the silicon is exposed.

So you get epi here and you get epi growth here. But you get nothing on top of the oxide. So it's automatically sort of self-aligned. And this is called selective epi growth. And to do that, you need dichlorosilane, and this is the reaction-- the silicon plus H2 plus Cl2 decomposes into another species. And that eventually decomposes on the surface to grow. And it forms HCl. And the HCl is important, it turns out, in etching the silicon off of the oxide, sort of keep it so you only deposit in the holes in the selective epi growth.

So those are two very commonly-used gases. All right. Let me just summarize. So far on thin film dep and epi, we have two main types. We said there's chemical vapor deposition, which we talked about today, and physical vapor deposition, which we'll talk about in the next couple lectures. Traditional epi growth uses atmospheric pressure. More modern systems use low pressure methods, typically in the 1 to 100 torr, these days.

We have a very simple model we developed for atmospheric CVD. And it led to rate-limiting regimes. Surface reaction rate, where the growth rate is exponentially dependent on temperature, activation energy of about 1.6 to 2 EV. And then at higher temperatures, you become mass transport limited. And you have very little dependence. Very slight dependence on temperature.

The mass transport limit regime is good in some ways. It gives a high growth rate. But the bad thing about it, it's very sensitive to how you design your reactor. So it's a little bit tricky. Reactor geometry has to be well designed. LPCVD in the 100-millitorr range, in a hot well batch reactor is used every day in fabs, particularly to deposit things such as a polysilicon gate, low-temperature oxide, and silicon nitride. And we're going to talk about these three types of films and this type of process next time.

All right. That's all I have for today's lecture. Just in case you came in late, the clipboard is going around. Make sure today, you put down on that clipboard your topic. I really want to have them so I can approve them. Tuesday is the deadline on that. Also, if you didn't pick up any prior homeworks, they're in the back.

[AI Auditory Hallucination]