This is a list of the topics you should focus on for Friday's quiz. Each topic also includes a reference to the related lecture slides (please use the revised slides found in the lecture notes section). For example, [L4:4-9] refers to Lecture 4, Slides 4 through 9. An asterisk (*) indicates that you should have a quantitative understanding of the material such that you could complete a quantitative quiz problem. No asterisk simply means a qualitative understanding of the material should be sufficient.

CMOS Technology and Logic Gate

- Recognize how a mosfet circuit diagram implements a logic gate [L3:14-22]
- Simple equivalent RC model for a CMOS logic gate [*L3:23-24]
- Transistor sizing using logical effort [*L3:28-37]
  [Also refer to ftp://ftp.mkp.com/Logical_Effort/Sutherland_Ch1.pdf]
  - Logical effort of inverters, nands, nors
  - Electrical effort, parasitic delays
  - Stage and path effort/delays
  - Using path logical/electrical effort to design each stage

Interconnect

- Where wire capacitance and resistance comes from [L4:4-10]
- RC wire delay models [*L4:11-13]
- Wire delay scaling: local vs. global wires [L4:14-15]
- Addressing wire delay: process, layout, circuit, architectural fixes [L4:16-25]

Synthesis

- Technology mapping using DAG covering [*L5:17-25]

Clocking

- Latch and flip-flop timing parameters [*L6:5,8,13,15-16]
- Where setup and hold times come from, latch design [L6:6-7,9-12,14]
- Clock distribution [L6:17-24]
- How skew and jitter affect overall circuit timing [*L6:25-27]

Power

- Basics of power consumption in CMOS gates [*L11:8-11]
- Techniques to reduce power [L11:12-31]

Bluespec Hardware Description Language

- You should have a qualitative understanding of all six bluespec lectures
- Designing with rules [*L8:2-22]
- Synchronous vs. asynchronous pipelines [*L8:23-28]
- Modules, methods, and interfaces [*L9:2-15]
- Sharing methods/state [*L9:16-20]
- Rule scheduling, rule synthesis, mapping Bluespec to hardware [*L10:2-35]
- Simple two-stage processor pipeline [*L12:16-36]
- Creating modular Bluespec designs [L13:2-30]
- One element FIFO implementation [*L13:32-33,35-36]
- Rule composition [L13:37-41]

Topics which will *not* be on the quiz

- CMOS fabrication
- Layout
- Verilog
- Boolean minimization
- Bluespec syntax - *Although we will not ask you to write any Bluespec code you should definitely understand any Bluespec code which we provide for you.*