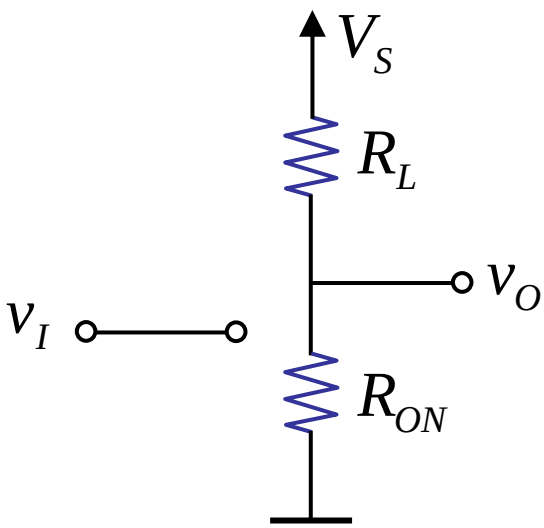
6.002 CIRCUITS AND ELECTRONICS

Energy, CMOS

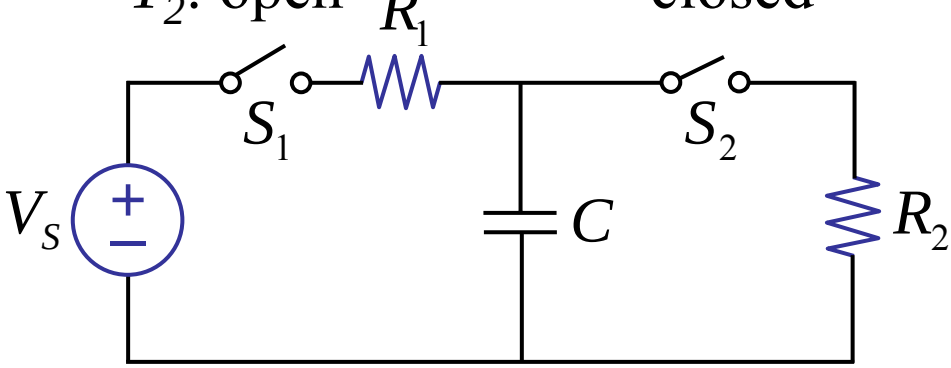
Review



$$P = \frac{V_S^{\,2}}{R_L + R_{ON}}$$ ★

T_1: closed open

T_2: open closed



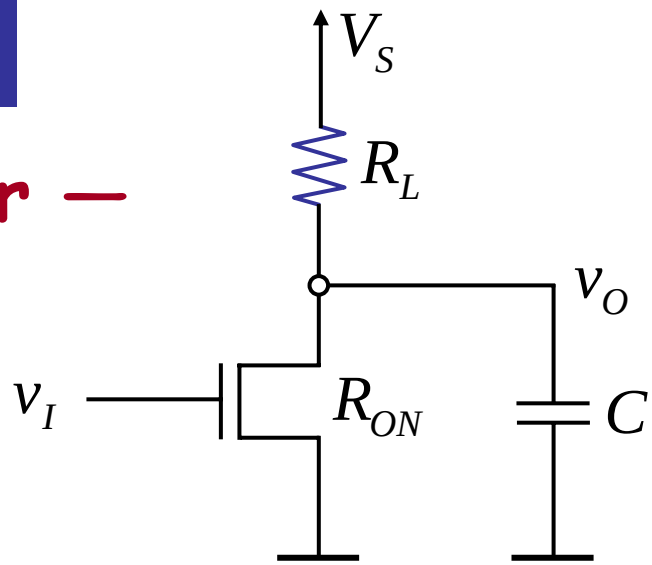
$$T = T_1 + T_2 = \frac{1}{f}$$

$$\overline{P} = CV_S^{\,2} f$$ ★★

Reading: Section 11.5 of A & L.

Review

Inverter —



Square wave input $T = \frac{1}{f}$

$$\overline{P} = \frac{V_S^{\,2}}{2R_L} + CV_S^{\,2} f$$

$\overline{P}_{STATIC}$ $\qquad$ $\overline{P}_{DYNAMIC}$

$R_L >> R_{ON}$

$\frac{T}{2} >>$ "RC"

time constant

Demo

independent of f. MOSFET ON half the time.

related to switching capacitor.

In standby mode, half the gates in a chip can be assumed to be on. So $\overline{P}_{STATIC}$ per gate is still $\frac{V_S^2}{2R_L}$.

In standby mode, $f \rightarrow 0$, so dynamic power is 0

Review

$$\overline{P} = \frac{V_S^{\,2}}{2R_L} + CV_S^{\,2} f$$

Chip with 10^6 gates clocking at 100 MHz

$$C = 1f\ F,\ R_L = 10\,K\Omega,\ f = 100\times 10^6,\ V_S = 5V$$

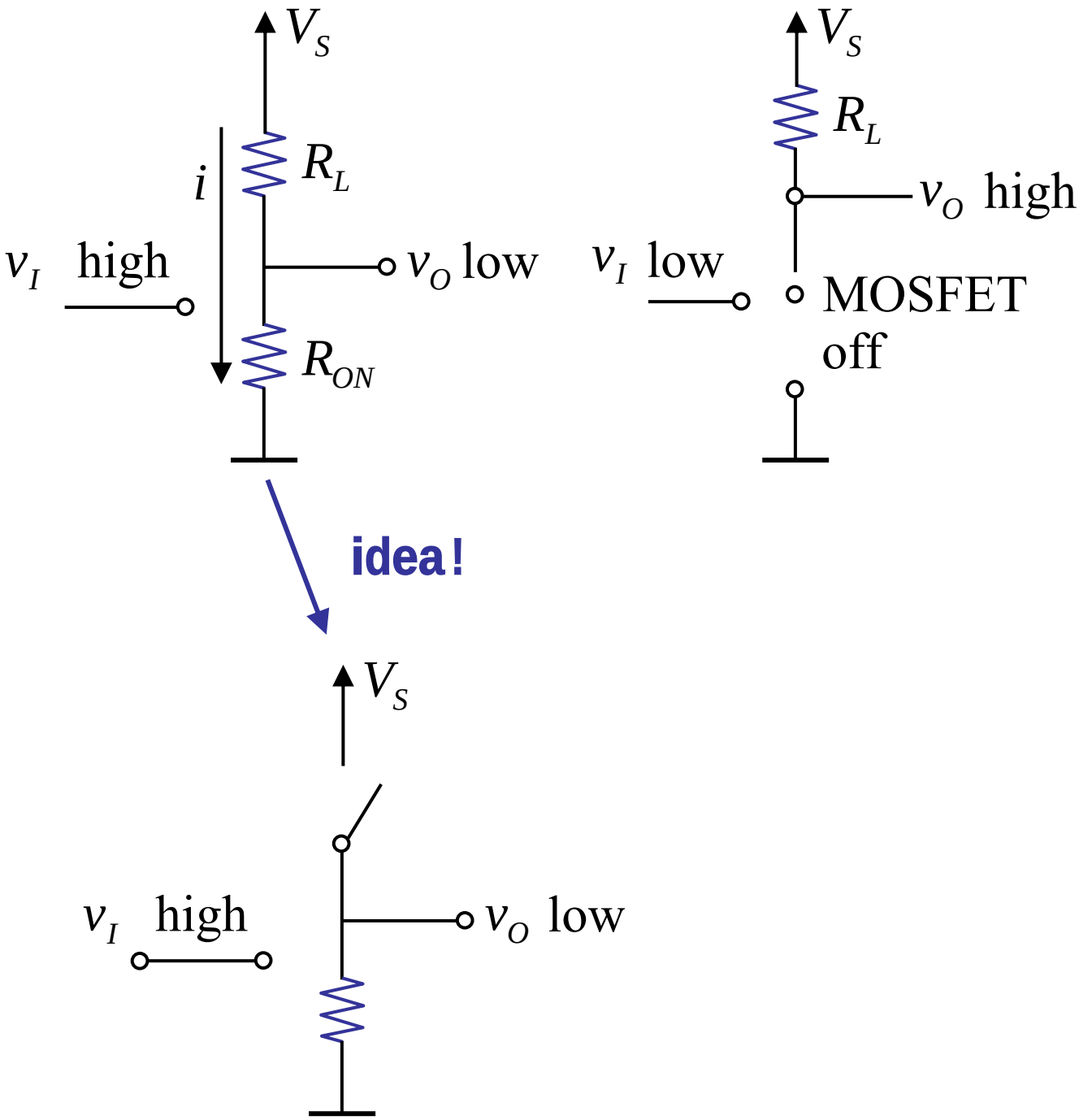
$$\overline{P} = \underset{gates}{10^6}\left[\frac{5^2}{2\times 10\times 10^3} + 10^{-15}\times 5^2\times 100\times 10^6\right]$$

$$= 10^6\left[1.25\ milliwatts + 2.5\ \mu watts\right]$$

$1.25KWatts$	+	$2.5Watts$
problem!		**not bad**
• independent of f • also standby power (assume ½ MOSFETs ON if $f \to 0$) • must get rid of this!		• αf • αV_S^2 reduce V_S $5V \to 1V$ $2.5V \to 150mW$

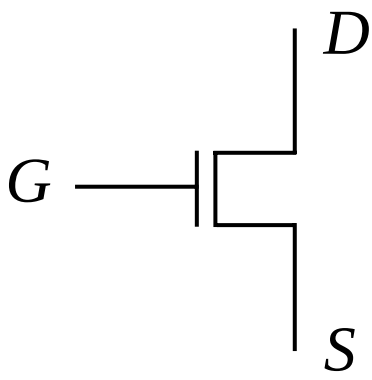
How to get rid of static power

Intuition:



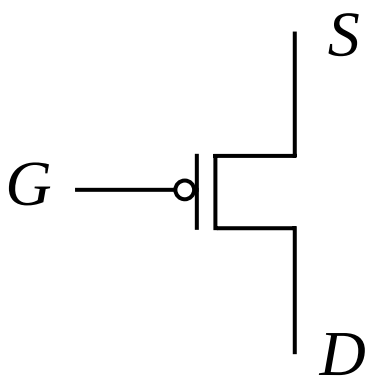
New Device PFET

- N-channel MOSFET (NFET)

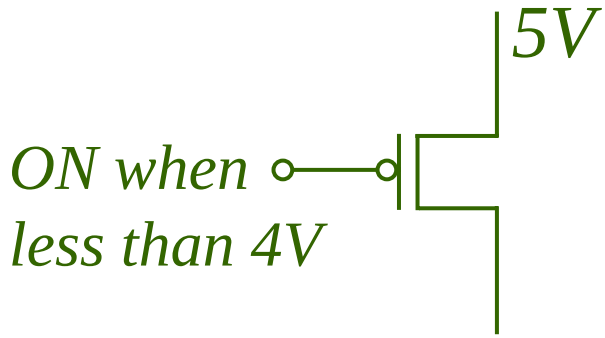


on when $v_{GS} \geq V_{TN}$
off when $v_{GS} < V_{TN}$
e.g. $V_{TN} = 1V$

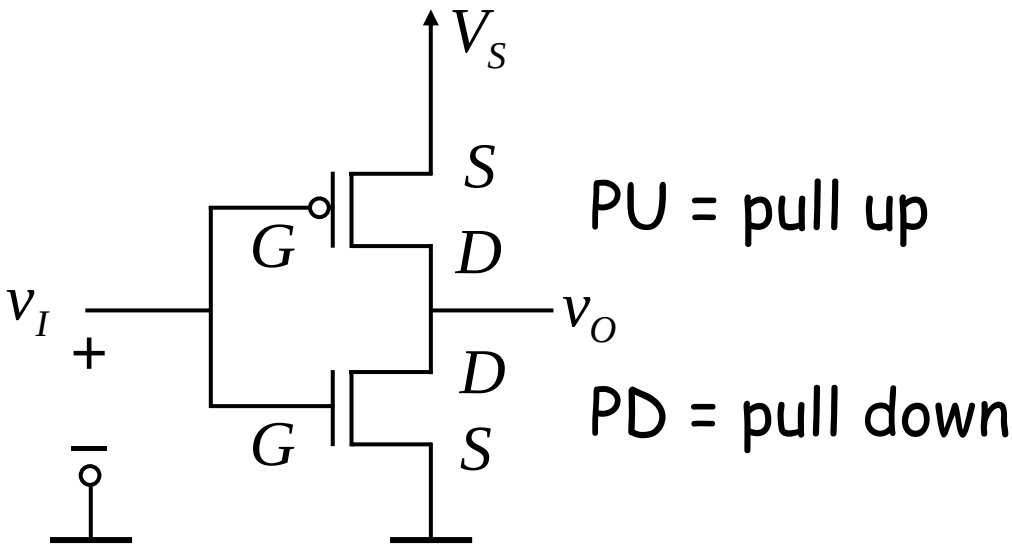
- P-channel MOSFET (PFET)



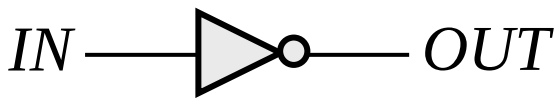
on when $v_{GS} \leq V_{TP}$
off when $v_{GS} > V_{TP}$
e.g. $V_{TP} = -1V$



Consider this circuit:



works like an inverter!



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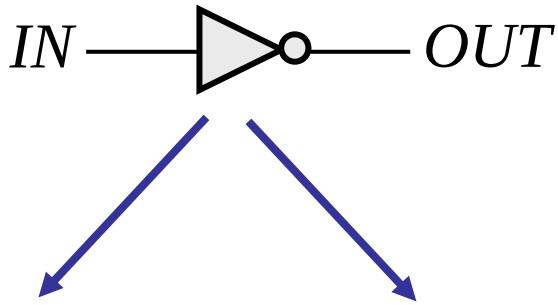
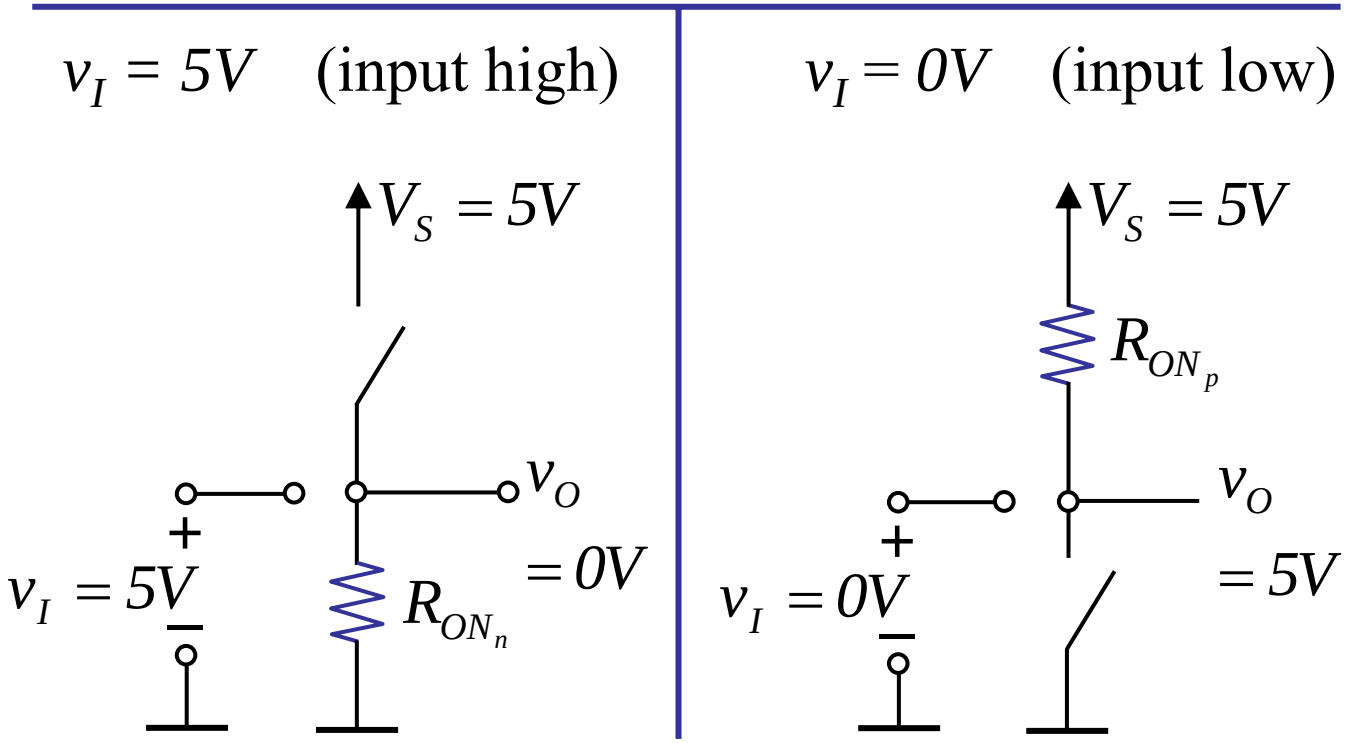


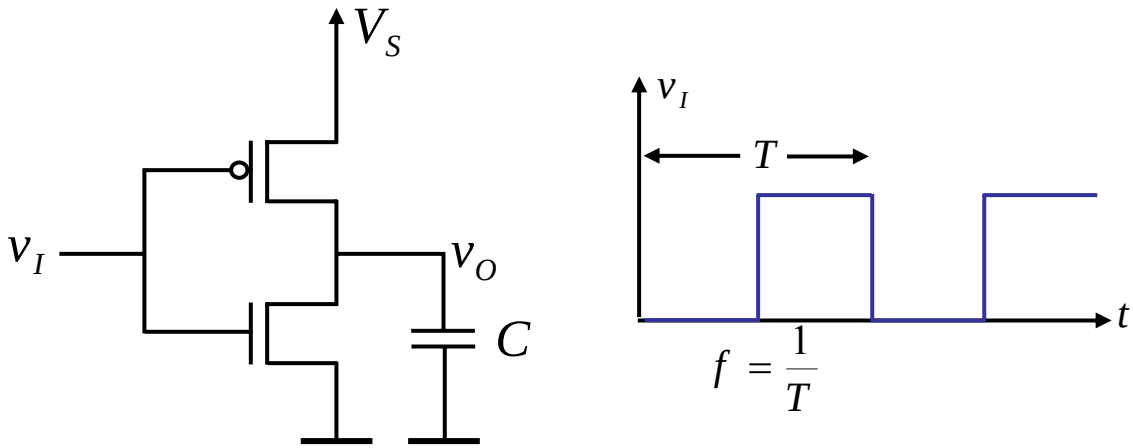


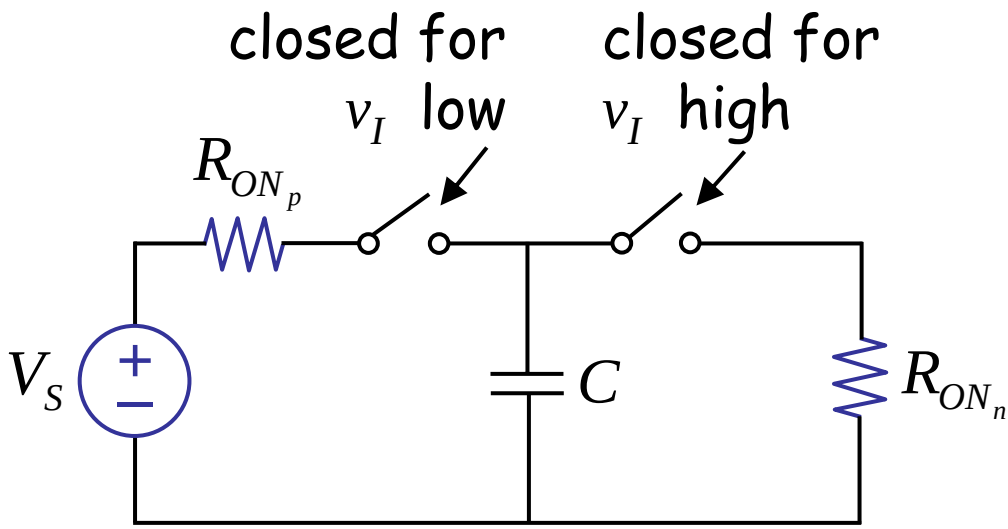
Called "CMOS logic" → Complementary MOS

(our previous logic was called "NMOS")

Key: no path from V_S to GND! no static power!

Let's compute $\overline{P}_{DYNAMIC}$





From ★★ $\overline{P} = CV_S^2 f$

For our previous example —

$$C = 1f\ F,\ V_S = 5V,\ f = 100MHz,\ 1$$

$$\overline{P} = CV_S^2 f$$

$$= 10^{-15} \times 5^2 \times 100 \times 10^6$$

$$= 2.5\ \mu\text{watts}\quad \text{per gate}$$

$$\overline{P} = 2.5\ \mu\text{watts}\quad \text{for } 10^6 \text{ gate chip}$$

Gates	f	$\overline{P}$	
10^6	100 MHz	~2.5 watts	Pentium?
2×10^6	300 MHz	~15 watts	PII?
2×10^6	600 MHz	~30 watts	PII?
8×10^6	1.2 GHz	~240 watts	PIII?
25×10^6	3 GHz	~1875 watts	PIV?

"keep all else same"

gasp!

How to reduce power

Ⓐ V_S 5V → 3V → 1.8V → 1.5V

~PIV → 170 watts → better, but high

and use big heatsink

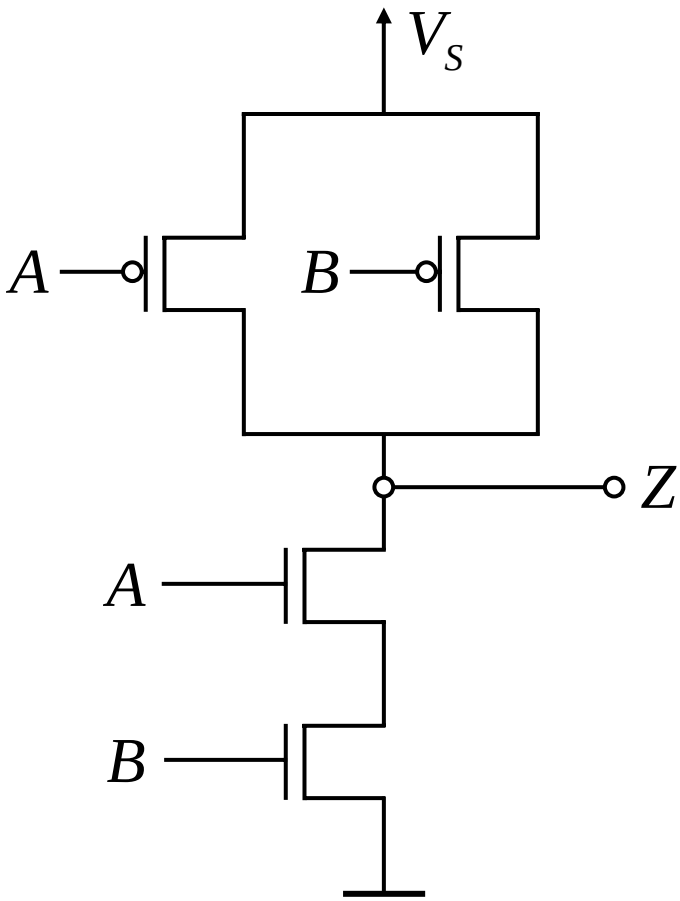
Ⓑ Turn off clock when not in use.

Ⓒ Change V_S depending on need.

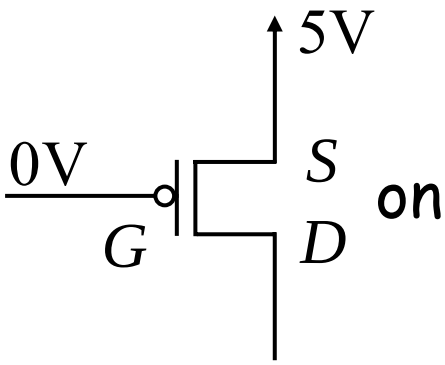
→ → next time:
power supply

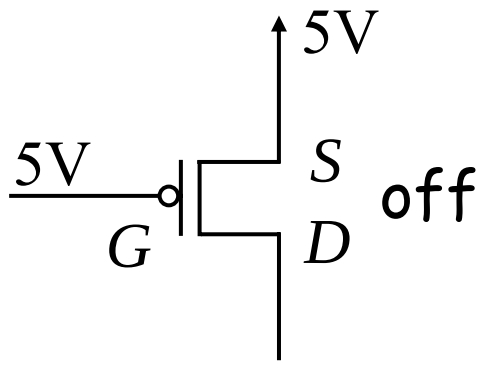
CMOS Logic

NAND:

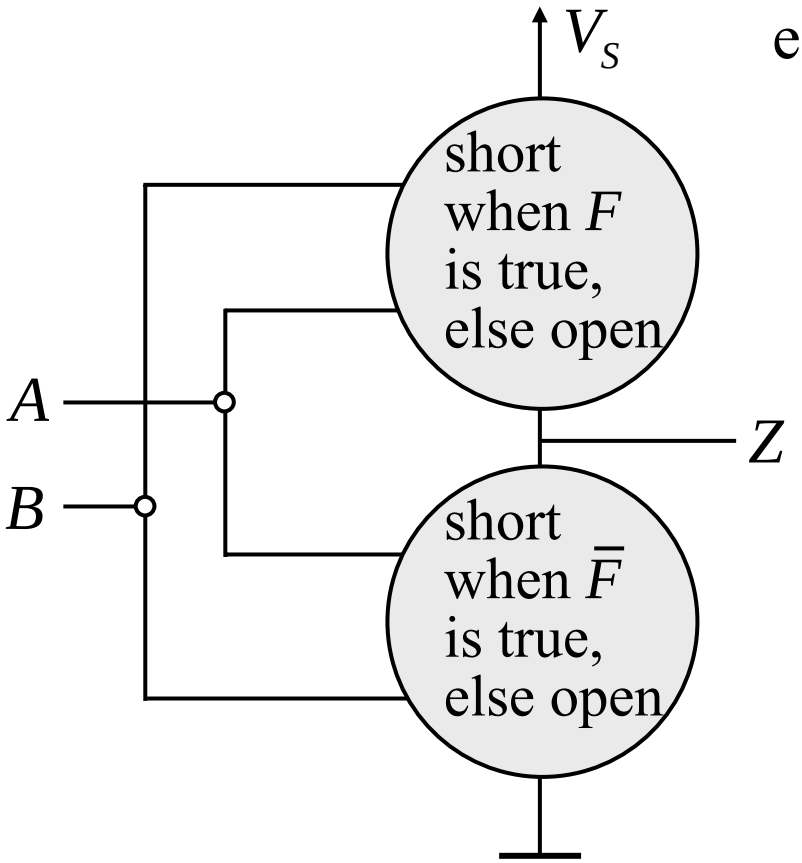


A	B	Z
0	0	1
0	1	1
1	0	1
1	1	0





In general, if we want to implement F



e.g. $F = \overline{A \cdot B} = \overline{A} + \overline{B}$

short when $A = 0$ or $B = 0$, open otherwise

short when $A \cdot B$ is true, else open

remember DeMorgan's law